Device and Circuit Level Gate Configuration Optimization for 2D Material Field-Effect Transistors

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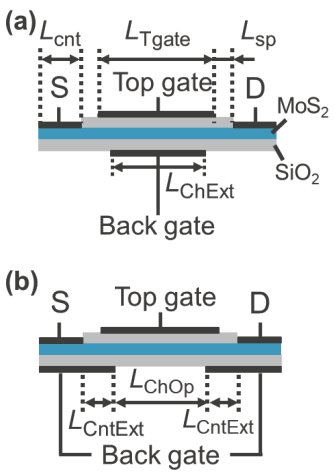
***Abstract*—A tied double gate structure has been shown to deliver optimal device-level performance in few-layer MoS_2 field-effect transistors. However, the enlarged gate capacitance from the added gate increases circuit-level power consumption and negatively affects minimum obtainable delay. Here, we therefore use a calibrated design-technology co-optimization approach that includes the interconnect load to evaluate back gate size reduction strategies in terms of power and delay. We consider the impact of a spacer region and varying interconnect length. We find that power consumption can be decreased by almost 20% by reducing the back gate overlap with the source-drain contacts without negatively affecting delay, as the carrier injection is occurring dominantly at the contact edges. We also show that opening the back gate underneath the channel provides additional benefit for locally interconnected devices.**

I. Introduction

Two-dimensional (2D) semiconductor channel materials open a path for the scaling of field-effect-transistors (FETs) to the 5nm node (N5) and beyond, through the promise of excellent gate control and limited short-channel effects [1], [2]. Of the many candidate 2D materials, MoS_2 is among the most studied, because it is stable in air, can be grown in large areas and has a high theoretical carrier mobility [3], [4]. So far, though, experimental MoS_2 FETs have not been able to realize their full potential, as they are hampered by non-idealities such as Schottky barriers at the source/drain (S/D) contacts, traps at the oxide interfaces and reduced mobility due to poor grown material quality [5]. While research is ongoing to continuously improve material growth, a parallel avenue to improve 2D FET performance is through gate configuration engineering. Previous simulation research which took into account the mentioned non-idealities showed that a tied double gate is preferable over a single gate as it improves gate control over both the channel and the Schottky contacts, while providing electrostatic doping of the access regions [6]. However, an extra gate means a larger gate capacitance, which increases power consumption (P) and limits the obtainable minimal delay (τ_{D}). In this work, we therefore optimize the back gate size to reduce P without negatively impacting τ_{D}. In doing so, we investigate the origin of the double gate improvement and determine which parts of the channel are most critical to be overlapped by both gates. The evaluation is carried out with calibrated Sentaurus Device TCAD simulations on the device level, which feed into a simple interconnect-aware circuit model.



L_{Tgate} (nm)	15
T_{ch} (nm)	1.4
W_{ch} (nm)	85
L_{cnt} (nm)	15
N_{dop} (cm^{-3})	5e18
EOT (nm)	0.7
V_{DD} (V)	0.65
f (GHz)	1
μ (cm^2/Vs)	14.5
D_{it} (cm^{-2})	6e12
E_{mid} (eV)	0.25
σ_{DIT} (eV)	0.48
ϕ_{SB} (meV)	720
CPP (nm)	42

Fig. 1: Simulated bilayer MoS_2 FETs and parameters. Mobility (μ), density and distribution of acceptor-type MoS_2-oxide traps (D_{it}, E_{mid}, σ_{mid}) and Schottky barrier height at the S/D contacts (ϕ_{SB}) were calibrated to experiment [5]. Dimensions and bias conditions align with imec's N5 process assumptions.

II. Modeling and Configuration Set-up

We consider two different tied double gate bilayer MoS_2 configurations to assess in which part of the channel the added back gate control is most critical. In the first configuration (shown in Fig. 1(a)) the back gate covers the center of the channel and is progressively extended symmetrically towards the S/D contacts by increasing the parameter L_{ChExt}. In the second configuration (shown in Fig. 1(b)), the back gate is split and covers the S/D contacts. The two parts are progressively extended symmetrically towards the channel center when L_{CntExt} is increased. Both 2D FET configurations have top contacted S/D contacts and allow for the presence of a spacer region (L_{sp}) between S/D contacts and the top gate. Default parameter values are shown in the table of Fig. 1.

Our modeling approach relies on a Synopys SDevice set-up modified with a 2D density of states, which was verified with atomistic non-equilibrium Green's function simulations

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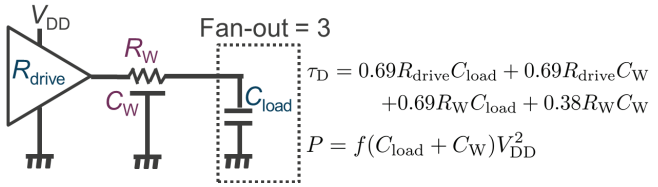

Fig. 2: Circuit model for the calculation of delay (τ_D) and power (P). R_{drive} and C_{load} are extracted from the 2D FET SDevice simulations. R_W and C_W represent wire resistance and capacitance and are extracted from a calibrated resistivity model for a three-level Cu-TaN/Ru interconnect scheme and Sentaurus Raphael simulations respectively [6], [7].

and for which non-idealities were calibrated to experimental bilayer devices [5]. Considered non-idealities are traps at the MoS_2-oxide interfaces, Schottky barriers at the S/D contacts and a limited mobility. The calibrated parameter values are shown in the table of Fig. 1. For the circuit-level evaluation, the SDevice model provides input to a simple circuit model that includes the interconnect load (shown in Fig. 2) [6]. Delay and power are calculated in the Elmore approximation.

III. Device-level evaluation

From the device-level transfer characteristics in Fig. 3, it is clear that the overlap of the back gate with the S/D contacts can be reduced without a significant performance penalty. Performance in terms of on-current (I_{ON}) and subthreshold swing (SS) improves as L_{ChExt} increases, with the improvement quickly saturating as the back gate extends underneath the S/D contacts. Even for the large, calibrated Schottky barrier (ϕ_{SB}) of 720 meV, there is only a small benefit to extending the back gate beyond alignment with the S/D contacts (L_{ChExt}=15 nm, grey dashed line in Fig. 3), as the carrier injection is occurring mainly at the contact edges [8], [9]. For a lower ϕ_{SB} of 200 meV, the improvement with increasing L_{ChExt} only comes from better channel control, so even for zero overlap with the S/D contacts the same performance as a full double gate is obtained.

Fig. 4, in which the back gate is extended from the contact edges, additionally shows that the overlap of the back gate with the center of the channel can be removed with limited impact on performance. This is particularly true for the large ϕ_{SB}, where the case of 5 nm L_{CntExt} (corresponding to 5 nm channel opening) almost coincides with the full back gate curve. This again confirms that for this case, control over the Schottky barrier through proximity to the S/D contact edges accounts for the largest share of the improvement delivered by the back gate. In the case of the low ϕ_{SB}, however, the current is channel limited and the overlap contributes significantly to performance, which means performance is progressively degraded as the back gate is opened underneath the channel.

From the device level evaluation, two strategies therefore emerge to reduce back gate size with limited impact on I_{ON} or SS: decreasing the S/D contact overlap and splitting the back gate, creating an opening underneath the channel.

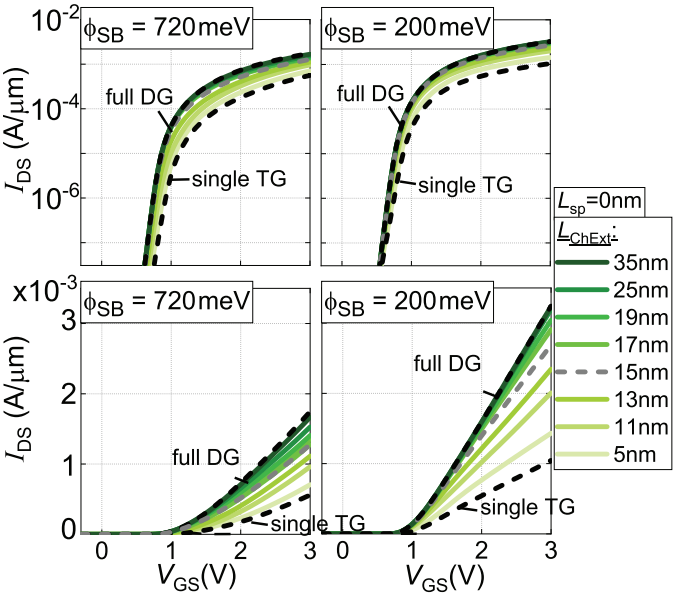

Fig. 3: Simulated transfer characteristics of the configuration in Fig. 1(a) for varying back gate extension underneath the channel and for two values of ϕ_{SB}. Top plots are in logarithmic scale, bottom in linear. The dashed lines correspond to a full double gate (DG) and single top gate (TG).

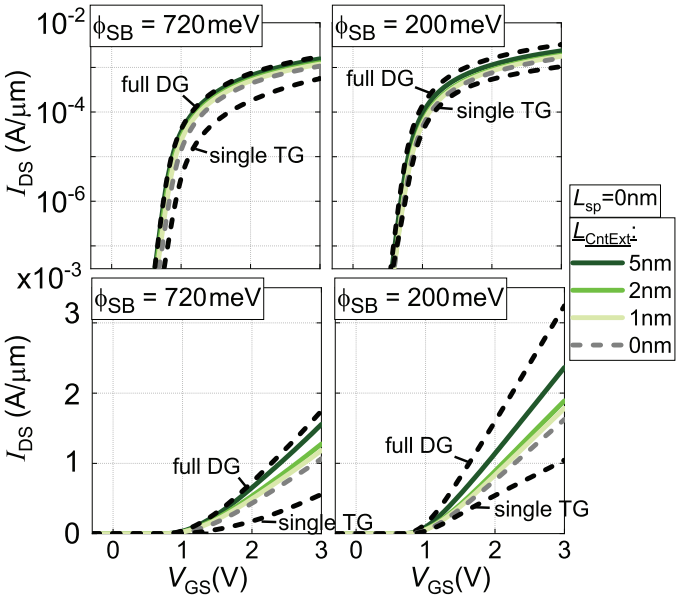

Fig. 4: Simulated transfer characteristics of the configuration in Fig. 1(b) with varying extension of the back gate from the contacts and for two values of ϕ_{SB}. Top plots are in logarithmic scale, bottom in linear. The dashed lines correspond to a full double gate (DG) and single top gate (TG).

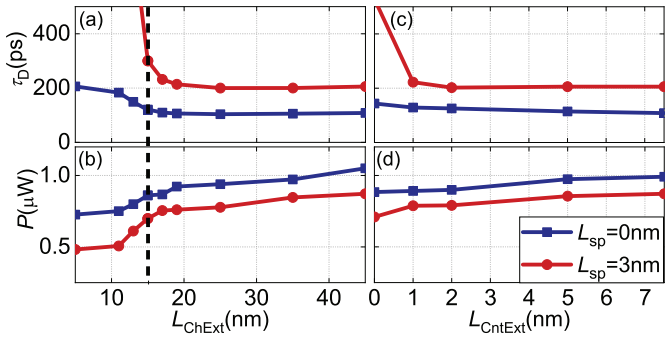

Fig. 5: Simulated delay at optimal wire dimensions and corresponding power consumption for the 2D FET in Fig. 1 for varying extension of the back gate underneath the channel and from the contacts. L_w is 300CPP. The dashed line indicates the boundary between the S/D contacts and the channel.

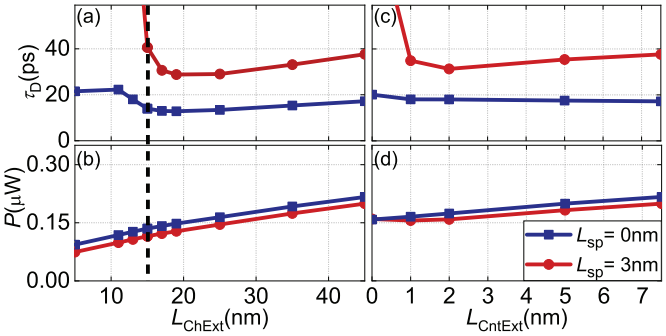

Fig. 6: Simulated delay at optimal wire dimensions and corresponding power consumption for the 2D FET in Fig. 1 for varying extension of the back gate underneath the channel and from the contacts. L_w is 3CPP. The dashed line indicates the boundary between the S/D contacts and the channel.

IV. Circuit-level evaluation

We now evaluate these strategies in terms of circuit-level τ_D and P in Figs. 5 and 6, first in the case without a spacer. Fig. 5(a-b) shows for a 300CPP wire length (L_w) that τ_D is almost unaffected from a reduction of the S/D overlap from 15 nm to 1 nm, while P drops with 18% to 0.87 μW. Reducing L_{ChExt} more decreases P further, but at the expense of τ_D. Fig. 5(c-d) shows that opening the back gate underneath the channel at the most reduces P with 12%, at the expense of a 30% τ_D increase. For constant τ_D, a 5 nm opening only delivers 2% P improvement, which might not be worth the added process complexity. For shorter wires (L_w=3CPP, Fig. 6), the wire capacitance is less dominant, allowing for greater benefits from the back gate reduction: a S/D overlap reduction to 1 nm results in a 35% reduction in P to 0.14 μW, accompanied with a 25% decrease in τ_D. Even a 5 nm channel opening underneath the channel now reduces P with 8%.

Next, we check if the same trade-offs hold when a spacer is present for the top gate. Such spacer is often unavoidable due to process limitations, but can also intentionally be introduced

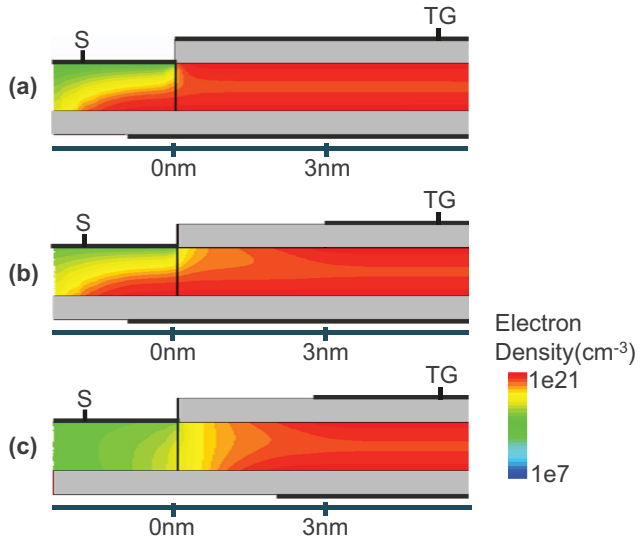

Fig. 7: Electron density profile at the source contact for (a) L_{sp}=0 nm, L_{ChExt}=17 nm, (b) L_{sp}=3 nm, L_{ChExt}=17 nm and (c) L_{sp}=3 nm, L_{ChExt}=11 nm. V_{GS} is 3 V. Other configuration details are listed in Fig. 1.

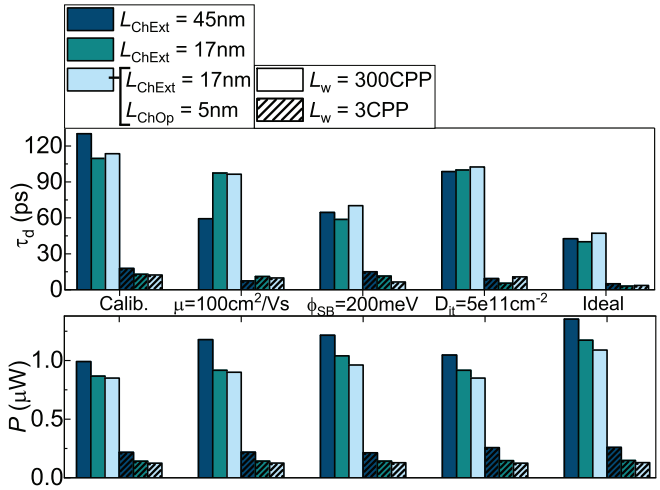

Fig. 8: Delay at optimal wire dimensions and corresponding power consumption in various projected scenarios for a full gate, compared to a configuration with reduced S/D contact overlap and a configuration with an additional channel opening. The ideal case combines all projected improvements. L_{sp} is 0nm. Other configuration details are listed in Fig. 1.

to reduce parasitic capacitance [10]. Indeed, Figs. 5 and 6 confirm the same trends for L_{sp}=3 nm, although a larger penalty exists for reducing the overlap of the back gate with the spacer region, because of a sharply increasing access resistance. Fig. 7 shows a 1 nm S/D overlap is sufficient to induce an electron density in the spacer region similar to the no spacer case (Fig. 7(a) and (b)). If the overlap with the spacer region is reduced, the electron density drops (Fig. 7(c)), resulting in a larger resistivity.

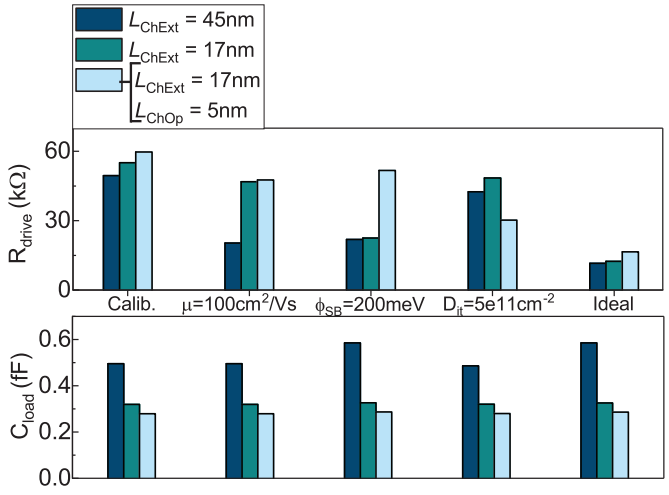

Fig. 9: Drive resistance and load capacitance in various projected scenarios for a full gate, compared to a configuration with reduced S/D contact overlap and a configuration with an additional channel opening. The ideal case combines all projected improvements. L_{sp} is 0nm. Other configuration details are listed in Fig. 1.

Finally, we project whether the τ_{D} and P advantages of reducing the back gate hold in a number of improvement scenarios that represent a future maturing of the technology. Fig. 8 shows that the two back gate reduction scenarios, one with the S/D overlap reduced to 1 nm and one with an additional channel opening of 5 nm, can be seen to retain the P advantage at similar τ_{D} to the full back gate configuration. This is generally true for both wire lengths, but for the longer wires ($L_{\mathrm{w}} = 300$CPP), adding the channel opening on top of the S/D overlap reduction can negatively affect τ_{D}. Fig. 9 shows that it is indeed the consistent drop in C_{load} with the decrease in back gate size that causes the lower P, even when R_{drive} tends to increase.

V. Conclusion

We showed using interconnect-aware calibrated TCAD simulations that back gate reduction is a viable strategy in double gate devices to avoid power consumption penalties from the increased gate capacitance while retaining the delay advantage over a single gate device. Although this delay advantage comes both from an improved control over the channel and the Schottky contacts, the overlap with the latter can be strongly reduced as a result of edge injection of the carriers. We showed that the advantages of back gate reduction increase for locally interconnected devices. This study provides a guideline in the trade-off between delay-power performance and process complexity.

Acknowledgments

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