# TCAD Framework to Estimate the NBTI Degradation in FinFET and GAA NSFET Under Mechanical Strain

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***Abstract*--A physics-based TCAD framework is used to estimate the interface trap generation ($\Delta N_{IT}$) during Negative Bias Temperature Instability (NBTI) stress in P-channel FinFET and Gate All Around (GAA) Nano-Sheet (NS) FET. The impact of mechanical strain due to channel length scaling ($L_{CH}$) on $\Delta N_{IT}$ generation is estimated. The bandstructure calculations are used to explain the impact of mechanical strain on $\Delta N_{IT}$ generation.**

***Keywords*—NBTI, RD model, GAA-NSFET, FinFETs, mechanical strain, RD model, $L_{CH}$ scaling.**

## I. Introuction And Background

The NBTI continues to remain a critical reliability issue in P-channel FinFETs [1,2] and GAA NSFETs [3]. It results in buildup of positive charges in the gate insulator which shift various device parameters over time and hampers the longtime operation of devices and circuits. Therefore, the accurate modeling of NBTI degradation is necessary for reliable operation of devices and circuits at advanced technology nodes. Although the physical mechanism of NBTI is debated [4], a framework explained in [5] has been used to predict the DC and AC stress and recovery kinetics in various technologies such as Si and Si capped SiGe planar, Si and SiGe FinFET and FDSOI, and Si SOI FinFET having HKMG gate stacks [5]-[11]. The framework uses uncorrelated contributions from interface ($\Delta V_{IT}$) and bulk ($\Delta V_{OT}$) trap generation and trapping of holes ($\Delta V_{HT}$) in pre-existing traps.

The framework of [5] uses Reaction-Diffusion Model (RD Model) to calculate trap density ($\Delta N_{IT}$) at channel/interlayer (IL) and IL /High-K interfaces, Transient Trap Occupancy Model (TTOM) to calculate their charge occupancy and contribution to $\Delta V_{IT}$, and analytical models to model the $\Delta V_{HT}$ and $\Delta V_{OT}$ time kinetics. Analyses of multiple technologies [5]-[11] have established that although the overall $\Delta V_T$ at shorter stress time is due to the multiple subcomponents, $\Delta V_{IT}$ dominates end of life (EOL) $\Delta V_T$ at lower bias use conditions.

Recently, RD model with proper physics has been implemented in Sentaurus Device using the Multi-State-Configuration (MSC) framework and Capture-Emission Depassivation (CED) model for inversion hole and IL field assisted breaking of interfacial Si-H bonds [12]-[14]. Figure 1 shows the schematic of MSC hydrogen transport model. In this model, hydrogen (H) passivated bonds (X–H) at the channel/gate insulator interface get broken, which create defects (X–) and H atoms during the stress phase. These H atoms diffuse in the gate insulator bulk and react with other H passivated bonds (Y–H), which result in additional defects (Y-) and $H_2$ molecules, which diffuse away in the gate stack layers. Note that, all the bulk insulator defects are assigned to IL/High-K interface for analysis. During recovery, the diffused $H_2$ reach out and react with Y- defects and create Y-H bonds and H atoms. These H atoms further react (re-passivation) with X-defects and form X-H bonds. With proper capacitance ratio, trap contribution from both the interfaces is used to compute $\Delta N_{IT}$. CED model is used for inversion hole (hole density $p_H$) and IL field (Eox) assisted breaking of interfacial Si-H bonds as shown in Fig.2 [12]-[14]. In the presence of oxide electric field (Eox), inversion layer hole tunnel to X-H polarized bonds, get captured and broken due to thermal dissociation (activation $E_{AKF1}$). The framework calculates reactions at channel/IL and IL/High-K interfaces and diffusion of H and $H_2$.

The RDM framework has been successfully validated against the measured $\Delta N_{IT}$ time kinetics in Si and SiGe channel FinFETs [12]-[13]. The model can accurately predict the stress and recovery time kinetics for different $V_{GSTR}$ and T using only four process dependent parameters: Pre-factor for Si-H bond dissociation ($K_{FIT}$), Activation energy ($E_{AKF}$), Tunneling parameter ($\Gamma_0$), and bond polarization factor ($\alpha$).

## II. Scope Of This Work And Experimental Details

Figure 3 shows the schematic of the simulation framework used to calculate the $\Delta N_{IT}$ time kinetics in FinFET and NS-FET devices. The Sentaurus Process [15] is used to generate FinFET and NSFET structures with a process flow that is consistent with actual practice including the epitaxial SiGe Source-Drain, whose volume decides the stress distribution in the fin and the three nano-sheets [16-17], as shown in Fig. 4. The structure uses a metal backend for $H_2$ diffusion. Note that unlike Sentaurus Structure Editor, the Sentaurus Process rightly consider the process induced strain in the channel due to variation in $L_{CH}$. The Bandstructure calculations [18] by the tight binding method are used to determine the impact of mechanical strain on the tunneling effective mass ($m_T$) and valence band offset ($\varphi_B$) which in turn affect the parameter $K_{F10}$ and $\Gamma_0$ (Fig.2 of reference [14]). Table-1 shows the dimensional description of the devices used in this work. The RDM is used to calculate generation and passivation of $\Delta N_{IT}$ at channel/ IL and IL/High-K interfaces in FinFET and GAA NSFET for different $L_{CH}$.

## III. Evaluation Of Strain Impact

Figure 5 shows the 3D isometric view of Source/Drain SiGe epi induced stress distribution along the channel direction ([110]) in FinFET and NSFET for a fixed channel length of 14nm. Figure 7 shows the 1D cut of the stress profile along the channel direction (Stress-ZZ) for FinFET and NSFET. Note that SiGe epi dominantly impacts the top part of the Fin in FinFET (Fig.7(a)) and top sheet in case of NSFET (Fig.7(b)).

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The 1D cut of the stress distribution in all the three directions of FinFET and NSFET is shown in Fig. 6. The stress magnitude in the other two directions (Stress-XX and Stress-YY) is negligible in both FinFET and NSFET. Figure 8 shows the $L_{CH}$ dependence of integrated stress along the channel direction for FinFET and NSFET. The integrated stress in the FinFET is higher than the average of the integrated stress in all sheets of NSFET for different $L_{CH}$, and it increases with a decrease in $L_{CH}$.

The impact of uniaxial compressive stress (UCS) on the valence bandstructure of (110) and (100) oriented Si surface is shown n Fig. 9. The impact of channel stress on $m_T$ and $\varphi_B$ is different in FinFET and NSFET due to different conducting surface domination; (110) in FinFET and (100) in the case of NSFET. The relative increase in $m_T$ is higher for FinFET compared to NSFET (Fig.10) while relative change in $\varphi_B$ is smaller for both FinFET and NSFET (Fig. 11). Figure 12 shows the impact of increase in strain (or decrease in $L_{CH}$) on the $K_{F10}$ and $\Gamma_0$. With increases in strain (or decreases in $L_{CH}$), the $K_{F10}$ reduces and $\Gamma_0$ increases. The reduction in $K_{F10}$ and increase in $\Gamma_0$ are higher for FinFET compared to NSFET (Fig.11).

## IV. MSC (DEVICE) SIMULATION

For device simulations, both FinFET and NSFET are calibrated for the same $I_{OFF}$ current by changing the metal work function. The MSC simulations are then performed for different $V_{GSTR}$ and for different $L_{CH}$ in both the architectures. Both the FinFET and NSFET show similar time kinetics and longtime power-law time dependence, as shown in Fig.13. Figure 14 compares the fixed time $\Delta N_{IT}$ with and without mechanical strain for different $L_{CH}$ at operating conditions for both the architectures. For both FinFET and NSFET, the $\Delta N_{IT}$ reduces with a reduction in $L_{CH}$. For a fixed $L_{CH}$, the NSFET shows smaller degradation compared to FinFET when strain is not considered. This ascribed to the lower field in the NSFET because of the fully depleted sheet and lower precursor bond density for (100) surface compared to (110) surface. These results are consistent with the measurement data shown in [3] for long channel FinFET and NSFET where strain due to SiGe epi will be minimal. However, when the effect of strain is considered, the actual $\Delta N_{IT}$ becomes lower for FinFET compared to NSFET due to a significant increase in $m_T$ for (110) surface compared to (100) surface (Fig. 13(a)). The reduction in $\Delta N_{IT}$ is higher for shorter $L_{CH}$ due to higher mechanical strain. The Voltage Acceleration Factor (VAF), an important parameter to extrapolate the degradation measured at higher stress voltages to operating voltage, of NSFET is smaller compared to FinFET, as shown in Fig. 15. The lower VAF for NSFET suggests higher NBTI degradation at the operating voltage. Figure 16 compares the VAF for different $L_{CH}$ in FinFET and NSFET. Although the unstrained VAF is smaller for FinFET compared to NSFET, the strained VAF is higher for FinFET compared to NSFET due to higher $m_T$ variation which increases the $\Gamma_0$ (Fig. 11).

## V. CONCLUSION

Sentaurus Device framework with proper physical models and Sentaurus Process are used to study the NBTI in FinFET and NSFET devices considering the impact of mechanical strain for different $L_{CH}$. The NSFET shows lower degradation compared to FinFET when the effect of strain is not considered. This is the case for long channel devices where the SiGe epi induced strain is small. However, the NSFET shows higher degradation than FinFET when effect of strain is considered. This is primarily due to (110) dominated surface in FinFET which shows relatively higher increase in $m_T$ compared to (100) dominated surface in NSFET.

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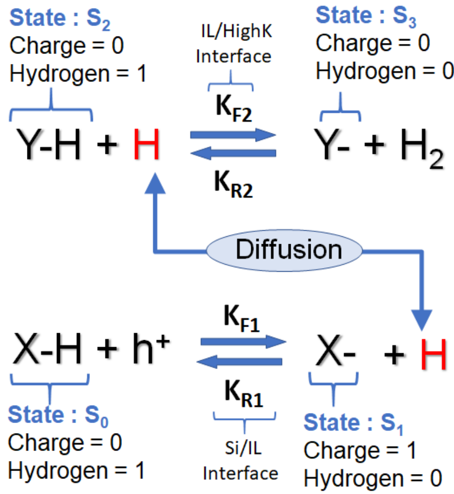


Fig.1. Schematic of the Multi-State-Configuration (MSC) Hydrogen transport degradation model and state diagram of Hydrogen depassivation (by Capture Emission Depassivation or CED model, Fig.2). MSC is used to model reactions between the mobile hydrogen elements and localized hydrogen states such as silicon-hydrogen bonds at the Si–SiO2 interface. Electrically active defects at Si–SiO2 interface are denoted as X-H bonds because of its unknown nature. Y-H bonds are located at IL/HighK interface. $S_0$, $S_1$, $S_2$ and $S_3$ are the state occupation probabilities used in MSC model. $K_{F1}$ $K_{R1}$, $K_{F2}$ and $K_{R2}$ are the forward and reverse reaction rates at Si/IL and IL/HighK interface respectively.

$$K_{F1} \sim K_{F10} * \exp(-E_{AKF1}/kT) * \exp(\Gamma_E E_{ox})$$

$$K_{F10} \sim p_H T_H \sigma$$

$$T_H \sim \exp(-\sqrt{m_T \varphi_B})$$

$$\Gamma_E = \Gamma_0 + \alpha/kT$$

$$\Gamma_0 \sim \sqrt{\frac{m_T}{\varphi_B}}$$

H X $p$ $E_{OX}$

Fig.2. Schematic of H passivated bond dissociation process at the channel/IL interface used in Capture Emission Depassivation (CED) model. Inversion layer holes tunnel into polarized interfacial X-H bonds, aided by oxide electric field.

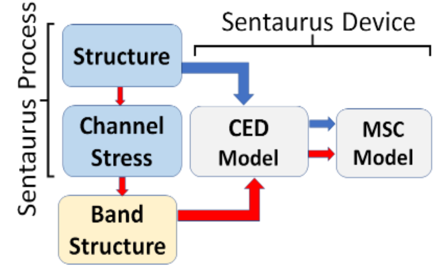


Fig.3. TCAD simulation framework: structure, material and strain are calculated from process simulation, band structure is calculated using tight binding method, CED and MSC models are used to calculate $\Delta N_{IT}$ kinetics.

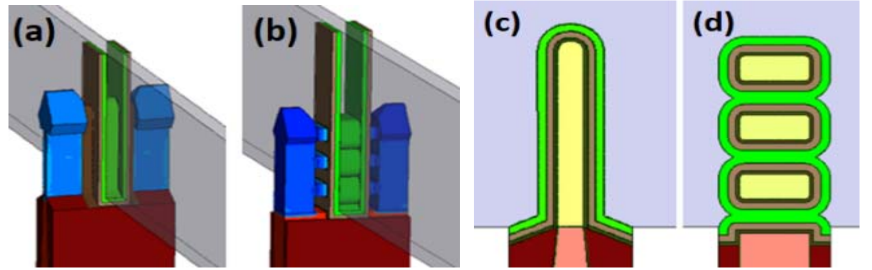


Fig.4. Isometric view of 3D (a) p-FinFET, and (b) p-NSFET structure with raised Source drain and lateral backend for hydrogen diffusion. 2D cross section of the channel in (c) p-FinFET, and (d) p-NSFET showing IL, High-K, TiN-Cap and Tungsten layers. Equivalent Oxide Thickness (EOT) of 1nm is used.

| FinFET | NSFET |
|---|---|
| Fin Height = 50nm | Nano-Sheet thickness = 6nm |
| Fin Width = 6nm | Nano-sheet width = 15nm |
| | Inter-Sheet Gap = 5nm |

Table I. Dimensions details of the device used in this work.

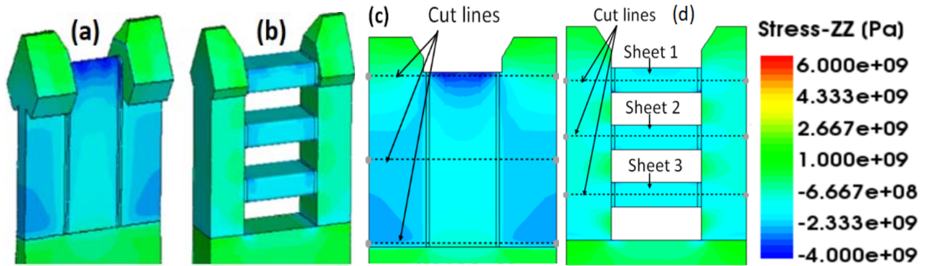


Fig.5. Isometric view of 3D (a) p-FinFET, and (b) p-NSFET showing stress distribution along the channel. Corresponding 2D view of (c) p-FinFET and (d) p-NSFET from source to drain with cut-lines for next 1D plot.

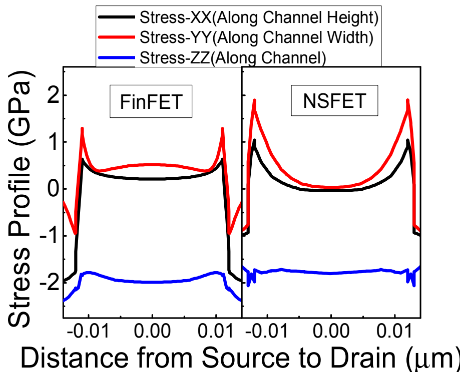


Fig.6. Stress profile from Source to Drain in (a) p-FinFET in the middle of the fin, and (b) p-NSFET in the middle of the sheet-2.

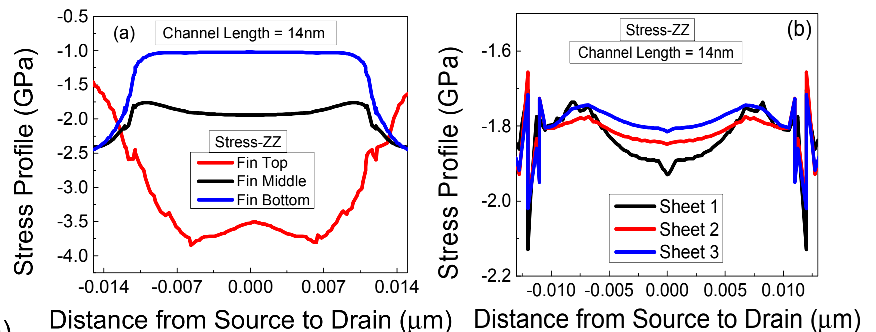


Fig.7. 1D stress profile (Stress-ZZ) in (a) p-FinFET at three positions (cut lines are shown in Fig. 5) and (b) all three sheets of p-NSFET. Fin top in FinFET and Sheet1 in NSFET are showing higher stress because of SiGe- epitaxial SD volume. TCAD simulation.

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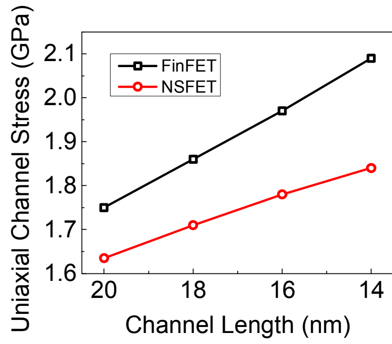


Fig.8. Uniaxial compressive stress along the channel for different channel length for p-FinFET and p-NSFET. TCAD simulation.

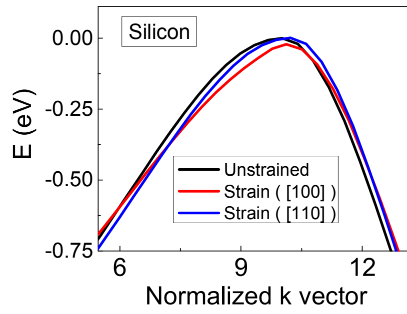


Fig.9. E-K diagram of the top most valence band with and without Uniaxial Compressive Stress (UCS) for [110] (dominating surface in FinFET) and [100] (dominating surface in NSFET)

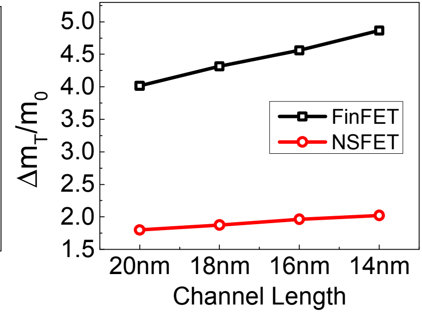


Fig.10 Impact of UCS on barrier height $\varphi_B$ for p-FinFET and p-NSFET.

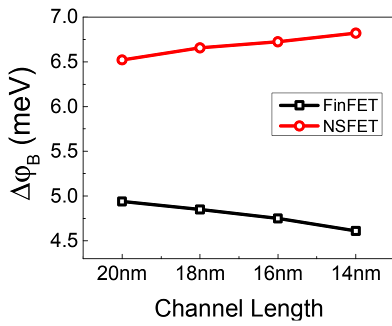


Fig.11. Impact of UCS on barrier height $\varphi_B$ for p-FinFET and p-NSFET.

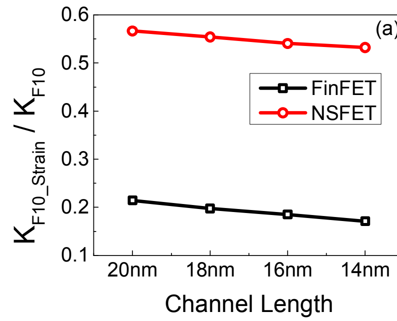


Fig.12. Mechanical strain impact on bond dissociation pre-factor (a) $K_{F10}$, and (b) field acceleration parameter ($\Gamma_0$) for different channel length. Parameters are normalized to unstrained values. TCAD simulation.

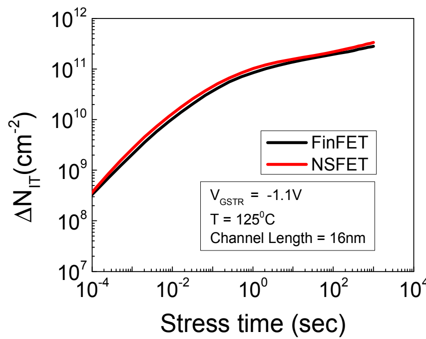


Fig.13. Consistency in $\Delta N_{IT}$ time kinetics in p-FinFET and p-NSFET for same $V_{GSTR}$-T and channel length. TCAD simulation.

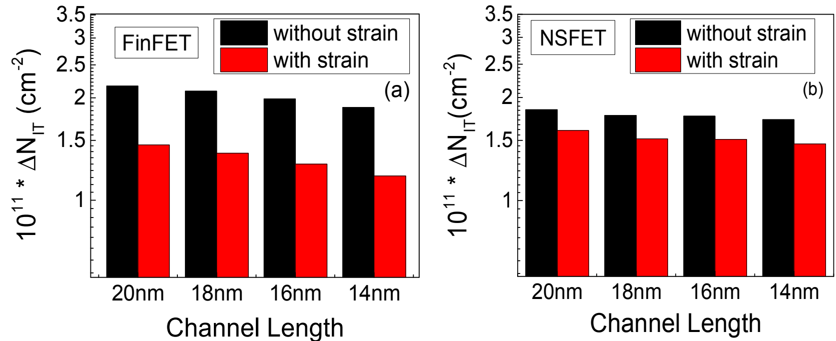


Fig.14. Mechanical strain impact on fixed time $\Delta N_{IT}$ of 1Ks for (a) p-FinFET, and (b) p-NSFET, showing higher degradation in NSFET as compared to p-FinFET when proper strain calculation is incorporated in TCAD simulation, at fixed $V_{GSTR}$ = -0.8V and T= 125$^0$C.

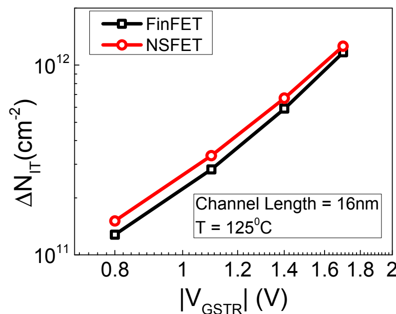


Fig.15. Fixed time $\Delta N_{IT}$ comparison between p-FinFET and p-NSFET at 1Ks vs $V_{GSTR}$ at fixed channel length. TCAD simulation.

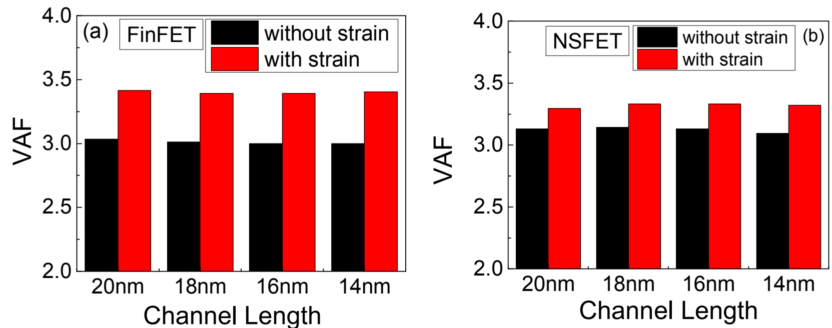


Fig.16. Mechanical impact on voltage acceleration factor (VAF ∝ $\Gamma_0$) for both (a) p-FinFET, and (b) p-NSFET for different channel lengths. T=125$^0$C. TCAD simulation.

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