Compact Modelling of Single Event Transient in Bulk MOSFET for SPICE: Application to Elementary Circuit

Neil Rostand
ONERA/DPHY, Univ.of Toulouse
Univ. Grenoble Alpes, CEA, LETI
Toulouse/Grenoble, France
neil.rostand@onera.fr

Sébastien Martinie
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
sebastien.martinie@cea.fr

Joris Lacord
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
joris.lacord@cea.fr

Olivier Rozeau
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
olivier.rozeau@cea.fr

Olivier Billoint
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
olivier.billoint@cea.fr

Jean-Charles Barbé
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
jean-charles.barbe@cea.fr

Thierry Poiroux
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
thierry.poiroux@cea.fr

Guillaume Hubert
ONERA/DPHY, Univ.of Toulouse
Toulouse, France
guillaume.hubert@onera.fr

***Abstract*— Single Event Transients (SET) are important issues concerning reliability of CMOS circuits. They lead to occurrence of soft errors in integrated circuits, such as Single Event Upset (SEU) which consists in unexpected bit state switch in SRAM cells [1,2]. We can find models which describe SET in literature [1, 5] but they are not compact (i e. physical model implemented in Verilog-A). In previous work [6], we proposed a theoretical SET model but the implementation in Verilog-A was still challenging. Here, we describe the implementation in Verilog-A of this model and use it through standard SPICE simulations to study the effect of SET on SRAM cell and shift register.**

Keywords— SET, SEU, Radiation, Heavy ion, Compact model, SPICE, Bulk transistor

I. Introduction

The effect of natural radiations (neutrons, muons, protons, alpha particles due to material inherent radioactivity…) on CMOS circuits has been widely demonstrated over the last decades and these effects are even more significant as we decrease transistor sizes [1,2]. Single Event Transients (SET) are one of these effects and consist in the formation of parasitic current pulses within MOSFETs after the particle impact. These pulses are able to propagate through circuits leading to some errors in data treatment and storage. The physics of SET is highlighted in former work [6] where we proposed a theoretical SET model (validated by TCAD simulations) based on an infinite number of RC circuits. So, this model suffers from some limitations in Verilog-A implementation because it supposes an infinite number of internal nodes. In this paper, we propose a methodology to reduce the number of RC circuits without reducing the physical contain of the theoretical model. The resulting model, called "implemented model" in the following, is then used through standard SPICE simulations in order to study effects of SET on SRAM cell and shift register. In section II, we remind our theoretical SET model and we explain the RC

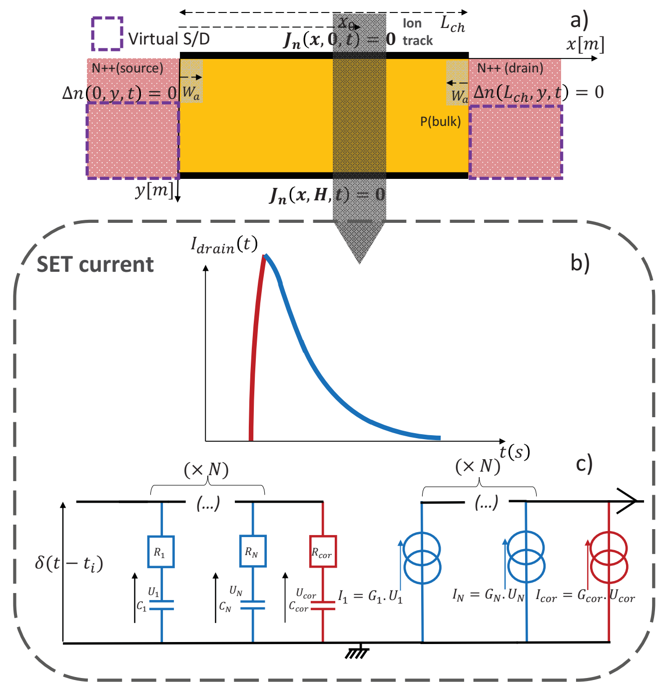

Fig. 1: a) physical system we consider. Note that we virtually extend Source/Drain junction vertically for modelling purpose as it does not impact the current calculation, as long as we consider vertical incidence only.b) typical shape of the SET current pulse. The red line is the rising part of the pulse while the blue line is the relaxation part.c) simplified equivalent circuit of SET phenomena. Particle impact is modelled as an impulsional voltage at the impact time. RC circuits, describing relaxation modes (blue) or corrective mode (red), are submitted to this voltage and control current generators which provide SET current pulse at the considered MOSFET electrode. G_k : conductance of kth mode (their expression depend on C_k expressions).

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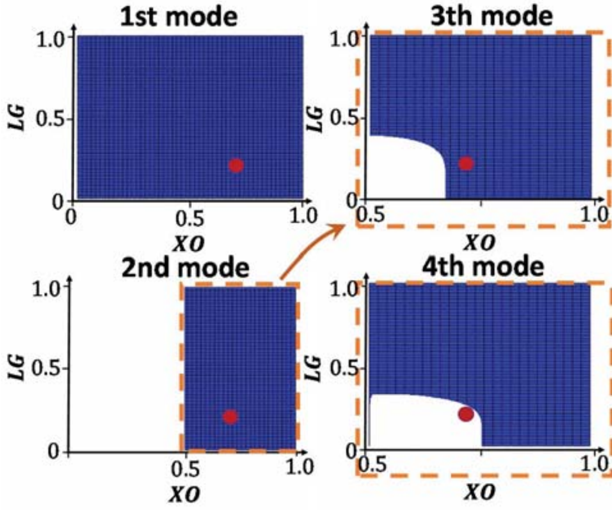

Fig. 2: analytical mapping of the sign of the diffusion modes. In blue color areas, the mode has positive values while it has negative values in white areas. The red dot represents one given set of values for particle parameters. For this set, we can deduce the first N modes which are positive until we reach a negative mode: they are the relaxation modes. In this example, the first negative mode is the 4th mode so we get $N = 3$.

elements number reduction based on physical arguments. Confrontations are made between theoretical and implemented models. Finally, in section III, we show how we can use the SET model to predict some well-known Single Event Effects (SEE) on SRAM cell and shift register.

II. From Theoretical to Implemented Model

A. *reminder of SET theoretical model*

The physical system we consider is depicted on Fig.1.a. As it has been explained in [6], the SET current pulse at one of the MOSFET electrode (for example the Drain) can be seen as the superposition of an infinite number of diffusion modes, linked to some time constants τ_k. Notice that such a result is valid as long as we consider absorbing boundary conditions at the PN junctions (Source/Bulk and Drain/Bulk). The current density expression at the electrode for a particle striking the device at $t = t_i$ (t_i=impact time of the particle) and with the gaussian generation rate described in [6] is then:

$$\boldsymbol{J_n}(t) = qN_d\mu_n.\left(\sum_{k=1}^{\infty} C_k e^{-\frac{(t-t_i)}{\tau_k}}\right).\boldsymbol{e_x} \tag{1.a}$$

$$C_k = \frac{(-1)^k LET\big(F_k(1) - F_k(0)\big)}{2\epsilon_{si}\pi k d}.\sin^2\left(\frac{k\pi WA}{2}\right) \tag{1.b}$$

$$F_k(X) = ie^{\frac{-\pi^2k^2LG^2}{4}}\left(\begin{array}{c} e^{-i\pi XOk}.\operatorname{erf}\left(\frac{X-XO}{LG} + i\frac{k\pi LG}{2}\right) \\ - e^{i\pi XOk}.\operatorname{erf}\left(\frac{X-XO}{LG} - i\frac{k\pi LG}{2}\right)\end{array}\right) \tag{1.c}$$

$$\tau_k = \frac{L_{ch}^2}{k^2\pi^2 D} \tag{1.d}$$

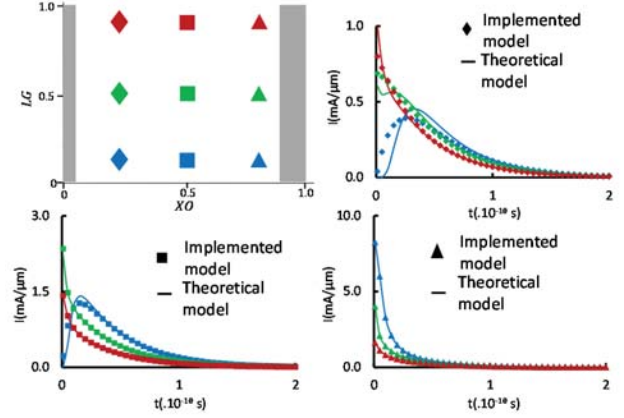

Fig. 3: For different sets of particle parameters values, we compare SET currents provided by theoretical and implemented model for $L_{ch} = 0.1\mu m$. We can see that there is a good matching between the 2 versions of the SET model, especially for the case $XO \to 1$. For a particle striking the MOSFET near the source, the matching is reduced but the temporal behavior is correctly conserved. Grey areas are out of the restricted range for XO.

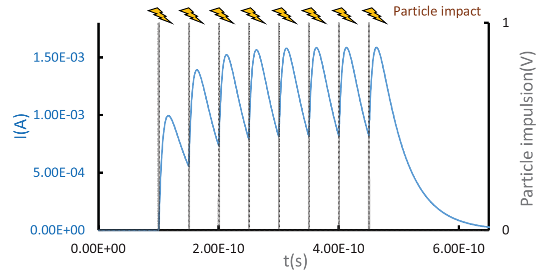

Fig. 4: impact of many identical particles at 2 different times for $L_{ch} = 0.1\mu m$. We show the drain current provided by the SPICE simulator and the input impulsional voltages describing the particles impacts. We see that the linearity of the equivalent circuit allows us to treat the incidence of many particles without creating a new circuit for each of them: the total SET current is the sum of the SET currents linked to each particles.

where q $[C]$ is the elementary charge, N_d $[m^{-3}]$ is the doping density in Source/Drain, μ_n $[m^2.s^{-1}.V^{-1}]$ is the electron mobility in Source/Drain, LET $[C.m^{-1}]$ is the Linear Energy Transfer, ϵ_{si} $[F.m^{-1}]$ is the silicon permitivity, d $[m]$ is the depth along z, $WA = W_a/L_{ch}$ is the reduced splitting width, $LG = L_g/L_{ch}$ is the reduced characteristic length of the gaussian generation, $XO = x_o/L_{ch}$ is the reduced gaussian center location, $X = x/L_{ch}$ is the reduced horizontal position, i is the imaginary number, and D $[m^2.s^{-1}]$ is the ambipolar diffusivity. Note that the expression of eq.(1.c) is real because imaginary number cancel out through the difference of imaginary error functions [7]. We can then deduce an equivalent electronical circuit made of an infinite number of RC circuits as explained in [6].

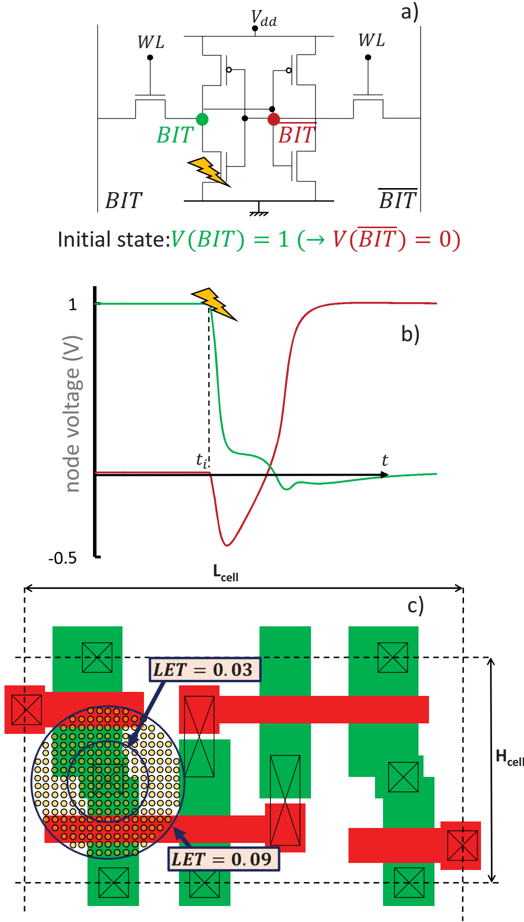

Fig.5: occurrence of SEU in a SRAM cell. a) SRAM schematic with highlight on struck MOSFET b) observation of the SEU: values of each floating node are switching just after striking of M1. Particle parameters are chosen so that we are at the limit SEU/no SEU. c) layout we consider for the SRAM cell. We map the SEU sensitive areas (blue circles) around the NMOSFET predicted by the proposed model for 2 different LET, keeping LG and D constant.

B. *Implemented model*

We now have to make the SET model suitable for Verilog-A implementation through reduction of the number of internal nodes. The idea is to keep all diffusion modes dealing with the relaxation part of the SET current pulse (blue line on Fig.1-b) and add a corrective function in order to describe the rising part (red line). This last function is a decreasing exponential with parameters $(\tau_{cor} > 0, C_{cor})$ in analogy with diffusion modes parameters (τ_k, C_k). Notice that this form for the corrective function is an approximation which is still able to catch the behavior of the rising part of the current pulse. It also allows us to recover the RC circuit formalism [6]. We denote N for the number of relaxation modes which can be formally defined as the first N positive modes, namely verifying, $C_k > 0$, the higher positive modes actually adjusting the behavior of the rising part of the pulse in theoretical model. As a result, the SET implemented model is given through:

$$J_{n,imp}(t) = qN_d\mu_n\left(\sum_{k=1}^{N} C_k e^{-\frac{(t-t_i)}{\tau_k}} + C_{cor}e^{-\frac{(t-t_i)}{\tau_{cor}}}\right) \quad (2)$$

Consequently, we obtain the simplified equivalent electronical circuit illustrated on Fig.1.c, made of N RC circuits dealing with current relaxation and one RC circuit which approximates the rising part of the pulse (they respectively correspond to blue and red components on Fig.1.c). We need now to find the 3 unknown parameters C_{cor}, τ_{cor} and N.

The SET current shape around the impact time and the collected charge $Q_c = \int_{t_i}^{\infty} J_n(t)dt$ (in $C.m^{-2}$) are important features for SEE studies. So, we have to guarantee that theses quantities are conserved between theoretical and implemented model. Thus, for determination of (C_{cor}, τ_{cor}), we first impose implemented (eq. (2)) & theoretical (eq. (1.a-d)) currents at the impact time to be equal. It results in the following equation:

$$C_{cor} = \frac{J_n(t_i)}{qN_d\mu_n} - \sum_{k=1}^{N} C_k \quad (3)$$

We also impose the implemented & theoretical collected charges to be equal. We obtain another relation:

$$\tau_{cor} = \frac{\frac{Q_c}{qN_d\mu_n} - \sum_{k=1}^{N} C_k\tau_k}{\frac{J_n(t_i)}{qN_d\mu_n} - \sum_{k=1}^{N} C_k} \quad (4)$$

If we restrict the range of XO to $XO \in [0.01, 0.91]$ (which covers most of the cases of particle incidence location in active zone), we guarantee that the series Q_c converges with a reasonable number (maximum 100) of iterations. For this range, if $LG \leq 0.3$, the series $J_n(t_i)$can be predicted to be egal to 0 and otherwise, $J_n(t_i)$ converges also with a maximum of 100 iterations. Notice that this methodology is valid only for $L_{ch} > 10\ nm$.

The second step is to be able to predict the number N of relaxation modes for a particle defined by XO, LG, LET. From eq.(1.a-c), the sign of one mode k is determined by the reduced variables XO and LG (as $\sin^2(k\pi WA/2)$ is always positive). Fig.2 shows one example of sign analysis plotting eq.(1-b) in the (XO, LG) plane: we begin with the first mode $k = 1$ (which is always the slower relaxation mode), and we then verify the sign of each following modes to deduce the number N. In an implementation point of view, we just have to define a "while loop" in the code. This method allows us to adjust the number of internal node related to relaxation according to particle parameters values (XO, LG) without reducing the accuracy of the model in describing this relaxation. We can then inject the value of N in eq.(3-4) and the corrective mode is fully determined.

Notice that we have to define a maximal number of internal node dealing with relaxation and we can show that this choice is directly linked to the range of XO we have chosen for (τ_{cor}, C_{cor}) determination. If we obtain $\tau_{cor} < 0$, we reach the limit of the implementation method: in these cases the form of the corrective function is not able to fit with the collected charge

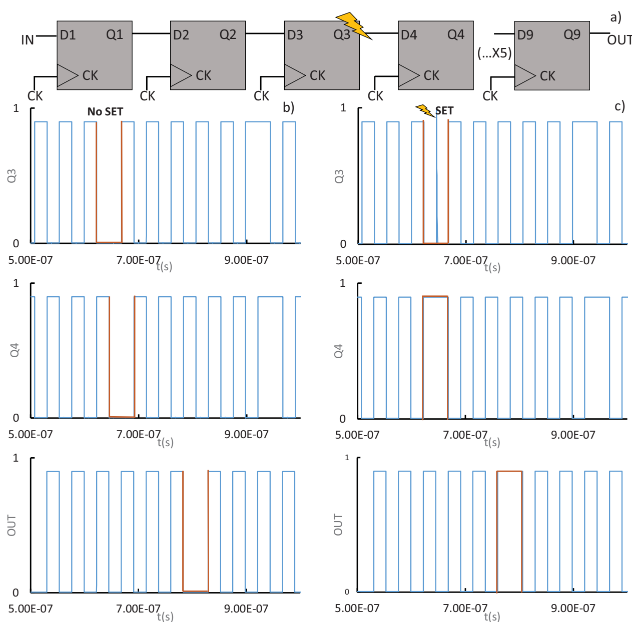

Fig. 6: chronograms of a shift register. a) Schematic and particle impact location during clock rising. b) observed pattern without SET at 2 successive Flip-Flops and at the output. c) same pattern with SET in Q3: we notice occurrence of a glitch which induces changes in subsequent Flip Flops as it is evidenced by orange lines.

condition because of the complicated shape of the rising part of the pulse. However, in these specific cases the total current pulse can be approximated by the N relaxation modes (so the series term in eq.(2)) without inducing significant errors.

Comparison between theoretical and implemented currents are provided on Fig.3. We notice good matching between the 2 versions of the SET model, especially for the case $XO \rightarrow 0.91$. For a particle striking the MOSFET near the source, the matching is reduced but the temporal behavior is correctly conserved. We also notice better agreement for $LG \rightarrow 1$. One of the main pros of this implemented model is that we can consider the same equivalent circuit for one or several particle impacts thanks to the circuit linearity as evidenced on Fig.4: we just need to define an impulsional voltage pattern (one voltage peak at each impact time) for each kind of particles defined by (XO, LG, LET) and the output current will be the sum of each single particle current pulse.

III. Proof of Concept on Elementary Circuits:

A. *SRAM*

The proposed model predicts some well-known SEE at the circuit level. One of them is SEU, which is the bit switch of a SRAM cell following the impact of the particle (Fig.5.a). So, we used the SRAM bit cell and associated MASTAR.VA model cards of BULK MOSFETs (representative of 20nm node $L_{ch} = 20\ nm$) proposed in [8]. We initialized the bit state and we analyzed the influence of particle striking during holding on one of the sensitive MOSFETs [1]. Fig.5.b illustrates chronograms of both floating nodes voltages BIT and $\overline{BIT}$ during holding time; we clearly see the bit inversion after the particle impact (if we choose proper particle parameters).

It is actually important to study the probability of SEU occurrence, dressing a mapping of sensitive areas of the SRAM in a given radiative environment. To do so, we discretize the SRAM cell surface through elementary surfaces and make particles strike the cell on each ones. We also calculate a shape factor which allows us to adapt the proposed SET model to full 3D gaussian generation. We then check whether or not we get SEU. As explained in Section. I, we need 2 electrodes in order to get the series formalism of eq.(1.a) (so far, we have considered the Source and Drain of the same MOSFET). It is no longer valid if we consider particle incidence outside the channel of SRAM cell MOSFETs. So, we choose the first electrode to be the one where we want to calculate the SET current and the second one is a virtual electrode located far from the particle location so that $XO \rightarrow 0.91$. In that way, we minimize the effect of this virtual contact while the value of XO still fit with the range we defined in Section II. On Fig.5.c, we show the resulting sensitive areas mapping for two realistic LET values and considering a basic particle environment (ie: constant LG, D and only vertical incidence on the half of SRAM cell). Notice that the proposed study is illustrative, we have not taken Shallow Trench Insulator (STI) into account as suggested in [3].

B. *Shift register*

Another important issue for reliability of ICs are glitches in shift registers, following particle strikes in Flip-Flops [1]. For a shift register (cf Fig.6.a using also MASTAR VA model) working as a delay circuit (series inputs, parallel outputs), the parallel outputs voltages can suffer from an extra shift in time due to particle strike on one of the Flip-Flops. This phenomenon can be predicted by our model as illustrated on chronograms of Fig.6.b & 6.c. Consequently, these proofs of concept show some practical uses of the model but a more complete work including a realistic radiative environment and all possible incidence orientations remain necessary.

IV. Conclusion

In this paper, we proposed an implementation method of the SET theoretical model of former work [6]. It resulted in a Verilog-A code which is based on a finite number of RC circuits and which is physical. The input of the model are particles parameters (XO, LG, LET), the ambipolar diffusivity D, the splitting width W_a and impact times voltage pattern and the output is the SET current. Such a formalism makes the SET model suitable for SPICE simulations and we showed some useful SPICE applications.

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