New physical insight for analog application in PSP bulk compact model

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***Abstract*— With the maturity of CMOS technologies and their use for low voltage analog applications, some additional parasitic effects must be modeled to improve again the accuracy of SPICE models. Indeed, with the decrease of supply voltage, devices operate close to the weak inversion, where some effects such as parasitic sidewall transistor, also called hump effect [1], and the interface states effect [2], can have a significant impact on the model accuracy. This paper describes the latest significant improvements of PSP model related to version 103.6 including new compact models of parasitic MOSFET and interface states. The major challenge is to provide accurate solutions with a low impact on CPU times for large analog circuit designs. The model extensions are validated against Silicon experiments from devices with channel length down to 40nm, and including low voltage and body bias operation.**

Keywords*— *PSP, compact model, SPICE, Bulk transistor.

I. INTRODUCTION

PSP is a standard compact model for deep-submicron bulk Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). This SPICE model, used in semiconductor industry, is a standard model [3] and available in most commercial simulators. The PSP model is surface-potential based and contains all relevant physical effects such as mobility degradation, velocity saturation, short channel effects, gate currents, lateral doping gradient effects, STI induced stress effects, etc [4]. PSP not only gives an accurate description of currents, charges, and their first order derivatives (i.e. transconductance, conductance and capacitances), but also of the higher order derivatives, resulting in an accurate description of electrical distortion behavior. The latter is especially important for analog and RF circuit designs. Since 2015, CEA-LETI is the main developer of PSP [5].

In this paper, we present new physical insights included in PSP 103.4 to 103.6 version [5]. In Section II, we focus on modeling of the edge transistor including a run time study and, in section III, we describe an innovative solution to capture the g_m/I_D curve through non-uniform Distribution of Interface States (DIT).

II. COMPACT MODELING OF HUMP-EFFECT: FAST CHARGE CALCULATION

A. Model concept

The parasitic transistor effect is related to the specific conduction conditions in the channel region close to the sidewall isolation. For the implementation of the hump effect, it is particularly challenging to keep accuracy with low CPU time impact. For that, we propose a fast calculation of the charge, coupled with a current formulation including main physical MOSFET parameters such as mobility, electrostatic and a dedicated substrate doping dependence parameter to provide sufficient flexibility during the parameter extraction. Note that to model the hump effect in subthreshold slope, the accumulation regime is not relevant. A simplified analytical resolution of surface potential is carried out where only free minority carriers are taken into account:

$$\left(x_g - x\right)^2 = G^2.e^{x-xth} \qquad (1)$$

Considering a threshold voltage approach including channel voltage (x_{th}):

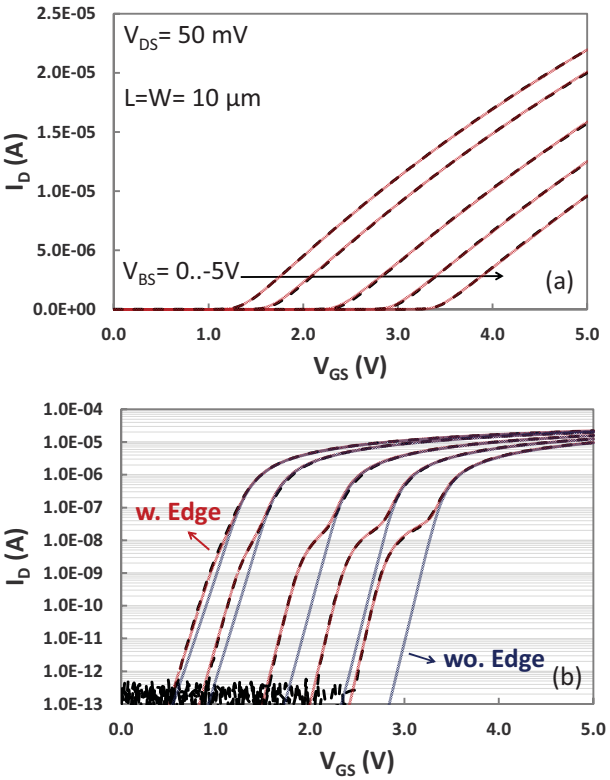

Fig. 1: Comparison between experiments (dotted line) and model (red line with and blue line without edge model) for W=10 µm & L=10 µm: linear current (I_D) in lin scale (a) and log scale (b) versus V_{GS}.

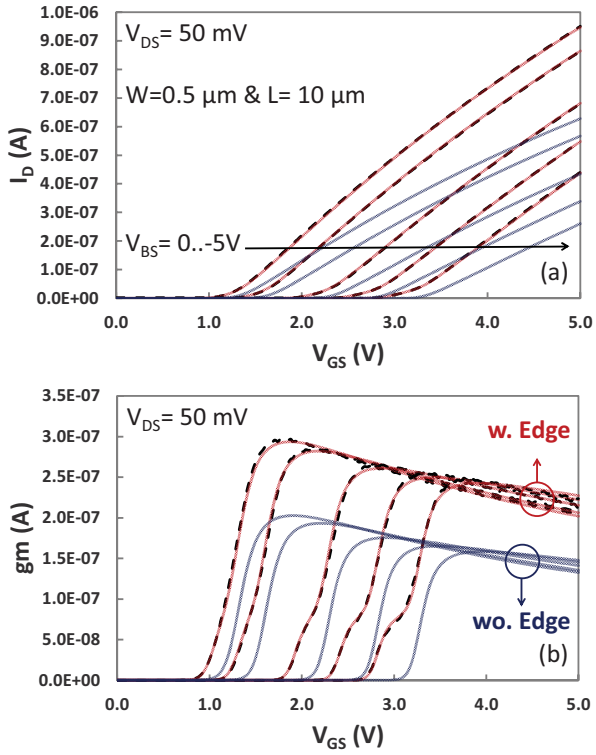

Fig. 2: Comparison between experiments (dotted line) and model (red line with and blue line without edge model) for W=0.5 µm & L=10 µm: linear current (I_D) (a) and first current derivative (gm) (b) versus V_{GS}.

$$x_{th} = x_{sth} + G \cdot \sqrt{x_{sth}} + dx_{th0} \quad (2.a)$$

$$x_{sth} = 2 \cdot ln(N_a/n_i) + x_n \quad (2.b)$$

$$G = \sqrt{2 \cdot q \cdot N_a \cdot \varepsilon_{Si}/\phi_T \cdot C_{ox}{}^2} \quad (2.c)$$

where q is the electron charge; C_{ox} is oxide capacitance; N_a is the channel doping; n_i is the intrinsic concentration; x is reduced surface (index s), gate (index g) or bulk (index b) potential; ϕ_T thermal voltage; ϕ_b is the bulk potential, x_n is the reduced quasi-fermi potential. Then, the drain current is calculated using inversion charge at source and drain sides by:

$$I_{ds,edge} = -BETNEDGE \cdot \phi_T{}^2 \cdot G_{mob}{}^{-1} \cdot (\alpha_{bm} \cdot q_{im} + 1) \cdot q_{ids} \quad (3.a)$$

where $q_{im} = (q_{id} + q_{is})/2$; $q_{ids} = q_{id} - q_{is}$; q_{is} and q_{id} are related respectively to source and drain charge; G_{mob} is the mobility dependence at high electrical field coming from the main transistor . Related parameters to this parasitic transistor are summarized in table I.

TABLE I. EDGE TRANSISTOR PARAMETER

Parameter	*Unit*	*Comment*
SWEDGE	-	Flag for drain current of edge transistors
VFBEDGE	V	Flat band voltage shift at TR
CTEDGE	-	Interface states
DPHIBEDGE	V	Offset parameter for ϕ_b
NEFFEDGE	m^{-3}	Effective substrate doping
BETNEDGE	$m^2/V/s$	Channel aspect ratio times zero-field mobility per side
PSCEEDGE	-	Subthreshold slope coefficient
PSCEBEDGE	V^{-1}	Bulk voltage dependence of subthreshold slope coefficient
PSCEDEDGE	V^{-1}	Drain voltage dependence of subthreshold slope coefficient
CFEDGE	-	DIBL parameter
CFDEDGE	V	Drain voltage dependence of DIBL
CFBEDGE	V^{-1}	Bulk voltage dependence of DIBL
STVFBEDGE	V/K	Temperature dependence of VFBEDGE
STBETEDGE	-	Temperature dependence of BETNEDGE

B. Confrontation with experiment and run time evaluation

Fig. 1-2 represents different figures of merit on current and g_m versus gate voltage for different values of back gate voltage and two geometries (large W=L= 10µm and narrow W=0.5 µm L=10 µm transistor). The hump induced by the parasitic transistor is well reproduced by the proposed model even for narrow transistor, where the parasitic transistor is predominant on total current as highlighted on gm of figure 2.b.

Due to duplication of parameters (main and edge transistor), the parameter extraction is impacted. For example, for a long channel, the subthreshold regime is usually model by extraction of electrostatic parameters such as flat band voltage, interface state factor and effective doping. Introducing the edge transistor, we must extract VFBEDGE, CTEDGE and BETNEDGE on the same region to capture the shape. Add to that the effect of effective doping NEFFEDGE, extraction strategy becomes challenging even if we keep similar philosophy.

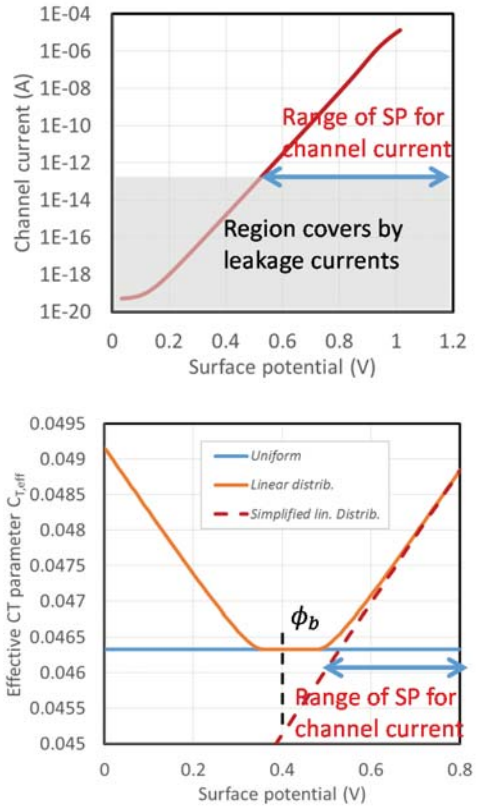

Fig. 3: Schematic view of current and pseudo calculation of $C_{T,eff}$ versus surface potential (SP). Illustration of most important region (weak inversion) where the simplification of $C_{T,eff}$ calculation is realized.

To evaluate the impact of this new model on the run time, a native model implementation in different Spice simulators is used (so, not using a Verilog-A code). Different test cases are considered: 1 model instance without edge transistor as reference, 2 model instances using PSP model (1 for main transistor and 1 for edge transistor) and 1 model instance with this new edge model. Table II summarizes the results and shows clearly the benefit to use a fast charge calculation included in core model on 3 different SPICE simulators. Compared with the use of 2 model instances, this new version of PSP reduces drastically the run times (between 25 and 30%).

TABLE II. RUN TIME EVALUATION

Simulator	*A*	*B*	*C*
2 instance of PSP 103.3 model is used (1 main & 1 for edge)	+56%	+64%	+50%
1 instance of PSP 103.4 using proposed edge model	+9%	+19%	+13%
Run time Improvement	**-30%**	**-27%**	**-25%**

III. GM/ID IMPROVEMENT: INTRODUCTION OF NON-UNIFORM DISTRIBUTION OF INTERFACE STATE (DIT)

A. Model foundation

From a deep investigation on different experimental data, it turns out that g_m/I_D in weak and moderate inversion suffers lack

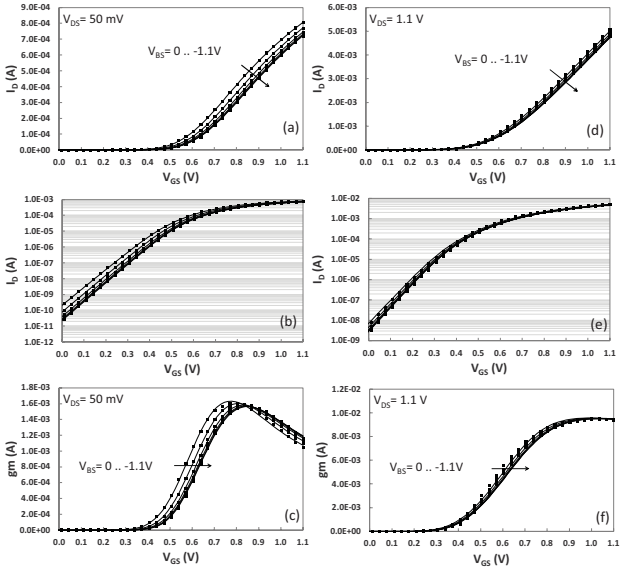

Fig. 4: Comparison between experiments (symbol) and model (line): linear current (I_D) in linear (a) and logarithmic (b) scale, transconductance (g_m) (c), saturated I_D on linear (d) and logarithmic (e) scale, saturate g_m (f) versus V_{GS} for different V_{BS}.

of accuracy where the g_m/I_D in PSP is relatively smooth compared to experimental data. Theoretically, in weak inversion the g_m/I_D should increase when the gate voltage increases due to the reduction of depletion capacitance. Nevertheless, a possible origin of the discrepancy observed on g_m/I_D characteristic in weak inversion could come from a voltage dependence of interface state capacitance, as already introduced in reference [6]. In the field of total ionizing dose, a work from S. Esqueda *et al.* [7] proposed an analytical surface potential based solution to take into account influence of non-uniform DIT in bulk compact model view.

In the classical case, the uniform DIT is described through the charge induced $Q_{it} = q \cdot N_{it}$ by DIT [2] and the total semiconductor charge:

$$N_{it} = \int_{-\phi_b}^{\psi_s} D_{it}(\psi_s)\, d\psi_s = D_{it0} \cdot (\psi_s - \phi_b - \phi_n) \qquad (4.a)$$

$$Q_{sc} = C_{ox} \cdot \Phi_T \cdot \left(x_g - x - CT \cdot (x - x_b - x_n)\right) \qquad (4.b)$$

To model this uniform DIT, a parameter $CT = q.D_{it0}/C_{ox}$, called "interface states factor", was introduced in PSP (which is classically used to mimic the non-ideal subthreshold slope of long channel transistors). Following the approach proposed in reference [7] for non-uniform DIT, we supposed here only linear distribution as described by:

$$N_{it}(\psi_s) = a \cdot (\psi'_s - \phi_{it})^2 + D_{it0} \cdot (\psi_s - \phi_b) \qquad (5)$$

where $a = (D_{it1} - D_{it0})/(2 \cdot E_1)$, $\psi'_s = max(|\psi_s - \phi_b|, \phi_{it})$, $\phi_{it} = (E_g - E_1)/2$ and D_{it1}, D_{it0}, E_1 are parameters related to non-uniform DIT. To simplify the calculation/implementation in PSP model, we define $C_{T,eff}$ through:

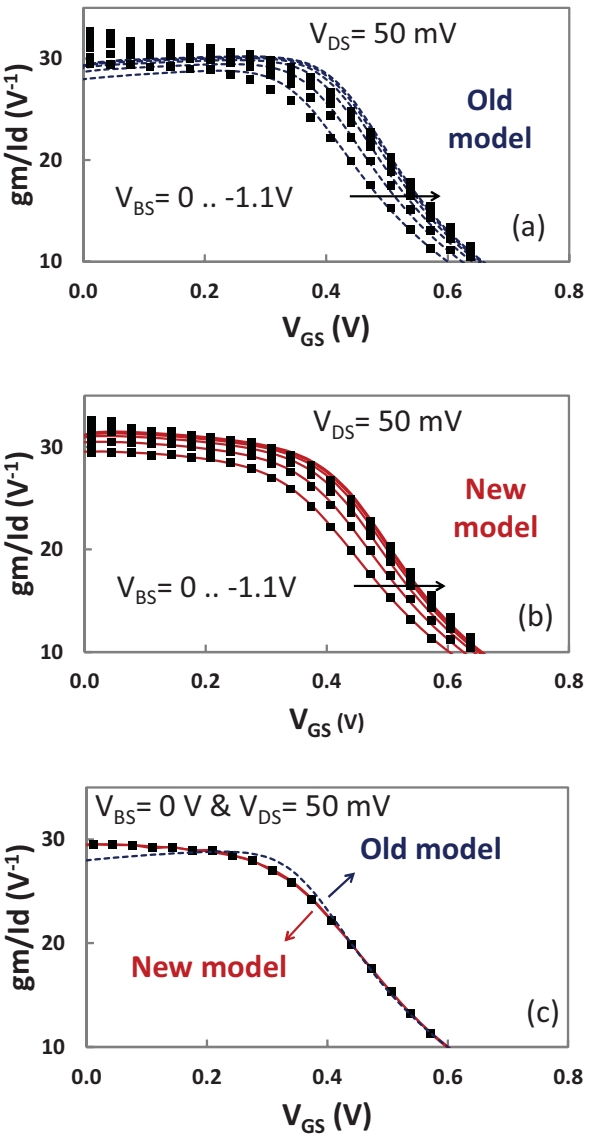

Fig. 5: Comparison between experiments (symbol) and model (line): (a) gm/Id versus V_{GS} without CTG & CTB, (b) g_m/I_D versus V_{GS} with CTG & CTB effect and (c) comparison with & without non uniform DIT model.

$$C_{T,eff} = q.N_{it}/\left(C_{ox}\cdot(\psi_s - \phi_b)\right) \quad (6)$$

By replacing CT in the surface potential calculation and avoiding negative value on $C_{T,eff}$ calculation versus the surface potential value (as illustrated on figure 3). We obtain after some algebra a new model:

$$C_{T,eff}(\psi_s) = CT\cdot e^{\left(CTG\cdot\frac{T_{KD}}{T_{KR}}\cdot\left(\frac{\psi_s}{\phi_T}-(1+CTB)\cdot\frac{\phi_b}{\phi_T}\right)\right)} \quad (7)$$

where $CTG = \Phi_{T,R}(D_{it1} - D_{it0})/(D_{it0}.E_1)$ are the gate voltage dependence parameter, $CTB = (\phi_{it}/\phi_b)\left(2 - (\phi_{it}/\phi_b)\right)$ are the bulk voltage dependence parameter, T_{KD} and T_{KR} are reference temperature and device temperature (respectively) and $\Phi_{T,R}$ is the thermal voltage at T_{KR}.

B. Confrontation with experiment

The influence of non-uniform related DIT parameter is relatively slight on classical figures of merit as represented in Fig. 4 where we plot current and g_m for the considered geometry (W=10 µm & L=0.04 µm) of bulk technologies. On the other hand, in figure 5.a, we observe clearly the lack of accuracy obtain by using only uniform DIT and the good agreement using this new model of non-uniform DIT particularly evident on g_m/I_D curves. As illustrated on Fig. 5.a, Fig. 5.b (for both V_{GS} and V_{BS} impact) and Fig.5.c (for V_{GS} only), our solution is able to capture the slight variation of experiment data.

The extraction strategy is not strongly impacted, by keeping the same strategy of extracting CT (uniform DIT part) on subthreshold on log-scale, and subsequently a fine-tuning CTG & CTB on the g_m/I_D figure of merit, which exhibits the non-uniform DIT part. Note that g_m/I_D is one of the key figures of merit in analog design.

IV. Conclusion

In this paper, we present recent PSP improvements based on experimental data following our collaboration with STMicroelectronics and NXP. The model and its implementation is available in all major commercial SPICE simulators. Note also, Verilog-A code and its associated document including all equations are available on the PSP official website [5].

References

[1] Y. Joly, L. Lopez, J-M. Portal, H. Aziza, Y. Bert, F. Julien and P. Fornara, "Impact of Hump Effect on MOSFET Mismatch in the Sub-threshold Area for Low Power Analog Applications", IEEE International Conference on Solid-State and Integrated Circuit Technology, 2010.

[2] I. Sanchez Esqueda, H. J. Barnaby, and M. P. King, "Compact Modeling of Total Ionizing Dose and Aging Effects in MOS Technologies", IEEE Transactions on Nuclear Science Volume: 62, Issue: 4, Aug. 2015.

[3] Compact Model Coalition for standardization of SPICE models: http://www.si2.org/cmc/

[4] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, Geert D. J. Smit, Andries J. Scholten, and Dirk B. M. Klaassen, "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation", IEEE Transactions on electron Devices, vol. 53, no. 9, sept. 2006.

[5] PSP 103.6 Verilog-A and documentation. http://www.cea.fr/cea-tech/leti/pspsupport.

[6] D. K. Schroder, "Defect in Microelectronics Materials and Devices" (CRC Press 2008).

[7] I.S.Esqueda, Hugh J.Barnaby, "Modeling the Non-Uniform Distribution of Radiation-Induced Interface Traps" IEEE Transactions on Nuclear Science., Vol.59 ,N°4, p. 723-727, 2012.