N7 FinFET Self-Aligned Quadruple Patterning Modeling

Sylvain Baudot[1], Sofiane Guissi[2], Alexey P. Milenin[1], Joseph Ervin[2], Tom Schram[1]
[1]IMEC, Kapeldreef 75, 3001 Leuven, Belgium, sylvain.baudot@imec.be
[2] COVENTOR, 3 avenue du Quebec, 91140 Villebon sur Yvette, France, sguissi@coventor.com

***Abstract*— In this paper, we model fin pitch walk based on a process flow simulation using the Coventor SEMulator3D virtual platform. A taper angle of the fin core is introduced into the model to provide good agreement with silicon data. The impact on various Self-Aligned Quadruple Patterning process steps is assessed. Etch sensitivity to pattern density is reproduced in the model and provides insight on the effect of fin height variability.**

Keywords— FinFET, Pitch Walk, Modeling, Process Simulation

I. Introduction

Advanced FinFET technologies use Self-Aligned Quadruple Patterning (SAQP) to define features below the resolution of 193nm immersion lithography techniques [1]. For the 7nm FinFET node, a 24nm fin pitch is targeted which requires careful adjustment of SAQP parameters to avoid a systematic pitch variation (pitch walk). Unbalanced spaces between fins lead to undesired variability for subsequent etch or deposition steps. In this paper we propose a method to characterize the fin pitch walk by modeling the SAQP process flow of a 7nm FinFET technology with SEMulator3D® [2]. Our goal is to minimize the pitch walk and characterize the impact on fin height variability. In Part II, we present the process flow simulation and characterization methodology, as well as the critical parameters impacting the pitch walk. The model is applied in Part III(A) to optimize the fin pitch walk assuming an ideal core profile. The impact of a tapered profile on pitch walk is studied in Part III(B) and benchmarked against silicon data. A pattern dependent etch is introduced in Part III(C) to simulate fin height variability and characterize the consequences of pitch walk.

II. Methodology

The Coventor SEMulator3D® modeling and analysis platform is used for fast and accurate 'virtual fabrication' of advanced manufacturing processes. A conventional SAQP process flow is simulated using Coventor SEMulator3D® and described in Fig. 1. Carbon core lines are patterned with a 96nm pitch. An oxide spacer (spacer1) is deposited conformally and etched, before the initial core is chemically removed. The remaining spacer acts as a hardmask for the dry etching step of the underlying amorphous silicon layer (core 1). This process doubles the initial pitch from 96 to 48nm. A spacer2 oxide is deposited and etched similarly to obtain the desired 24nm pitch on the amorphous silicon (core 2). The pattern is transferred into the silicon substrate, leaving the silicon nitride hardmask on top of the fins to enable further integration of Shallow Trench Isolation (STI) oxide, not shown here.

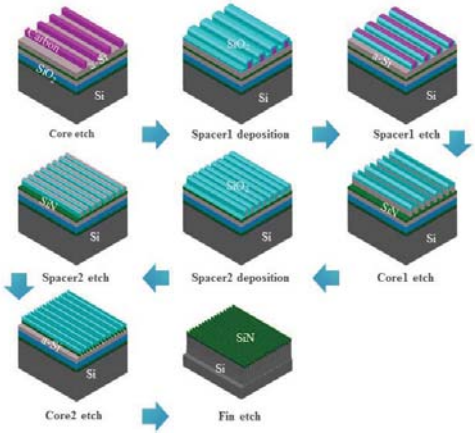

Fig. 1. Process Flow of SAQP Fin Patterning.

From Fig. 2 we can establish a graphical link between the cross sections obtained with our model after the spacer1 & spacer2 etch steps and the final structure.

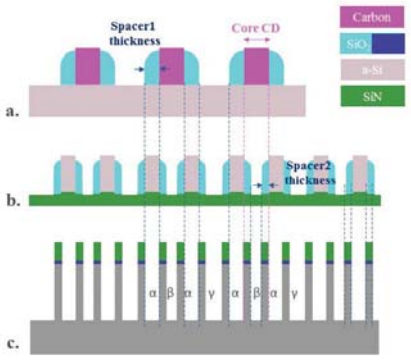

Fig. 2. Cross-section of (a) spacer1 etch, (b) spacer2 etch, (c) fin etch. Definition of α, β, γ spaces between fins.

The main parameters controlling the spaces between fins are the spacer1 and spacer2 thicknesses (Sp1_Thk and Sp2_Thk), the core line critical dimension (Core_CD) and its pitch (Core_Pitch). A non-ideal core profile is also known to impact pitch walk [3] and it will be studied in Part III(B). The combination of those dimensions lead to 3 different fin spaces labelled α, β, γ. Assuming conformal spacer depositions, we can describe those parameters using the following analytical equations:

$$\alpha = Sp1\_Thk \quad (1)$$

$$\beta = Core\_CD - 2.Sp1\_Thk \quad (2)$$

$$\gamma = Core\_Pitch - 2Core\_CD - 2Sp1\_Thk - 2.Sp2\_Thk \quad (3)$$

The pitch walk is defined as the difference between the largest and smallest space between the fins :

$$Pitch\_walk = \max(\alpha, \beta, \gamma) - \min(\alpha, \beta, \gamma) \qquad (4)$$

The impact of the critical parameters listed above on pitch walk can be systematically characterized by performing a process sensitivity analysis using the Analytics module of SEMulator3D®. Parameters will be varied using a full factorial design of experiment. The software can directly and automatically measure the pitch walk. As illustrated in Fig. 3 the Extract Top-Down function saves the visible silicon surface in a new mask and the Via CD check function measures min/max CD from the new mask representing fin spaces. This enables a reliable measurement of fin pitch walk for any process variation simulated.

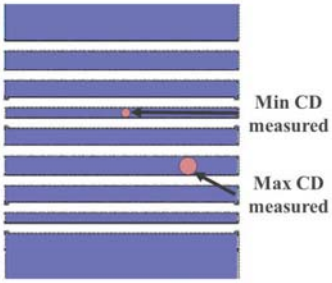

Fig. 3. Top down view of fin array, visible silicon area is colored in blue (fin spaces). Feature measured by *Via CD Check* highlighted.

III. Results & Discussion

A. Pitch walk optimization for ideal fin core profile

The model described earlier is applied to optimize the fin pitch walk assuming a straight fin core profile. The spacer1 and spacer2 thicknesses are varied around their target value by 25% and the core line CD by 2nm. The pitch walk obtained is depicted in Fig. 4 as a function of the SAQP parameter dimensions. For a core CD of 33nm the pitch walk is at a minimum for a spacer1 and spacer2 thicknesses of 15.0 and 9.25nm respectively (black triangle in Fig. 4). We noticed that for a spacer thickness variation of 1nm around its optimal value the pitch walk remains reasonably low. For a larger spacer thickness variation, the pitch walk is rapidly degraded to reach values above 14nm on the corners of the simulated values, corresponding to closed gaps between fins.

When reducing the Core CD from 33 to 31nm the pitch walk dependency to the spacer thicknesses is unchanged, but the optimum point is shifted. The optimal spacer1 thickness is 1.5nm larger (15.5 vs 17nm) and the spacer2 is at least 1nm lower – the optimum point is not found in the simulation space. For a core CD of 29nm the minimum pitch walk area is further shifted towards a larger spacer1, and a thinner spacer2. No pitch walk value below 2nm is found for this core CD, indicating a clear limitation of the spacer process window.

The values obtained from the SEMulator3D® model are compared to equations (1) to (3) in Fig. 5. The simulated results are in good agreement with the analytical model (correlation R^2=0.97). The maximum difference found is within 1nm corresponding to twice the model resolution used. A better accuracy has been obtained by reducing the model resolution. After this verification, the SEMulator3D® model was extended with non-ideal process assumptions, not taken into account in the analytical model.

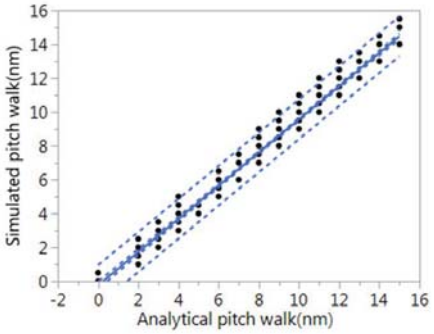

Fig. 5. Simulated pitch walk with SEMulator3D® model compared to analytical equations.

B. Core taper angle impact on pitch walk

Measurements obtained on 7nm FinFET silicon wafers at the end of the SAQP patterning are shown in Fig. 6 and compared with the simulated process using the same nominal Core CD, spacer1 and spacer2 thicknesses. The simulation shows a clear difference between two adjacent gaps corresponding to a pitch walk value of 14nm. The hardmask lines defined on silicon are regularly spaced, with a pitch walk value measured at 2.5nm. The process parameters used in this experiment are indicated in Fig. 4 with a star.

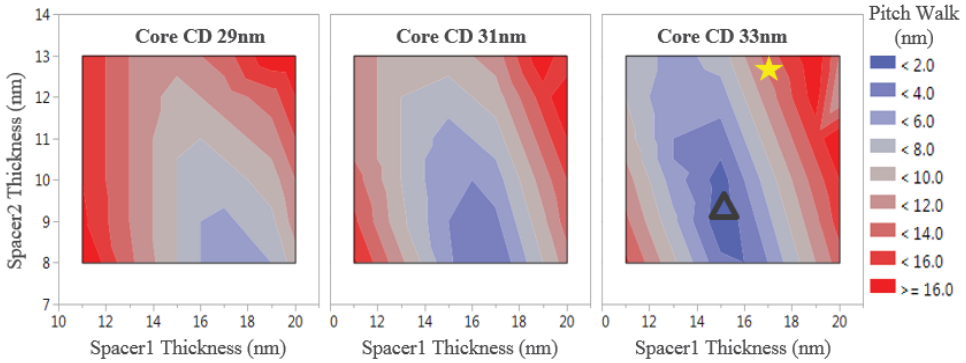

Fig. 4. Pitch walk calculated from analytical model as a function of spacer1 and spacer2 thicknesses for various core CD. Process condition used on silicon is marked with a star.

The large gap between this process condition and the minimum pitch walk displayed (black triangle in Fig. 4) highlights the discrepancy between the simulated results and the actual measurement.

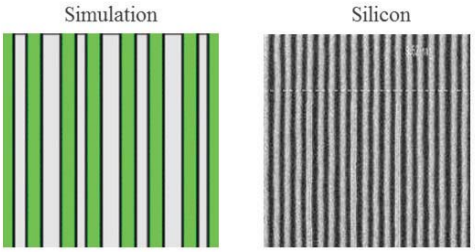

Fig. 6. Top down view of fins from simulation (left) compared to silicon (right) for 33nm Core CD, 17nm Spacer1 and 13nm Spacer2.

To obtain superior agreement with silicon, the model is compared to TEM cross-sections taken at different stages of the SAQP process. The initial core has a straight profile after etch and becomes tapered with an angle of 86 degrees after spacer deposition. Interaction of the oxide spacer deposition is known to degrade the amorphous carbon core profile [3]. This phenomenon can be modeled in SEMulator3D® by a taper angle during the core etch step. Fig. 7 shows the cross section of the different SAQP process step affected by a tapered core. For the simulated amorphous silicon core thickness, the taper angle leads to a 6nm difference between the top and bottom core CD. During spacer 1 etch, a TEM observation shows that the spacer oxide is partially consumed and its height is reduced. This effect is taken into account by adjusting the oxide etching selectivity in the model. The bottom spacer width is no longer equal to the deposited spacer thickness, contrary to the assumption made in the analytical model. A difference of 2.3nm is measured between the deposited spacer thickness and bottom CD on silicon, which is very well reproduced in our model.

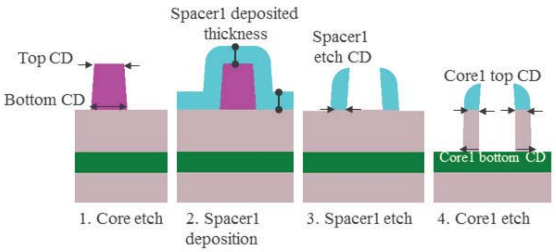

Fig. 7. Simulated impact of a 86 degrees core taper angle on subsequent process steps.

The pattern transfer to the amorphous core1 is also impacted by the non-ideal spacer1 shape. As a consequence, the oxide spacer CD is further reduced by 1nm, but the strong outward taper angle of the spacer is further transferred to the Core1 and cancels out the top CD reduction. A deposition-etch bias was also introduced similarly in the spacer2 etch step in order to reproduce the observations on silicon. The difference between the silicon results, the analytical model with a straight core, and the refined model with a tapered core are summarized in Table 1.

TABLE I. Summary of SAQP process parameters and associated fin spaces and pitch walk obtained from (a) silicon, (b) analytical model, (c) core taper angle model. *TEM measurement.

		Measurements on silicon	Analytical model	Core taper angle model
Process inputs	Core Pitch (nm)	96	96	96
	Core1 Top CD (nm)	33	33	29*
	Taper Angle (deg)	86*	90	86*
	Core1 Bottom CD (nm)	-	33	35.2*
	Sp1 THK (nm)	17	17	17
	Sp1 CD (nm)	14.7	17	14
	Sp2 THK (nm)	13	13	13
	Sp2 CD (nm)	10.3	13	10
Spaces between fins	Alpha (nm)	13.2	17	14
	Beta (nm)	15.7	7	15.2
	Gamma (nm)	15.1	3	12.8
Pitch walk (nm)		2.5	14	2.4

The initial core CD value of 33nm is based on the CDSEM measurement on silicon. It is an input for the analytical model, since the SEMulator3D® model takes input from the TEM for both top and bottom core CDs (resp. 29 and 35.2nm). The bias between the spacer deposition and etch described earlier leads to a significant difference in the alpha, beta and gamma spaces. The analytical model without bias gives a theoretical gamma space of 3nm, which translates in practice to a partial merging of the neighboring fins. The prediction for the refined model is much closer to the silicon results, within 15% of the actual measured values. The pitch walk provided by the model is more accurate, as it depends only upon the maximum gap width difference. The pitch walk obtained by the refined SEMulator3D® model is in good agreement, and resides within 5% of the measured values.

C. *Impact of pitch walk on fin height variability*

A reference TEM with a non-ideal pitch walk is shown in Fig. 8(a) at a later stage, when the fins are fully formed and a STI oxide is present between the fins. The total silicon fin height varies across the fin array within a 20nm range. The variation has a repeated pattern that has the same period as the SAQP process. Every 4 fins, a trench is significantly deeper and slightly larger than its neighbors. To establish a clear link between the fin height variation and the SAQP pitch walk, we first calibrate our model using the TEM picture 8(a) before characterizing the fin height as a function of pitch walk.

We introduced a predictive modeling approach for pattern-dependent etch processes that is available in the SEMulator3D® virtual fabrication software platform [4]. “Pattern dependence” refers to all types and sources of etch behavior which depends on pattern density, feature size, or aspect ratio. The pattern dependence modeling is based on 2D proximity functions, which can be easily calibrated to known structural data. These proximity functions are used to sample pattern-density within a characteristic distance of a point of interest on the mask. In our study, we introduced a pattern dependent etch to model the fin depth dependency to fin space and width across 16 fins. The resulting cross section is shown in Fig. 8(b) and accurately reproduces the periodical variations seen in the TEM.

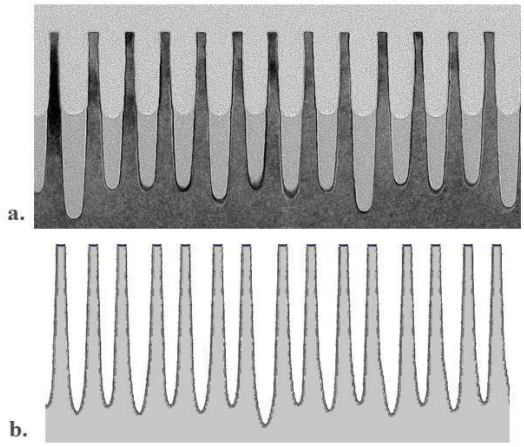

Fig. 8. (a) TEM of fin array after fin reveal.
(b) SEMulator3D® cross section using pattern dependent fin etch.

The fin height obtained from the model, as a function of top space, is compared to the values extracted from the TEM shown in Fig. 9. The experimental data show a linear dependency to the fin top space, with a significant dispersion of 5nm around the fitting line. This indicates that not only top space influences the fin height, but also other incoming variations which are not taken into account here.

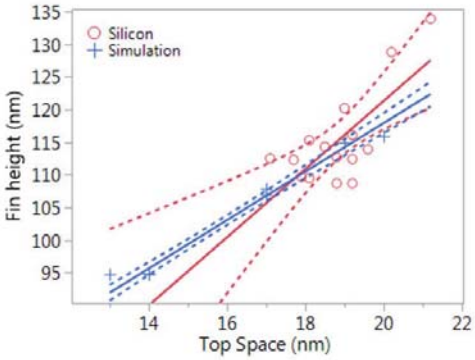

Fig. 9. Fin height variation as a function of top space for silicon (red) and simulation (blue).

The model accurately reproduces fin depth change between the range of 17 to 20nm top space. Outside this range, the experimental data are sparse and the linear fitting not accurate. The pattern dependent etch does not reproduce the measured abrupt fin depth variation. The simulated fin depth for 20nm top space remains in the linear trend, comparable to the majority of experimental points. More data with a broader range of top spaces would be necessary to calibrate the pattern dependent etch more accurately.

This model was used to assess the pitch walk impact on fin height variability. The core CD, spacer1 and 2 thicknesses are swept to simulate a fin array with a pitch walk varying from 3 to 13nm. The robustness of the model is evaluated through combinations of SAQP parameters giving the same pitch walk but different α, β, γ space values. The fin height non-uniformity across the simulated 16 fin array is normalized to the average fin height and reported in Fig. 10 as a function of fin pitch walk.

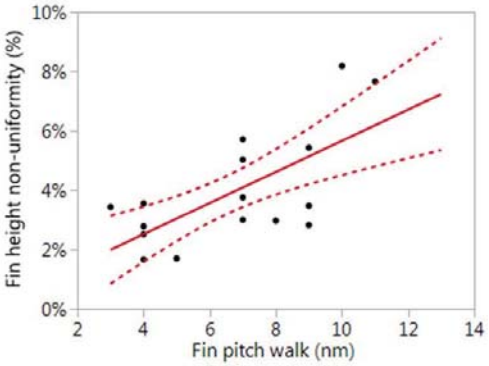

Fig. 10. Simulated impact of pitch walk on fin height variability using a pattern dependent etch model.

A strong correlation is evidenced between the fin non-uniformity and the fin pitch walk. The non-uniformity is as expected, worse when the pitch walk value increases, at a rate of 0.5%/nm. This confirms the importance of pitch walk as a key source of variability.

IV. CONCLUSION

In this study, we modeled the fin pitch walk on a 7nm FinFET technology node using the Coventor SEMulator3D® virtual fabrication platform. We proposed an optimization method to minimize pitch walk and the related process variability. We identified the spacer1 and spacer2 thicknesses, and the core line CD as key process parameters impacting pitch walk. The values obtained by our model are in a good agreement with the analytical equations describing pitch walk for an ideal SAQP process flow, but not completely in agreement with the silicon data. The core profile is tapered after spacer deposition, which impacts the line width and space after spacer1 etch and significantly degrades the pitch walk. By introducing a tapered core etch in our SEMulator3D® model, we obtained pitch walk values within 5% of the actual silicon values. In the last part of this study, we simulated a pattern dependent fin etch to reproduce fin height variability observed in silicon. The pitch walk is confirmed as a key source of variability, impacting the fin height non-uniformity by 0.5%/nm.

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