Technique for Asymmetric Source/Drain Resistance Extraction on a Single Gate Length MOSFET

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***Abstract*—A simple inline measurement technique for extracting the individual resistance components of the source, drain, and channel on a single MOSFET device using DC measurements is proposed. Modeling data is used to prove the efficacy of the technique. This method can be applied to symmetric or asymmetric devices.**

Keywords—parasitic resistance, device characterization

I. Introduction

The performance of MOSFET logic and memory devices is increasingly being limited by parasitic resistance and capacitance [1]. 40% or more of the total device resistance may be attributed to non-channel components, i.e. extension, source and drain spreading resistance, metal/source contact resistance and contact plug metal resistance [2]. It is important to be able to understand and measure the parasitic and channel resistance of MOSFETs. Common methods used to measure and separate out the extrinsic and intrinsic device resistances are shift and ratio [3], channel modulation method [2], R_{on} variation with changes in L_{gate}, or high frequency measurements [4].

Some of the limitations of these methods are that multiple gate length devices might be needed for extraction, or AC methods are required. These methods make the further assumption that the source and drain resistances are the same. Considering that shared source or drain causes inherent asymmetry in the extrinsic device resistance or that some of the options being considered for the technology node beyond 7nm are asymmetric gate-all-around devices [5,6], it is important to be able to extract the source, drain and channel components separately.

In this work, we present a simple technique to extract the source, drain, and channel resistance components on a single gate length device using DC measurements. The advantage of the technique is that it is fast and can be implemented as an in-line test. Section II describes the methodology and Section III shows the viability of the technique using simulation data from a contrived asymmetric structure. Section IV suggests other structures that can be analyzed with this technique and draws conclusions.

II. Extraction Technique

The 5 basic steps and assumptions are as follows:

- Measure forward saturated and linear I_d-V_g. Flip the source and drain contacts and measure the reverse I_d-V_g.
- Assume R_{source} and R_{drain} are independent of V_g.
- Assume $R_{channel}$ is linear with V_{od} (Q_{inv} α $(V_g$-$V_t)$; μ,V_{sat} ~constant).
- Extract $R_{channel}$ and $(R_s$+$R_d)$ from linear R_{on} vs $1/V_{od}$.
- Use saturated I_d-V_g to obtain $(R_d$-$R_s)$ via V_g difference at same I_d.

In the linear region, the on resistance can be written:

$$R_{on} = \frac{V_{ds}}{I_{ds}} = R_s + \frac{R'_{chan}}{\left(V_g - V_{tlin}\right)} + R_d$$

$(V_g - V_{tlin})$ is the overdrive voltage. The channel charge is assumed to be linear with the overdrive voltage. R'_{chan} represents the scattering limited channel mobility of the carriers and is assumed to be approximately constant. Plot the total R_{on} vs $(V_{od})^{-1}$ and the slope will be R'_{chan} with the intercept being $(R_s + R_d)$.

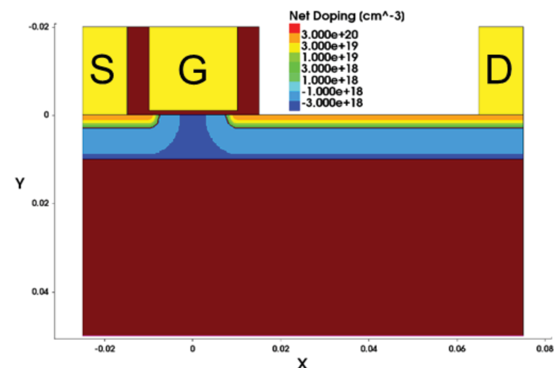

Figure 1. Simple Asymmetric MOSFET used in the study of source, drain and channel resistance extraction. For this device, Lg=20nm, EOT=1nm.

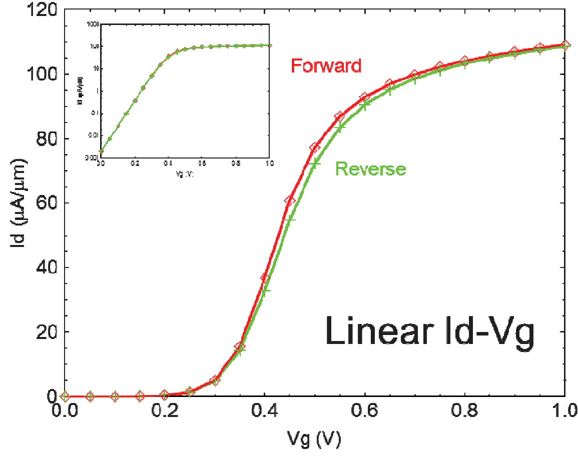

Figure 2. Linear I_d-V_g characteristics of the device in Figure 1 without additional lumped resistors.

In saturation,

$$I_{dfwd} = V_{sat}*C_{ox}*(V_{gfwd}-I_{dfwd}*R_s-V_{tsatfwd})$$

and

$$I_{drev} = V_{sat}*C_{ox}*(V_{grev}-I_{drev}*R_d-V_{tsatrev})$$

with "*fwd*" and "*rev*" implying conventional bias on the source/drain and reversing of the contacts. For short channel devices, we can safely assume that the device will be operating at nearly constant saturation velocity, so for a given fixed $I_{dfwd} = I_{drev} = I_d$, we should be at a fixed overdrive. This means that:

$$V_{gfwd}-I_{fwd}*R_s-V_{tsatfwd} = V_{grev}-I_{drev}*R_d-V_{tsatrev}$$

Rearrange to yield

$$(V_{gfwd} - V_{grev}) = I_d*(R_s - R_d) + (V_{tsatfwd} - V_{tsatrev})$$

For many such values of I_d, determine $(V_{gfwd} - V_{grev})$, and

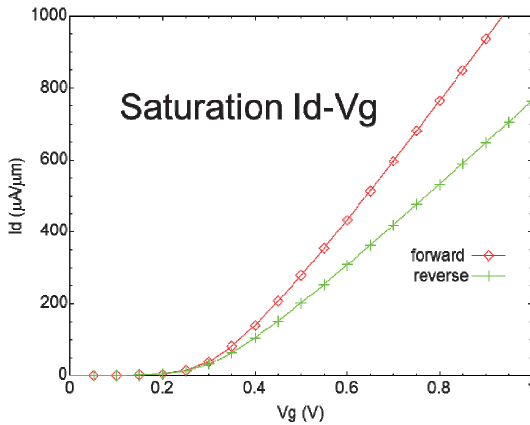

Figure 3. Saturated I_d-V_g characteristics of the device in Figure 1 without additional lumped resistors. At a fixed drain current, the gate overdrive for forward and reverse operation is the same, but the difference in applied gate bias is due to a voltage drop across the source resistance.

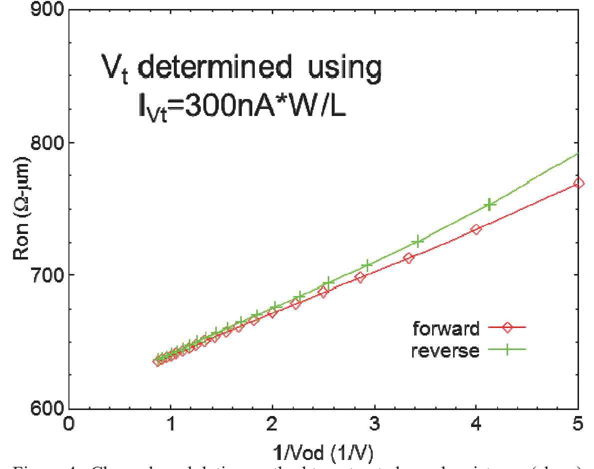

Figure 4. Channel modulation method to extract channel resistance (slope) and (R_s+R_d) (y-intercept). In this case, we determined the linear threshold voltage using a constant current method.

the slope of the resulting plot will be $(R_s - R_d)$. A non-zero value of the y-intercept for this line simply indicates that the V_t is different between the forward and reverse bias conditions. R_s and R_d can then be easily obtained along with the channel resistance.

III. Verification of the Technique

A simple asymmetric device was built and modeled using the Fielday device simulator [7,8] and a parameter set calibrated against short channel hardware. Figure 1 shows the structure studied. Asymmetry was built in to the device via a long diffusion on the drain side. In addition to the diffusion, 100 Ω–µm and 200 Ω–µm lumped resistors were added to the source and drain contacts to provide for more or less asymmetry. Figures 2 and 3 show the forward and reverse linear and saturated I_d-V_g characteristics of the contrived device. Figure 4 shows the linearity of the channel modulation method for extraction of R_{chan} and R_s+R_d under the assumption that the linear threshold voltage can be determined using the constant current criterion. Figure 5 shows the extraction of R_d-R_s from the difference in the forward and reverse saturation I_d-V_g characteristics. Table 1 summarizes the results. The results in Table 1 clearly show that the addition of resistance to the source or drain region increases the respective extracted R_s or R_d commensurately.

The Drift-Diffusion model does not inherently capture the effect of velocity overshoot nor ballistic transport well, so our assumption that the carriers will reach a nearly constant saturation velocity becomes a self-fulfilling prophecy using this model. We expect to see some fraction of the carriers experiencing ballistic transport in short channel devices, so we have used a high field transport solver based on the solution of the Boltzmann transport equation [9]. A 6nm×6nm square cross-section Si nanowire device of gate length, L_g=15nm with lumped resistors on the source and drain of *10kΩ* and *20kΩ* was modeled. Phonon and surface roughness scattering was included in these simulations. Figure 6 shows the I_d-V_g characteristics obtained from these simulations. The linear

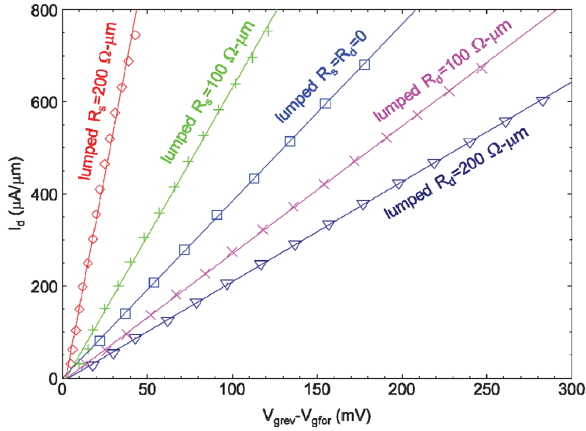

Figure 5. Extraction of (R_s-R_d) from the difference in the forward and reverse saturation I_d-V_g data. The separate lines in the above plot are for different cases for added lumped resistors on the source or drain.

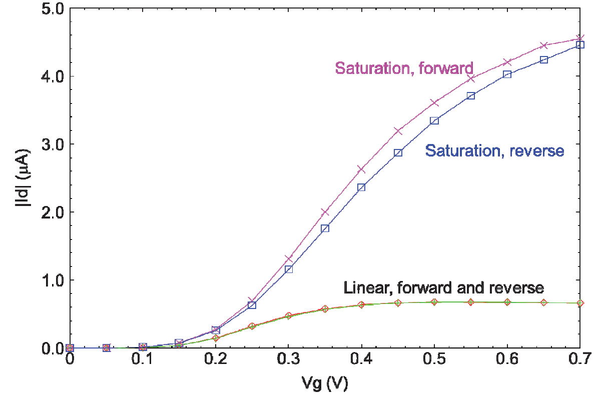

Figure 6. Simulation results of the linear and saturated I_d-V_g characteristics of a short channel (Lg=15nm) nanowire MOSFET using a BTE solver.

region at high overdrive is relatively flat, indicating a large external resistance. In saturation, the carriers showed ballistic transport, even at modest V_{ds}. Using the method described above, we obtain $(R_s + R_d) = 52.2k\Omega$, indicating the source and drain regions in the intrinsic device added $22.2k\Omega$ to the total device resistance. The difference in source/drain resistance was then extracted to be $(R_d - R_s) = 9.87k\Omega$. $9.87k\Omega$ agrees with the expected value of $10k\Omega$.

A final practical example of the usefulness of this technique is in analyzing the effect of a shared source (drain) of a 2-fin device, such as that shown in Figure 7. The asymmetry in this typical device configuration comes from the fact that although the source and drain regions have full contact areas, when both devices are in the ON state, twice the amount of current will flow through the source than each of the drains. The impact of a shared source can be determined. Assuming FinFET dimensions commensurate with a typical 7nm technology such as in [10], and continuing to use a Drift-Diffusion device model with a nominal MOS transport model, the additional source resistance adds approximately 13% to the total $(R_s + R_d)$.

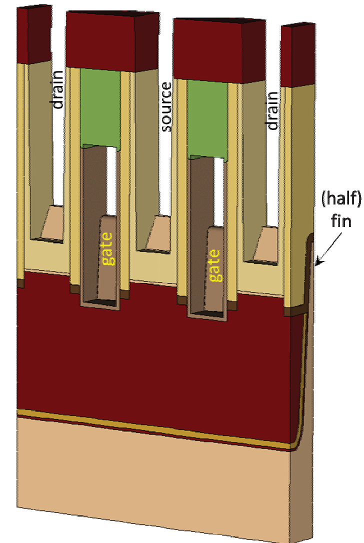

Figure 7. Example of symmetric device having asymmetric S/D resistance due to layout. The shared source will show a larger effective resistance than the unshared drain for this 2-fin device.

TABLE I. EXTRACTED SOURCE, DRAIN, AND CHANNEL RESISTANCE FOR THE SIMPLE PLANAR DEVICE SHOWN IN FIG. 1.

R_{chan} is the linear channel resistance at a gate overdrive of 500mV. The addition of 100 or 200 Ω-µm to the source or drain yields the correct extracted source or drain resistance (to a few % error). For the case of zero added lumped resistance, the difference between R_d and R_s is 260 Ω-µm, which is the resistance of the long drain region in the planar device. Extracted channel resistances are all within ~5% of each other.

Lumped R_s (Ω-µm)	Lumped R_d (Ω-µm)	Extracted R_s (Ω-µm)	Extracted R_d (Ω-µm)	Extracted R_{chan} (Ω-µm)
200	0	278	330	66.0
100	0	176	330	68.6
0	0	73.5	334	66.7
0	100	73.6	434	65.1
0	200	72.4	533	70.5

IV. Conclusions

A simple technique for measuring the individual source, drain, and channel resistance components was proposed and demonstrated using data generated from modeling of a contrived prototype short channel device. Simulation tools capable of modeling high-field transport showed that this technique works well even for devices exhibiting ballistic transport. The technique can be implemented as an in-line test since standard I_d-V_g characteristics are needed along with simple manipulations of that data. It should be noted that this method can be utilized on symmetric devices as well as asymmetric devices. It was shown that nominally symmetric device types may show asymmetric behavior depending on their connectivity or layout. One such example was a shared source 2-fin FinFET device.

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