Modeling and Finite Element Simulation of Gate Leakage in Cylindrical GAA Nanowire FETs

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***Abstract*—The gate-all-around (GAA) nanowire based devices have generated research interest in recent years for their potential in scaling beyond 10nm as they offer excellent control over channel. Reduction in gate oxide thickness and low effective mass channel material for better drive current aid gate leakage which can put limit to further scaling. In this work, we study gate leakage problem for cylindrical nanowire (NW) GAA device and present a model to accurately compute lifetime of the quasi-bound-states (QBS) in inversion region of NW. We study scattering of cylindrical waves by solving Schrödinger equation with open boundary conditions using finite element method (FEM), and thereby calculate gate leakage current for the GAA device. We conduct survey of a broad range of device materials, investigate effect of device dimensions and stress on the gate tunneling leakage. We try to bring out the conditions at which direct tunneling current through the oxide is significant and can possibly exceed the maximum permissible gate current density.**

***Index Terms*—Gate Leakage, Nanowire MOSFETs,**

I. Introduction

Multigate devices are known to reduce short channel effects as channel is surrounded from various sides and among all, best electrostatic controllability over channel is achieved by GAA device as channel is covered from all sides [1] [2] [3]. Due to this advantage, GAA-NW-FET has generated lot of interest recently and it is considered the future of the ultimate CMOS transistor scaling [1], [4]. The cylindrical nanowire FETs with GAA are among the advanced structures that can provide better electrostatic integrity, and offer symmetry that can be utilized to simplify the device model.

Scaling the oxide thickness for continuing Moore's law results in exponential increase in gate leakage current, and diameter scaling increases ground-state energy and modify the effective mass as well that can cause significant impact on loss of inversion charge [5]. Gate leakage is known to be one of the most constraining limit to scaling. Therefore, evaluation of dependence of gate leakage on device geometry is required and corresponding scaling limits need to be determined.

Charge quantization and gate leakage in nanoscale GAA MOS structure are discussed in detail by Spinelli *et al.* [6]. However, study is limited to Si NW and for a fixed geometry. 3D gate leakage model for rectangular NW triple gate device is presented by Luisier *et.al.* [7], however, it lacks a detailed mathematical model and study is limited to Si NW only. Cao *et.al.* [8] present a compact model that compares ground state tunneling probabilities and study is done for limited oxide cases. Recently, fabrication of GAA $In_{.53}Ga_{.47}As$ NW FETs are demonstrated in [9] [10] [11] showing excellent drive current, and it is important to study gate leakage for such III-V material GAA devices as well.

For the purpose of calculating the effect of quantum confinement, it usually suffices to treat the electrons as inhabiting bound states in a quantum well. However, for tunneling calculations, the states need to be treated as quasi-bound since the boundary conditions are open in the radial direction. Tunneling probability estimation is mostly based on WKB approximation that considers electrons traveling to the barrier as plane waves, whereas in NW due to strong confinement the states are strongly localized. The concept of tunneling probability is not meaningful for such states [12] and lifetime of these QBS needs to be calculated in order to accurately determine the tunneling current.

II. Model

In this paper, we consider cylindrical, undoped MOS GAA device with nanowire diameter d_{nw} and oxide thickness t_{ox} as seen in cross sectional view on 2D FEM grid in Fig. (1). Charge density of GAA devices is obtained by employing self-consistent Schrödinger-Poisson simulation with the effective mass approximation to obtain potential profile required for the tunneling calculation. The electron wavefunction in the channel is the product of a 1D plane wave in the z direction and a 2D envelope function on the $x-y$ quantization plane of NW. The electron density inside channel in Hartree a.u. is given as

$$n = \sum_i \sum_v g^v \sqrt{\frac{2m_z^v kT}{\pi}} F_{-1/2}\left(\frac{E_F - E_i^v}{kT}\right) |\psi_i^v|^2 \quad (1)$$

where, g^v, m_z^v are degeneracy and effective mass in transport direction for v^{th} valley and $F_{-1/2}$ is the Fermi-Dirac integral of order -1/2 [6].

We model the system of cylindrical NW MOS structure with cylindrical gate as an open system in radial direction and gate contact as reservoir of electrons. Incoming cylindrical waves described by Hankel function aH_l^- hit the cylindrical barrier and are scattered-off in outward radial direction as seen in Fig. (1). The input amplitude of scattering state a goes to zero at

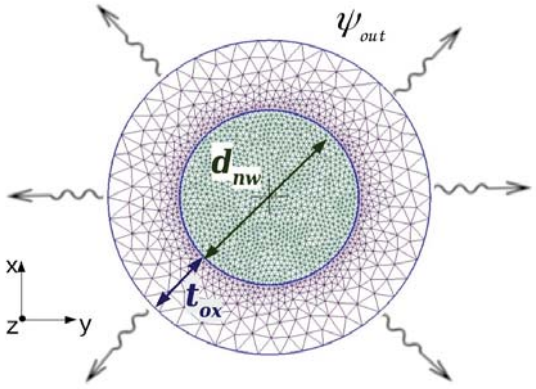

Fig. 1. A non-uniform FEM mesh, generated in GMSH [13], is used for saving computational time without compromising accuracy.

the resonance or pole in the complex-energy plane for QBS are the resonant poles of S-Matrix with complex energy

$$E = E_R - \frac{i\,\Gamma}{2}, \tag{2}$$

where, real part E_R is the resonance energy, its imaginary part Γ and the lifetime τ are related by $\tau = 1/(\Gamma)$ [14]. Outgoing resonant wavefunctions in the gate can be written as,

$$\psi_{out}(\rho,\theta) \quad = \quad rH_l^+(k_m\rho)\zeta(\theta), \tag{3}$$

where ζ is the complex phase and

$$k_m = \sqrt{2m_g^*(E - E_{fm})}, \tag{4}$$

where, E_{fm} is the gate fermi level and m_g is the effective mass in gate material. At contact, the wavefunction can be further simplified by considering asymptotic form of Hankel function. Schrödinger equation can be written in weak form as

$$\underbrace{\frac{1}{2m_g}\int_\Gamma \left(\frac{1}{2\rho_r} - ik_m\right)\Psi^*\Phi d\Gamma}_{C-k_m\Sigma} - E\underbrace{\int_\Omega \Psi^*\Phi d\Omega}_{B} + \underbrace{\left[\frac{1}{2}\int_\Omega \frac{1}{m_q^*}\nabla\Psi^*\nabla\Phi d\Omega + \int_\Omega U\Psi^*\Phi d\Omega\right]}_{A} = 0, \tag{5}$$

where, m_q^* is mass in quantization plane and $\mathbf{\Sigma}$ is complex self-energy matrix representing the open boundary condition. Putting the value of E from (4), above equation can be written as quadratic eigenvalue equation

$$\left(\boldsymbol{H} - k_m\boldsymbol{\Sigma} - k_m^2\boldsymbol{D}\right)\Psi = 0, \tag{6}$$

where,

$$\boldsymbol{H} = \boldsymbol{A} + \boldsymbol{C} - E_{F_m}\boldsymbol{B}; \quad \boldsymbol{D} = \frac{1}{2m_g}\boldsymbol{B}. \tag{7}$$

Above eigenvalue equation can be solved by the sparse solvers to obtain Ψ and the complex wavevector k_m, and thereby the complex energy eigenvalue can be obtained. The finite element matrices are assembled in the Distributed and Unified Numerics Environment (DUNE), that is a modular toolbox for solving differential equations with grid-based methods [15]. Eigenvalue problem in (6) is solved using packages 'Portable, Extensible Toolkit for Scientific Computation' (PETSc) and 'Scalable Library for Eigenvalue Problem Computations' (SLEPc). SLEPc is a software library for the solution of large sparse eigenvalue problems on parallel computers [16].

The tunneling current density due to QBS in NW structure can be written in terms of lifetime τ_i^v for i^{th} state in v^{th} valley,

$$J_{qbs} = \sum_i\sum_v \frac{g^v}{\pi(d_{nw}+2t_{ox})}\sqrt{\frac{2m_z^v kT}{\pi}} F_{-1/2}\left(\frac{E_F - E_i^v}{kT}\right)\frac{1}{\tau_i^v}. \tag{8}$$

III. Simulation Results and Discussion

The parameter values for different channel and oxide materials that are considered in the simulation are shown in Table. (I) and (II), respectively. Band offset of $In_{.53}Ga_{.47}As$, InAs and GaN with Al_2O_3 is taken as 3.1, 3.6 and 2.16eV, respectively. The same for Si with SiO_2 is taken as 3.1eV.

Self-consistent Schrödinger-Poisson simulations are run for a non-uniform grid as shown in Fig. (1) for generating the band profiles at a given gate bias. Once the band profiles are obtained, a quadratic eigenvalue equation (6) is linearized and solved as described in [17] to get the lifetime of the states and its contribution towards the tunneling current. The bound quantum state wavefunctions in channel and leaky QBS obtained by self-consistent simulation and lifetime calculations can be seen in Fig. (2) and (3), respectively. Simulator is validated against the available tunneling current data for Si/SiO_2 NW in Ref [6] which can be seen in Fig. (4).

TABLE I
Parameters values for channel materials

Materials	E_g	ϵ_r	n_i	χ_e	m_q	m_z	g
Si	1.12	11.8	1.45E10	4.0	0.43	0.19	4
					0.19	0.98	2
$In_{.53}Ga_{.47}As$	0.74	13.9	6.4E11	4.5	0.04	0.04	1
InAs	0.36	15.15	2E14	4.9	0.08	0.08	1
GaN	3.2	8.9	2E-10	4.1	0.3	0.3	1

TABLE II
Parameters values for oxide materials

Materials	E_g (eV)	ϵ_r	$m_e{}^*$
SiO_2	9	3.9	0.5
HfO_2	5.9	25	0.2
Al_2O_3	6.5	9	0.2

Self-consistent charge density obtained from the model is shown for different NW devices in Fig. (5). Charge density is minimum for $In_{.53}Ga_{.47}As$ channel due lower m_q which results in larger confinement energy and smaller fermi function.

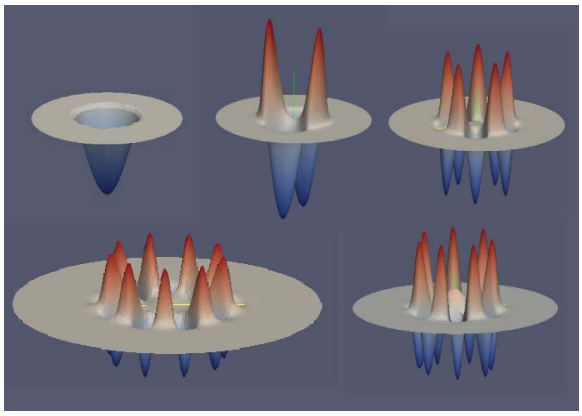

Fig. 2. 3D plot of wavefunctions for various states in the channel with vanishing boundary condition on gate

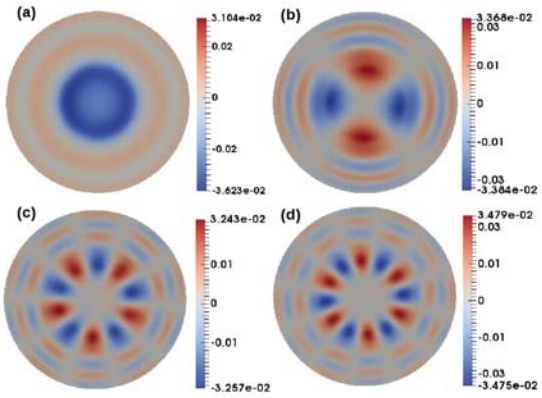

Fig. 3. 2D color plot of various QBS with barrier height reduced to 1eV in order to visualize the tunneling. Tunneling from these states in the radial direction can be seen as ripples in the oxide.

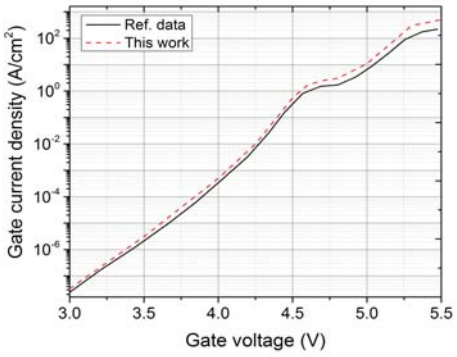

Fig. 4. Validation of this model with the available data in Ref [6] for Si/SiO_2 device with d_{nw}=6nm and t_{ox}=4nm.

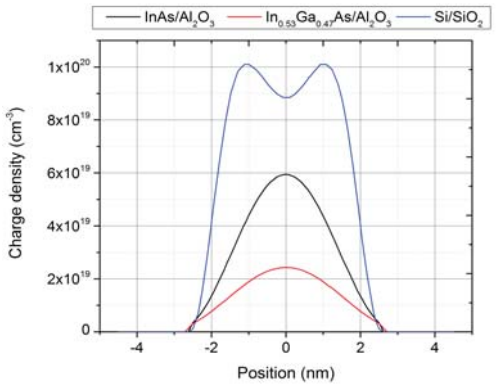

Fig. 5. Charge density for different materials at V_g=1V for $d_{nw} = 5$nm with $t_{ox} = 2$nm.

The gate leakage dependence on oxide thickness for $In_{.53}Ga_{.47}As$ NW device is shown in Fig. (6). There is almost three-decade increase in gate leakage with 1nm decrease in oxide thickness. This suggests that oxide scaling below 3nm requires nearly 0.2V voltage scaling per nm for maintaining same gate current density. The oxide scaling for $In_{.53}Ga_{.47}As$ channel below 2nm will exceed gate current value 1e2 A/cm^2 which can pose a problem.

Fig. (7) shows that gate leakage for GaN device is significantly low even at high V_g. It can also be seen that $In_{.53}Ga_{.47}As$ with composite oxide have lower leakage than InAs for $V_g < 0.7$V. Use of composite Al_2O_3/HfO_2 (EOT = 0.56nm) stack does not significantly increase direct tunneling current compared with single Al_2O_3 (EOT = 0.86nm) having the same physical thickness. Noticeably, the lower leakage current at $V_g = 1$V for Si/SiO_2 device compared to InAs and $In_{.53}Ga_{.47}As$ with Al_2O_3 oxide indicate larger lifetime for Si as its charge density is comparatively higher (see Fig. (5)). Electron lifetime depends on field across oxide, NW diameter and the channel and oxide effective mass. As NW diameter is same for all devices, larger lifetime in Si/SiO_2 device despite high oxide field is because of comparatively higher oxide mass and m_q.

Decreasing channel diameter increases the confinement energy and channel effective mass [18] [19]. This results in reduced charge density due to reduction in fermi function. Lifetime increase with increasing effective mass. Thus, NW diameter scaling reduce gate leakage current as seen in Fig. (8).

Compressive strain lowers the gate leakage as seen in Fig. (9) which is computed by considering modified band valleys Δ_2 and Δ_4 as described in Mehrotra *et. al* [3]. For the GAA devices studied, gate leakage does not exceed 1e2 A/cm^2 at 1V for EOT larger than 0.9nm.

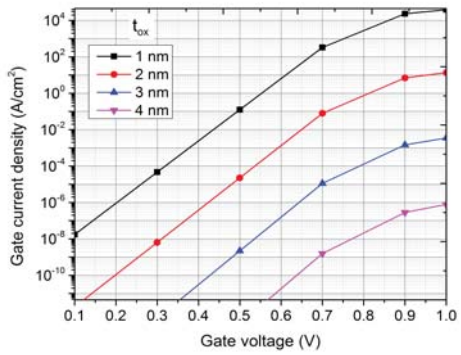

Fig. 6. Gate current-voltage characteristics of $In_{.53}Ga_{.47}As$ with d_{nw} =5nm and various Al_2O_3 thickness.

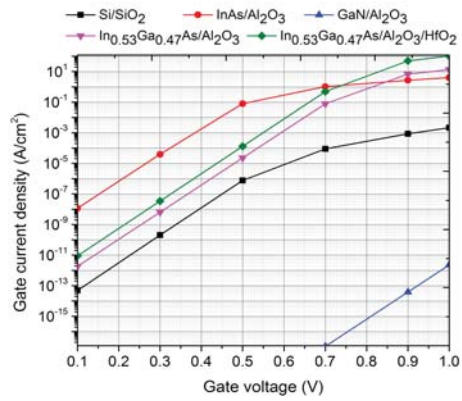

Fig. 7. Gate current-voltage characteristics of different channel-oxide materials with d_{nw} 5nm and oxide thickness of 2nm. Al_2O_3/HfO_2 is 1nm each keeping same physical thickness for comparison.

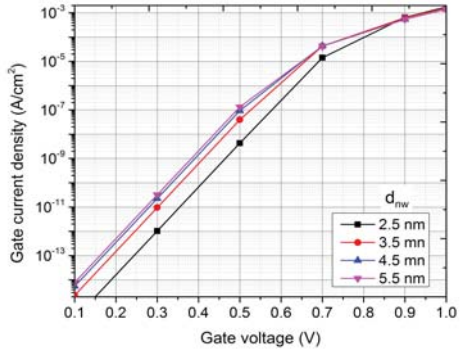

Fig. 8. Variation of gate current-voltage characteristics of Si/SiO_2 with d_{nw} = 2.5nm, 3.5nm, 4.5nm and 5.5nm, t_{ox} = 2nm.

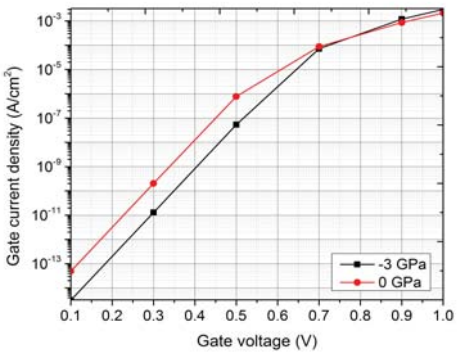

Fig. 9. Gate leakage for compressive strained and unstrained Si NW with d_{nw} = 5nm with t_{ox} = 2nm.

IV. Conclusion

The gate leakage current in cylindrical NW MOS structure is calculated for various channel, oxide materials, strain and geometries using a new method for computing lifetime of the QBS formed in cylindrical inversion region. $In_{.53}Ga_{.47}As$ and InAs channel material devices give rise to higher leakage current compared to Si device due to lower channel and oxide effective mass. It is found that GaN has the lowest gate leakage as compared to other channel materials due to its high bandgap. $In_{.53}Ga_{.47}As$ with composite oxide structure show highest gate leakage among the studied devices at 1V gate bias. Compressive strain and diameter scaling are found to reduce gate leakage current density.

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