Statistical Variability Simulation of Novel Capacitor-less Z2FET DRAM: From Transistor to Circuit

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Introduction

The downscaling of traditional DRAM [1] is facing challenges due to the presence of external capacitor. Z2FET [2-5] has been demonstrated as a promising DRAM candidate eliminating the need for external capacitor. In the past, attention was focused on the optimization of device structure [5] and fabrication process [2] without paying much attention to the Statistical (local) Variability (SV) which is crucial for any memory technology. In this paper, a novel simulation methodology is proposed and the SV of DRAM Memory Window (MW) is investigated systematically. It is found that SV of MW is dominated by Metal Gate Granularity (MGG) coming from the Gated-SOI region of the Z2FET. Although Random Discrete Dopant (RDD) induced variations in the threshold voltage (Vth) has larger spread in the Intrinsic-SOI part, it has no significant effect on the overall Z2FET characteristics. Based on the proposed methodology, SV of MW at different process corners has also been studied. Results reveal the necessity for further process optimization due to the best corner giving rise not only to larger average MW but also less variations. Furthermore, circuit level read performance (including the variability) of a Z2FET-based memory cell have been evaluated. All these findings could guide the further performance optimization from both device and memory cell circuit point of view for Z2FET-based volatile memory product development.

Z2FET Memory Operation

The Z2FET (Fig. 1a) channel consists of a p-i-n structure on a SOI substrate. The front gate (FG) partially covering on top of Si channel and back gate (BG) together control electron and hole potential barriers. For memory operation, the FG and BG are independently biased positively and negatively. Hence, complementary potential barriers are created in the channel. The typical memory operations with sequence of program '0' (P0), hold (H0), read (R0), program '1' (P1), hold (H1), and read (R1) have been simulated in Fig. 1b. The memory window (Fig. 2) is defined by the gap between switch-on anode voltages (VA) of state '0' and '1'. The concentration of electrons (Fig. 3a) in Gated-SOI region determines memory state '0' or '1'. The one sweeping from state '0' has higher switching VA, corresponding to low non-equilibrium concentration of electrons in Gated-SOI, gives rise to higher local potential barrier (Fig. 3b). MW determines the appropriate VA that should be applied during read operation (Fig. 3c). Detailed Z2FET operation principles have been given in [2-5]. Device simulation in this work were carried out by employing Synopsys Garand and Sentaurus Device [6, 7]. Circuit simulation was done using the Sentaurus Device mixed-mode function [6] by connecting additional physical transistors and capacitor. Fabrication process is fully compatible with STMicroelectronics 28 nm FDSOI technology [4, 5].

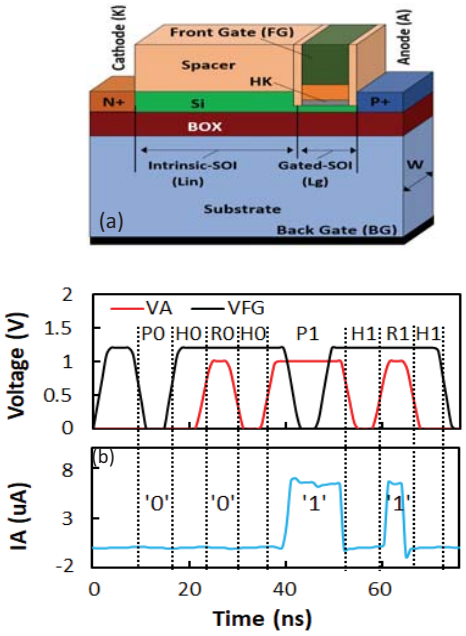


Fig. 1 3D Z2FET structure. Lg, Lin and W are 30nm, 100nm and 30nm respectively. The current flowing path is composed of p-typed anode, body Si, and n-type cathode. (b) is simulation result of typical Z2FET memory operation.

Simulation Methodology

Z2FET has combined behaviour of diode, thyristor and MOSFET. For statistical study, we developed a novel methodology to evaluate SV in Z2FET. The procedure is described in Fig. 4: 1) Z2FET is partitioned into two components (Fig. 4a): Gated-SOI transistor and Intrinsic-SOI gate-less SOI transistor. 2) Each SOI device is calibrated to match the fabrication technology of ST FDSOI

28nm process. 3) Four major statistical variability sources were introduced in each component: Random Discrete Dopant (RDD), Line Edge Roughness (LER), Metal Gate Granularity (MGG) and Body-Si Roughness (BSR). 4) For each variability source, 200 Intrinsic-SOI (Fig. 4b) and 200 Gated-SOI (Fig. 4c) are simulated independently using Garand [7]. 5) Extracted variations in the Vth of the simulated characteristics are reflected into work-function (WF) variations for Gated-SOI and interface states (Nit) variation for Intrinsic-SOI based on formulas in Fig. 4d. 6) These statistical distributions are combined in statistically independent manner and applied to the Z2FET MW statistical simulation (Fig. 4e) or memory cell circuit variability for design-technology co-optimization [8, 9].

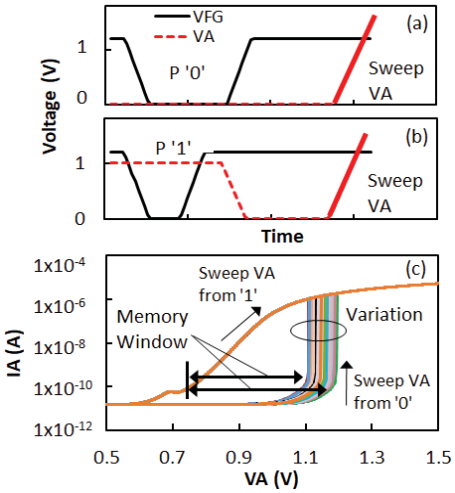


Fig. 2 Memory window simulation. Voltage waveform of FG (VFG) and Anode (VA) sweeping from a) state '0' and b) state '1'. c) shows the obtained simulation results considering device-to-device variation. The memory window is defined as the gap between two VA voltages where IA current starts to switch. Within the memory window, state '1'/'0' gives rise to higher/lower current. Too high or too low VA would not be able to differentiate currents of '0' and '1'.

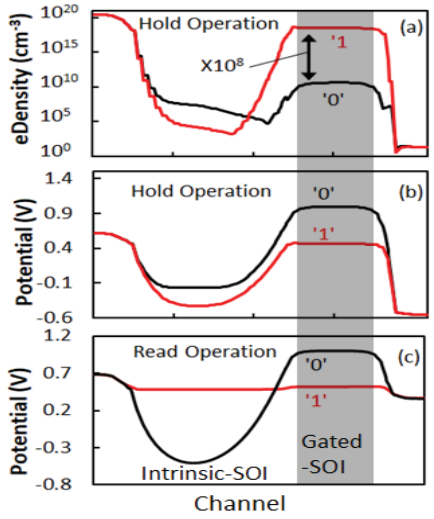
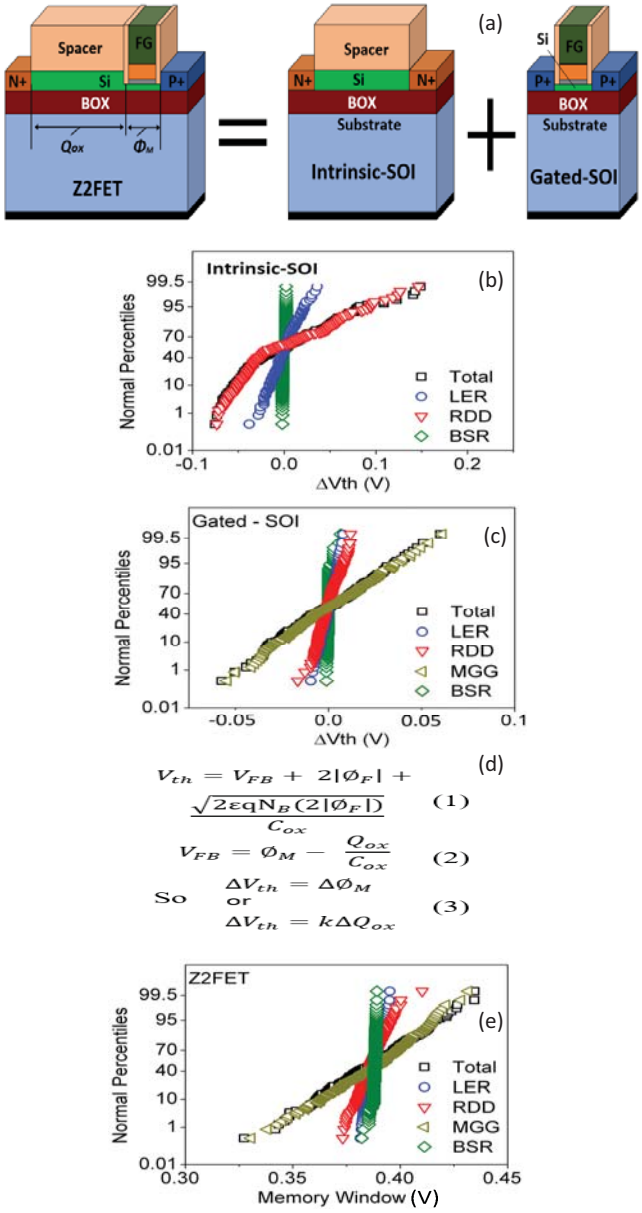


Fig. 3 Distribution of (a) Electron density, (b) Potential under Hold operation, and (c) Potential under Read operation for both state '0' and state '1' along body Si channel. State '0' contains much more electrons than '1' in Gated-SOI.



$$V_{th} = V_{FB} + 2|\phi_F| + \frac{\sqrt{2\varepsilon q N_B (2|\phi_F|)}}{C_{ox}} \quad (1)$$

$$V_{FB} = \phi_M - \frac{Q_{ox}}{C_{ox}} \quad (2)$$

$$\text{So} \quad \Delta V_{th} = \Delta\phi_M \text{ or } \Delta V_{th} = k\Delta Q_{ox} \quad (3)$$

Fig. 4 Methodology illustration of Z2FET variability simulation. Z2FET is divided into two components a) Intrinsic-SOI component and Gated-SOI component. Variability of each component can be obtained in (b) and (c) by employing GARAND, then the individual variability data is integrated into Z2FET according to eq. (d). Four major variability sources LER, RDD, MGG and BSR are considered. Total is the variability considering all sources. MGG is not simulated in Intrinsic-SOI since absence of metal gate. e) is the integrated variability of Z2FET.

Results and Discussion

There are only three variability sources for Intrinsic-SOI region due to the absence of metal gate. Results in Fig. 4b show that RDD dominates the overall variability in Intrinsic-SOI region, while LER contributes less and BSR has the weakest contribution. This is due to the fact that the

Intrinsic-SOI device has extremely thick back-gate oxide (25nm), hence any RDD induced channel un-screened potential fluctuation cause large Vth variations. Meanwhile its long/thick channel significantly suppress LER/BSR effect. However, in the Gated-SOI region, MGG (Fig. 4c) is the dominant source of variability. RDD becomes less important due to the near intrinsic channel doping in combination with strong front gate screening, and LER and BSR are also negligible. Although the MGG induced Vth spread only of ~100mV, which is much less than RDD induced 300mV in the Intrinsic-SOI region, MGG dominates the overall Z2FET variability (Fig. 4e). This suggests that Z2FET MW is mainly controlled by Gated-SOI region. This is confirmed by the correlation results presented in Fig. 5, where MW has a strong correlation with the Gated-SOI region but weak correlation with Intrinsic-SOI region. Positive ΔVth result in smaller |Vth| in Gated-SOI and as a result, smaller MW will be obtained.

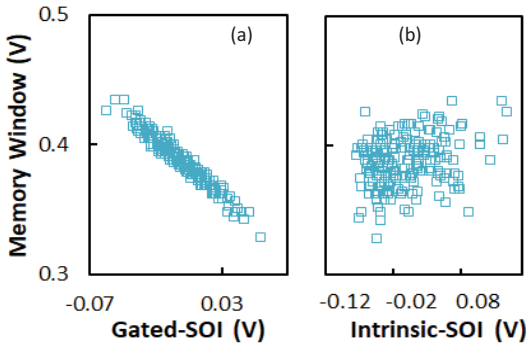


Fig. 5 Correlation of memory window on partitioned components, a) Gated-SOI and b) Intrinsic-SOI. Strong correlation is observed on Gated-SOI but not on Intrinsic-SOI, suggesting MW is only sensitive to Gated-SOI.

Process Corners

Four process parameters: EOT of front gate, intrinsic region length (Lin), front gate length (Lg) and channel Si thickness (Si), are regarded to have the most significant impact on Z2FET characteristics. The nominal size represents median value in fabrication, while the other corners are the possible process variation within a certain sigma deviation from the nominal value. The dependency of MW on each process parameter can be seen from the surface plot shown in Fig. 6. The MW linearly increases with the reduction of the Si, EOT and the increase of the Lin and Lg length. Red point '●' indicates the best corner and green point '●' indicates the worst corner for MW. The SV in combination with process corners can be used to evaluate memory cell yield. As expected, the worst corner has smaller averaged MW (Fig. 7a); but it has also the largest standard deviation (Fig. 7b), which suggests that in terms of MW the fabrication process can be optimized by reentering in the direction of the best corner without compromising the device performance and process variation. At all corners, MGG is always the dominant variability source for the Z2FET MW.

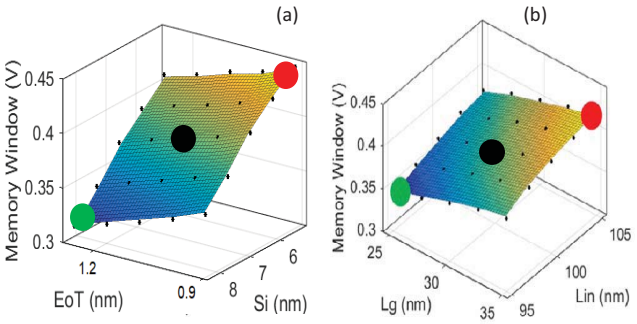


Fig. 6 Process corners in terms of parameters: a) thickness of EOT and Si, and b) length of Lin and Lg. Memory window increases with thinner Si, EOT, and longer Lin, Lg. Best corner (●) and worst corner (●) can be obtained according to the linear dependency.

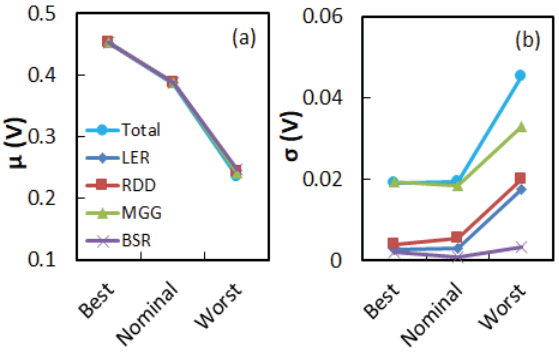


Fig. 7 a) Mean and b) sigma value of MW under different process corners. Although best corner gives a wider memory window, the standard deviation even becomes smaller. MGG always dominates the variation under all corners.

Variability of Z2FET-based Memory circuit

MW (Fig. 2c) is an important FoM that determines the range of VA that could be applied in read operation. Fig. 8a shows the memory cell circuit where VDD pre-charges the capacitor corresponding to the parasitic bit line capacitance in a memory matrix. The stored state can be sensed by the voltage differentiation on complementary bit lines. Read operation starts by disabling N1 meanwhile enabling P1. Simulations (Fig. 8b) confirm a voltage drop for stored '1', however, too low pre-charged VA (dashed line) would not be suitable for sensing. The other way around, too high pre-charged VA will destroy the stored '0' (dashed line in Fig. 8c). Both extreme cases are not able to differentiate between '1' and '0' correctly.

Using the optimized VA level, variability of read time (t_R) and differentiation voltage (ΔV) are simulated (Fig. 9) by importing the extracted device variability data. Results show that both t_R and ΔV are mainly affected by process corners, the SV is less important. It is interesting to note that the best/worst corners of MW swap and become to worst/best corners for t_R and ΔV. Read speed is controlled by the discharge current of capacitor which depends on the magnitude of IA flowing through Z2FET. The worst/best

corner of MW has thicker/thinner body-Si thickness (Fig. 6a) which leads to higher/lower IA current, corresponding to shorter/longer t_R or larger/smaller ΔV. At the worst corner, cells yield (Fig. 9c) is calculated at different pre-charged VA. Clearly, for longer read time (t_R=35ns) the yield gets improved with reduced pre-charged VA as lower VA can reduce the damage rate of data '0', as illustrated in Fig. 8c. However lower pre-charged VA will also reduce the read current and slow down the read speed, as a result, yield becomes worse again with lower VA when t_R is shorter (Fig. 9c). Therefore, associated with VA optimization, trade-off need to be made between yield and read speed.

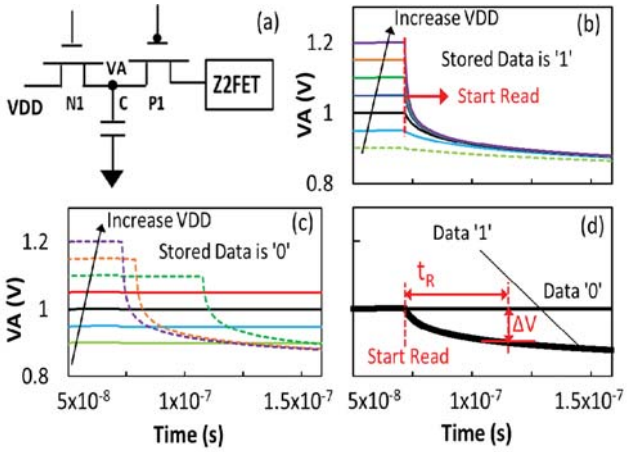


Fig. 8 a) Compact Z2FET-based memory circuit implemented using mixed-mode in Sentaurus Device. VA voltage at different read time is simulated when stored information is b) '1' or c) '0'. Dashed lines indicate inappropriate VDD (pre-charged VA) values are used which either causes too small VA drop in b), or turning of stored data from '0' to '1' in c). d) defines the read time t_R and differentiation voltage ΔV.

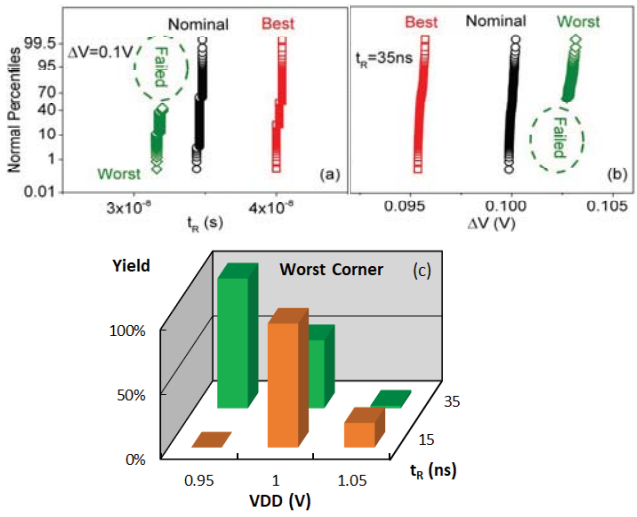


Fig. 9 a) Variability simulation of a) read time t_R and b) differentiation voltage ΔV. Criteria ΔV=100mV in a) and t_R=35ns in b) are used respectively. Read performance is mainly affected by long-range process variation instead of SV. At the worst corner, partial DUTs failed since the data damage described in Fig. 8c. c) shows the yield can get improved at lower VDD for t_R=35ns, but not for t_R=15ns.

Conclusion

In this paper, we have proposed a novel simulation methodology to study variability in Z2FET technology at both device and circuit levels. It is found that MW variability of Z2FET comes predominantly from MGG in the Gated-SOI region. The process optimization can move towards best corner since best corner can give rise to not only larger mean MW, but also less deviation. Simulation of Z2FET-based memory circuit reveals that process corners have dominant impact on read performance. Optimization of VA level is essential to improve yield, with the tradeoff on read speed. All of these findings will be very helpful for circuit designers to optimize memory matrix cell.

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