A Highly Scalable and Energy-Efficient 1T DRAM Embedding a SiGe Quantum Well Structure for Significant Retention Enhancement

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***Abstract*— In this study, a capacitorless one-transistor dynamic random-access memory (1T DRAM) featuring a novel structure with SiGe quantum well (QW) is proposed and characterized by rigorous simulation. It is demonstrated that the ultra-thin vertical channel and SiGe QW greatly improve device scalability and data retention. In write operation, band-to-band tunneling is applied for faster write speed, higher device scalability, and stronger temperature tolerance. Moreover, the SiGe QW at the drain side generates an increased amount of holes at lower operation voltage and enhances the retention time by constructing a more effective hole storage. As the results, the proposed SiGe QW 1T DRAM showed sub-10-ns fast write and erase times and a long retention time reaching up to 1.12 s.**

Keywords—capacitorless DRAM, 1T DRAM, SiGe quantum well (QW), band-to-band tunneling, enhanced retention time, SiGe QW 1T DRAM, sub-10-ns write and erase

I. Introduction

Conventional DRAM cell has one transistor and one capacitor (1T1C) for making up a unit cell. Although great deal of effort is being still made for DRAM capacitors through high-κ dielectric and novel structuring with larger effective area, the existence of capacitor has been the major hindrance to higher device scaling and has actually retarded the evolution of DRAM technology. To make the breakthrough, capacitorless DRAM or one-transistor (1T) DRAM has been aggressively researched recently [1]–[3]. A hole pocket by constructed by SiGe QW replacing the capacitor can be schemed for storing larger amount of holes compared with the existing devices based on the plain Si floating body [4]. In this study, further advance is achieved by employing band-to-band tunneling for write operation, by which increased scalability and enhanced reliability through controlling the SiGe thickness below the critical thickness and discarding impact ionization are obtained. It has been confirmed that optimal device design ensures the significantly increased data retention and sensing margin, along with the benefits of full Si processing compatibility and high cost effectiveness thanks to fabrication basis on bulk Si.

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II. Device Structure and Simulation Strategy

Fig. 1 shows a schematic of the proposed 1T DRAM with insets for energy-band diagram at $V_{GS} = V_{DS} = 0$ V (upper) hole concentration contours at the off state (lower left segment) and write operation (lower right one). Gate length (L_g) and channel thickness (T_{ch}) are 100 nm and 30 nm, respectively. Ge fraction (x) and length of the SiGe layer is 30% and 50 nm, respectively.

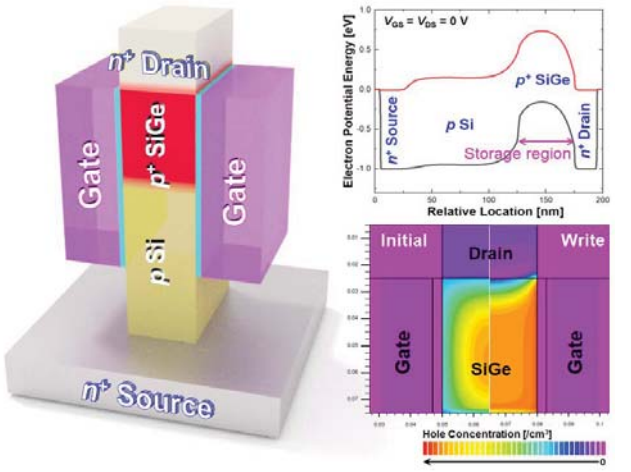

Fig. 1. Schematic of the SiGe QW 1T DRAM cell. Insets for off-state energy-band diagram (upper) and hole distributions at off-state (lower left segment) and right after a write operation is completed (lower right).

Under these conditions, it was confirmed that the $Si_{0.7}Ge_{0.3}$ QW effectively confines the excessive holes generated over a write operation, without serious lattice mismatches with top/bottom Si. The material parameters including carrier mobilities and saturation velocities were semi-empirically prepared by modeling as a function of x, from the existing measurement results [5], and then, fed into the device simulations of devices with different x values in performing the optimal device design. For even higher accuracy of the simulation results, field-, doping-, and temperature-dependent mobility models, doping-concentration-dependent Shockley-Read-Hall (SRH) model, Auger recombination model, bandgap narrowing model, and non-local band-to-band tunneling calculation were activated.

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III. Operations of the SiGe QW 1T DRAM

Fig. 2 shows the energy-band diagrams under write (upper) and erase (lower) operation conditions. While writing state "1", the valence electrons in the p^+ $Si_{0.7}Ge_{0.3}$ layer are injected into the drain junction by band-to-band tunneling. The remaining holes are confined in the $Si_{0.7}Ge_{0.3}$ QW and lower the bands by elevating the QW potential. Erase operation is performed by sweeping out the holes to the drain junction through a large enough negative drain voltage (V_{DS}) as shown in the figure.

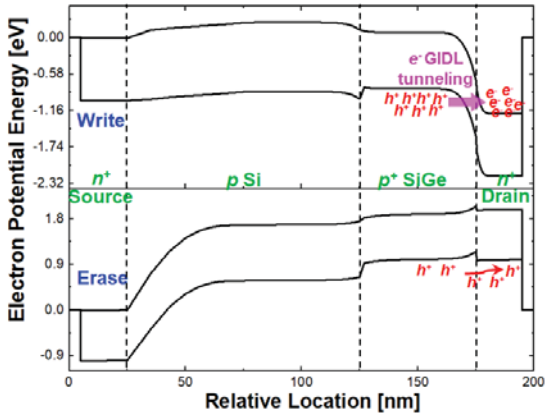

Fig. 2. Energy-band diagrams. Program (upper) and erase (lower) operations.

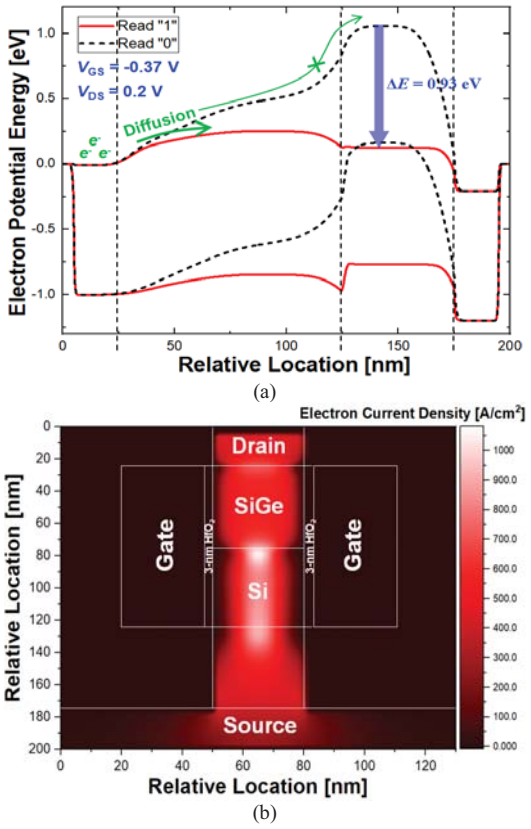

Fig. 3. Read operation characteristics. (a) Energy-band diagrams at read operations for state 0 (upper) and 1 (lower). (b) Electron current density contour under the read-1 operation condition.

In Fig. 3(a), the energy-band diagrams in read operations of state 0 (black dotted line) and 1 (red solid line) are depicted. It is confirmed by the simulation results that there is a large difference between energy barriers for each state, 0.93 eV, seen by the source electrons. Fig. 3(b) shows the electron current density spatially read at state 1, where high brightness is observed along the vertical channel, owing to barrier lowering.

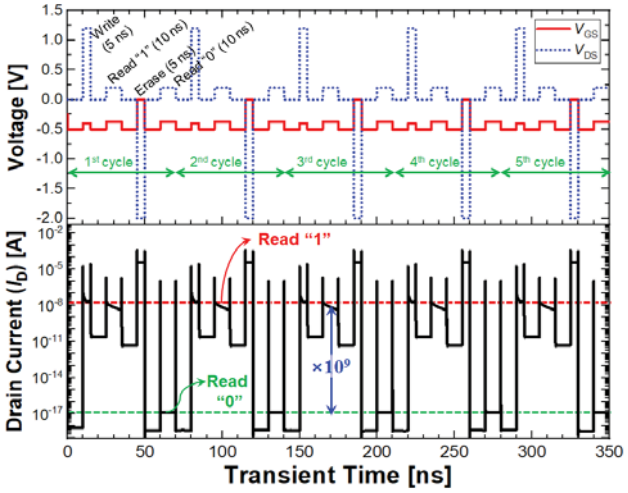

Fig. 4. Transient operation characteristics of the $Si_{0.7}Ge_{0.3}$ QW 1T DRAM over 5 cycles where a single cycle consists of 8 operations (write 1/hold/read 1/hold/write 0/hold/read 0/hold).

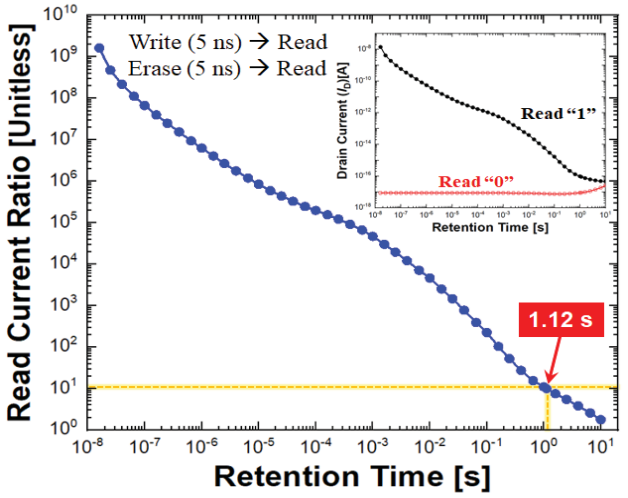

Fig. 5. Read-1/read-0 current ratio as a function of time. Retention time as long as 1.12 s is obtained by a presumable reference current ratio of 10^1. The inset shows the raw read currents.

Fig. 4 demonstrates the transient simulation results from the optimally designed $Si_{0.7}Ge_{0.3}$ QW 1T DRAM over 5 cycles of 1T DRAM operations. Sub-10-ns ultra-short write and erase operation time and the high current ratio of 10^9 between states 1 and 0 are confirmed. Fig. 5 depicts the read-1/read-0 current ratio as a function of time and the retention time is extracted to be 1.12 s long for a presumable reference current ratio of 10^1.

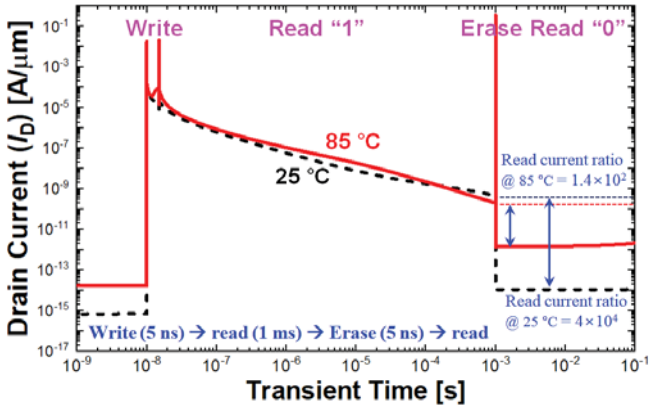

Fig. 6. Temperature dependence of drain currents in the respective operation regions at 25 °C and 85 °C. Even under the harsher temperature condition, current ratio is maintained to be > 10^2.

In Fig. 6, dependence of read current on temperature is investigated at 25 °C and 85 °C. While read-1 current is practically invariant with temperature, read-0 current shows the relatively larger difference, which is mainly due to the larger contribution of thermally generated carriers in portion in state 0. It is notable even under the harsher condition that the read-1/read-0 current ratio is kept to be higher than 10^2.

TABLE I. OPERATION SCHEME FOR THE $Si_{0.7}Ge_{0.3}$ QW 1T DRAM

	V_{GS} [V]	V_{DS} [V]	Time [ns]	Energy [J]
Write	-0.4	1.2	5	1.29×10^{-16}
Erase	0	-2.0	5	3.83×10^{-13}
Read	0.37	0.2	10	Read "1": 1.66×10^{-16} Read "0": 1.13×10^{-25}
Hold	-0.5	0	10	0

Table I summarizes the operating bias schemes and the energy consumption for each operation through a straightforward calculation. The total energy consumption over a single cycle is as low as 0.38 pJ.

IV. CONCLUSION

In this study, we proposed a highly scalable and energy-efficient vertical SiGe QW 1T DRAM. Ultra-short program and erase operations taking no longer than 5 ns are realized and a long retention time reaching 1.12 s has been confirmed. The energy consumption per cycle could be dragged down to 0.38 pJ and the robustness against temperature deviation has been also confirmed. The proposed QW 1T DRAM equips both high-speed and low-power operation capabilities which make the device ready for leading the advanced DRAM technology and highly suitable to more embedded-system-oriented DRAM.

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