Investigation of the Dynamic Thermal Characteristic in Bulk FinFET

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***Abstract*—Knowledge of thermal characteristic in device is valuable to thermal management determination. In this paper, the dynamic thermal characteristic of bulk FinFET is investigated with an analytic method of thermal impedance extraction. The validation of this method is confirmed with the model of small-signal Y-parameters at low frequency. The results show that, although the saturation current is relatively small, the associated temperature rise is very significant. As comparison, dynamic thermal behavior of SOI is also investigated. The results provide a reliable base for the selection of thermal management algorithms for the circuits carrying various frequency components. This method is easy to scale and adjust to device with different dimension and fabrication processes.**

***Index Terms*—FinFET, thermal impedance, dynamic thermal characteristic**

I. Introduction

3D FinFET has been proved as an alternative for planar CMOS as technology scales down below the 20 nm technology node [1], [2]. Meanwhile, as power density has continued to increase unprecedentedly with the technology scaling, the accompanying self-heating induced thermal impact across the device and circuit has become a growing concern. It affects the design decisions like margins, floorplan and cooling costs. To minimize the thermal impact on the performance of device and functional circuit, dynamic thermal management [3] has been proposed as an effective technique to control the over-heating of the circuit. Typically, in order to obtain reliable results of thermal management, simulation data are used to determine the thermal management algorithm. This technique relies heavily on the knowledge of thermal properties at device and circuit level. Hence, it is quite indispensable to characterize and model the thermal behavior of FinFET device.

Since heat transfer is by nature a lowpass mechanism, a conventional p-node RC thermal equivalent circuit shown in Fig.1(b) is proposed to represent the thermal behavior in previous work [4]. Thermal resistance (R_{th}) and thermal capacitance (C_{th}) are used to predict thermal behavior in device. The thermal impact is significant in DC when the device power dissipation is high, and becomes diminishing as the frequency increases. According to this, Scholten [4] proposed a method of extracting thermal resistance and thermal capacitance of a p-node thermal network by fitting the difference between the actual Y-parameters (Y_{DD}) and isothermal counterparts (Y_{DD}^{iso}).

$$\Delta Y_{DD} = Z_{th} M \left(I_{ds} + V_{ds} Y_{DD}^{iso} \right) \tag{1}$$

$$\Delta Y_{DG} = Z_{th} M V_{ds} Y_{DG}^{iso} \tag{2}$$

Instead of this fitting based method, this paper proposes an analytic method for thermal resistance and thermal capacitance extraction. The thermal resistance and thermal capacitance is calculated by Y-parameter of measurement at low frequency and high frequency. With this method, the dynamic thermal behavior of FinFET device is characterized and modelled. The temperature increase can be estimated and the dynamic thermal impact on device can be evaluated. This method is easy to scale and adjust to device with different dimension and fabrication processes.

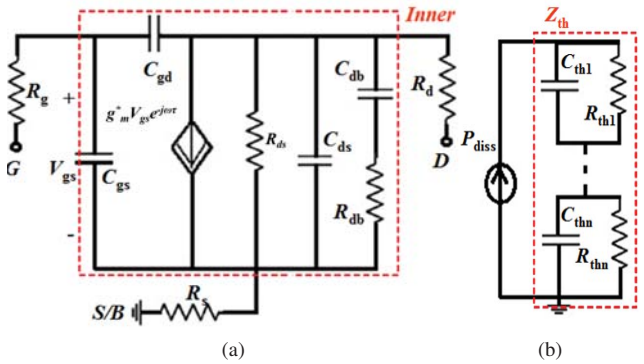

Fig. 1. (a) Proposed small-signal model for bulk FinFETs and (b) General thermal equivalent circuit. R_{thi} and C_{thi} $(i = 1$ to $n)$ are the thermal resistances and capacitances, respectively.

II. Thermal Impedance Extraction Method

Considering the small-signal equivalent circuit and thermal feedback network in Fig.1(a) [5], the intrinsic Y-parameters of a bulk FinFET at low frequency can be written as:

$$Y_{11,\text{int}}^{*} = j\omega \left(C_{gs} + C_{gd} \right) \tag{3a}$$

$$Y_{12,\text{int}}^{*} = -j\omega C_{gd} \tag{3b}$$

$$Y^*_{21,\text{int}} = \left(g_m e^{-j\omega} - j\omega C_{gd}\right)\left(1 + \sum_{i=1}^{p} \frac{k_{thi}}{1 + j\omega\tau_{thi}}\right) \quad (3c)$$

$$Y^*_{22,\text{int}} = g_{ds} + j\omega C_{ds} + \left(R_{sub} + \frac{1}{j\omega C_{sub}}\right)^{-1} + \sum_{i=1}^{p} \frac{1}{R_{ti} + j\omega L_{ti}} \quad (3d)$$

Where C_{gd}, C_{ds}, C_{gs} and C_{sub} are Gate to Drain, Drain to Source, Gate to Source and Drain to Substrate capacitance, respectively. g_m and g_{ds} are DC transconductance and output conductance, respectively. R_{ds} and R_{sub} are Drain to Source resistance and Substrate resistance respectively. $k_{thi} = -M_D P_{diss} R_{thi}$, $\tau_{thi} = R_{thi} C_{thi}$, $R_{ti} = (M_D I_D R_{thi})^{-1}$, $L_{ti} = C_{thi}/M_D I_D$. P_{diss} is the dissipated power. M_D is the relative change of the drain current (I_D) per degree temperature change at constant voltages.

The small-signal parameters in (3) can be extracted from S-parameter at high frequency with the method mentioned in [5]. By applying [5], $R_{d/s}$ can be extracted from linear but strong inversion region of FinFET device as $R_d = \text{Re}\,(Z_{22} - Z_{12}) - A/2$ and $R_s = \text{Re}\,(Z_{12}) - A/2$, respectively. Where $A = \text{Im}\,(Z_{22})\,/\,(\omega C_x)$, C_x is the slope of the linear regression of $-\omega/\text{Im}\,(Z_{22})$ against ω^2 curve. R_g can be determined from the linear regression of $\text{Re}(Y_{11})/\text{Im}(Y_{11})^2$. Once $R_{g/d/s}$ is obtained, the high frequency intrinsic part of Y-parameters ($Y_{\text{int\_HF}}$) in Fig.1(a) can be derived from the Z-parameters of the device as:

$$Y_{\text{int\_HF}} = \begin{bmatrix} Z_{11} - R_g - R_s & Z_{12} - R_s \\ Z_{21} - R_s & Z_{22} - R_d - R_s \end{bmatrix} \quad (4)$$

After that, R_{sub} and C_{sub} can be extracted from the intercept and slope of $[\text{Re}\,(Y_{22,\text{int\_HF}} + Y_{12,\text{int\_HF}})]^{-1}$ versus ω^{-2} at zero bias ($V_{ds} = V_{gs} = 0$). C_{gd} and C_{gs} can be extracted as $C_{gd} = -\text{Im}\,(Y_{12,\text{int\_HF}})\,/\omega$ and $C_{gs} = -\text{Im}\,(Y_{11,\text{int\_HF}})\,/\omega - C_{gd}$, respectively. C_{ds} can be calculated from the imaginary part of $Y_{22,\text{int\_HF}}$.

For a p-node thermal feedback network, p different resonant frequencies can be used to determine τ_{thi} as $\tau_{thi} = 1/2\pi f_{thi}\,(i = 1, \cdots, p)$. As the small-signal parameters are extracted, R_{thi} and C_{thi} can be derived from (3) as:

$$-M P_{diss} W R^T = G^T \quad (5)$$

where

$$R = [R_{th1} \cdots R_{thp}] \quad (6)$$

$$W = \begin{bmatrix} (1 + j\omega_1\tau_{th1})^{-1} & \cdots & (1 + j\omega_1\tau_{thp})^{-1} \\ \vdots & \ddots & \vdots \\ (1 + j\omega_p\tau_{th1})^{-1} & \cdots & (1 + j\omega_p\tau_{thp})^{-1} \end{bmatrix} \quad (7)$$

$$G = \left[\frac{g_m e^{-j\omega_1\tau} - j\omega_1 C_{gd}}{Y^1_{21,\text{int}}} - 1 \cdots \frac{g_m e^{-j\omega_p\tau} - j\omega_p C_{gd}}{Y^p_{21,\text{int}}} - 1\right] \quad (8)$$

As the thermal resistance and thermal capacitance are extracted, the dynamic thermal impact on device can be characterized and modelled.

III. Dynamic Thermal Behavior

In this work, the dynamic thermal behavior of a 14 nm FinFET device is investigated. The number of fin is 8, the number of fingers 8 and channel length is 36 nm. Small-signal S-parameters from 100 KHz to 3 GHz and 200 MHz to 50 GHz are measured and de-embedded (open + short) for small-signal parameters extraction using Keysight E5072 and E8363B network analyzers, respectively. The RF power of measurement is -20dBm.

A 3-node thermal network is adopted and three resonant frequencies of Im (Y_{21}) (f_{th1} = 1.2 MHz, f_{th2} = 22.3 MHz and f_{th3} = 172.6 MHz) versus frequency within 1 GHz are used to determine τ_{thi} as $\tau_{thi} = 1/2\pi f_{thi} (i = 1, 2, 3)$. The saturation current of this device is 2.07 mA. The relative degradation of drain current per degree temperature change at operation voltage is 1.5 μA/K. The extraction results are listed in Tab.I.

TABLE I
Small-Signal Parameters Extraction Value

Parameter	Extracted Value
$C_{gs}/C_{gd}/C_{ds}/C_{sub}$ (fF)	7.6/2.3/1.7/0.74
$R_g/R_d/R_s$ (Ω)	6/5.4/6.8
R_{ds}/R_{sub} (KΩ)	1.6/14.4

The dynamic thermal impact on Y-parameters of measurement ($V_{ds} = V_{gs} = 0.9V$) are shown in Fig.2 (dot line). The dynamic thermal behavior is modelled both with our method (red line) and method in [4] (blue line). The extracted thermal resistance and thermal capacitance with two method are listed in Tab.II. Our model results show excellent agreement with the measurements both in Y_{21} and Y_{22} respectively, while the method in [4] only have good agreement in Y_{22}. That is because, due to the non-uniform of power dissipation in device, the thermal impact on Y_{21} and Y_{22} are different. Therefore, Y_{21} and Y_{22} cannot be characterized well with the same Zth value. Our model takes into account this difference and uses two associated components (R_{th}/C_{th} and R_t/L_t) to characterize the thermal impact. The results confirmed the validation of our method.

TABLE II
Extracted Thermal Resistance and Capacitance

Parameter	Extracted Value with our method	Extracted value with [4]
$R_{th1,2,3}$ (KΩ)	11.5/22.5/7.4	11.1/22.6/6.5
$C_{th1,2,3}$ (pF)	11.8/0.31/0.13	5.6/0.2/0.057
$R_{t1,2,3}$ (KΩ)	104.5/11.5/19.2	-
$L_{t1,2,3}$ (μH)	14.1K/80.4/19.3	-

As the thermal impedance are extracted, the dynamic thermal impact on device can be characterized. The relationship between static temperature increase in local device ($\Delta T_{dev} = T_{dev} - T_{chip}$) and dissipation power is shown in Fig.3. The temperature rise is quite significant and amounts to 80 K at the highest bias. The dynamic temperature increase in local

device are shown in Fig.4. The dynamic temperature rise with power dissipation increase is consistent with static state. The $Mag\,(\Delta T_{dev})$ remains approximately constant at low frequency from 100 KHz to 150 MHz and decreases exponentially above 150 MHz. It is certain that, for more aggressive channel lengths and finger number than the presented in this paper, the temperature rise will be larger and pose a concern to analog circuit design definitely. On the contrary, the impact of $Phase\,(\Delta T_{dev})$ on device and circuit is little. Therefore, the thermal management algorithms need to be dynamically adjusted according to frequencies and voltages to maximize its performance.

Also, we investigated the thermal impact on 0.13 μm SOI device as comparison. The P_{diss} of FinFET and SOI are comparable and the results are shown in Fig.5. Although the temperature increase in FinFET and SOI at DC bias are similar, the dynamic thermal behaviors are quite different. Hence, it is necessary to characterize and model the dynamic thermal behavior before the thermal management algorithms is determined.

IV. Conclusion

In this work, an analytic method of thermal resistance and thermal capacitance extraction is proposed. The validation of this method is confirmed with the model result of Y-parameters. The dynamic thermal behavior of FinFET is investigated with this method. The results show that, although the saturation current is relatively small, the associated temperature rise is very significant. As comparison, dynamic thermal behavior of SOI is also investigated with this method. The results provide a reliable base for the selection of thermal management algorithms for the circuits carrying various frequency components. The benefits of thermal management can be maximized with the assist of knowledge of dynamic thermal behavior of device.

Acknowledgment

This work was supported by the National Natural Science Foundation of China under Grant 61331006.

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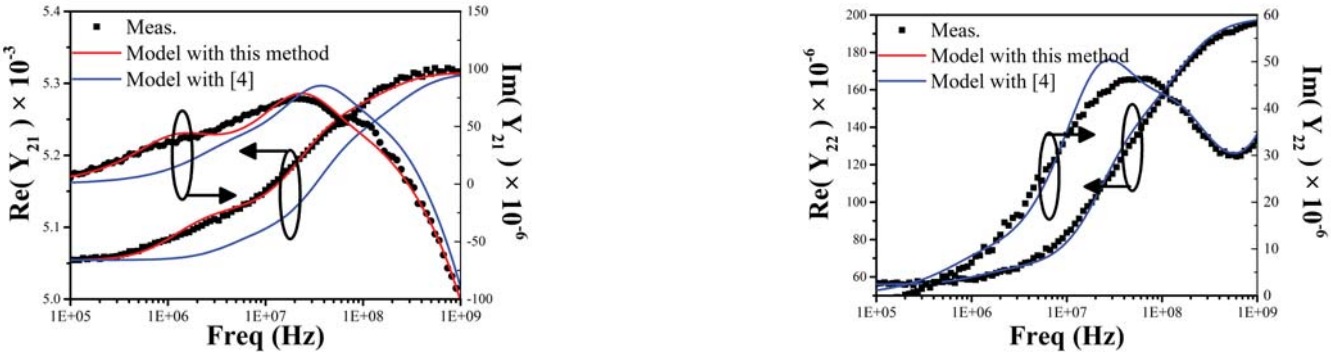

Fig. 2. Model of Y_{21} and Y_{22} with thermal impact

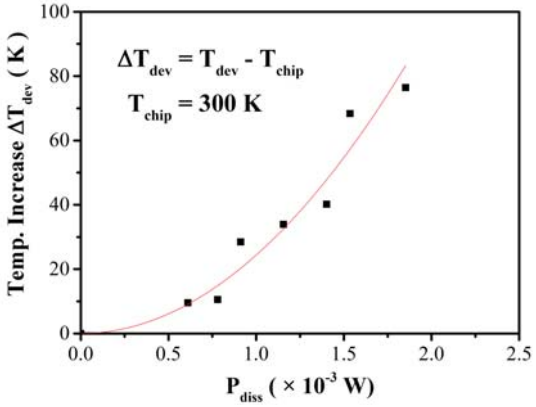

Fig. 3. Static temperature increase with P_{diss} at DC bias

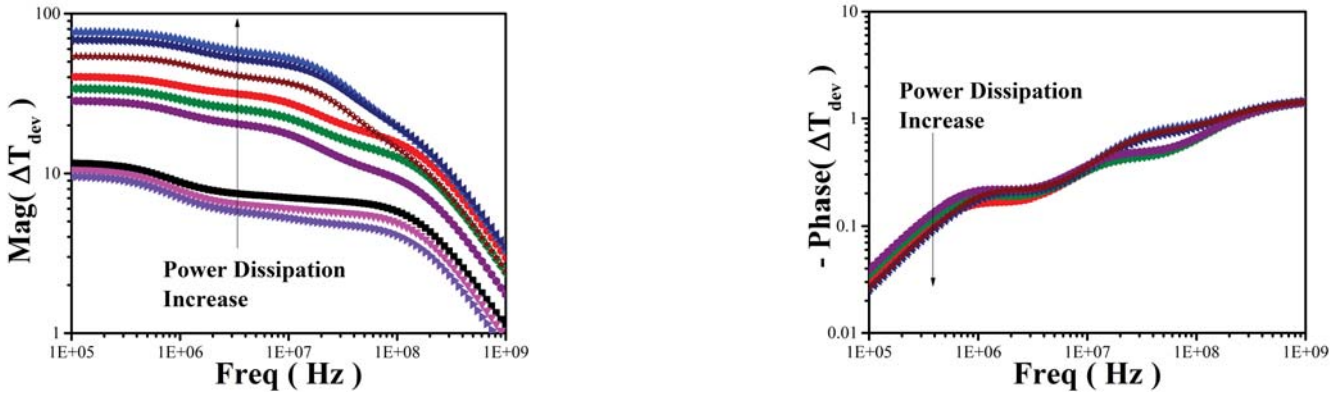

Fig. 4. Dynamic temperature increase with frequency

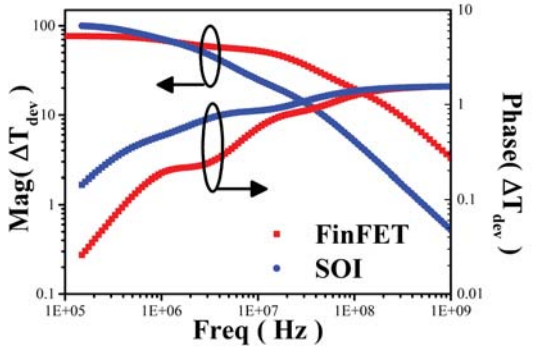

Fig. 5. Comparison of 14 nm FinFET and 0.13 μm SOI of Dynamic temperature increase