Surface and Grain-boundary Effects in Copper interconnects Thin Films Modeling with an Atomistic Basis

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***Abstract*—As interconnects become smaller, their conductivity increases along with the parasitic effects in MOSFET technologies [1]. Therefore, investigating how to model the scattering effects on the nanoscale is important to determine how to engineer interconnects to reduce those parasitic effects. In this work, a fully atomistic method is studied to model the electronic transport properties of copper thin films. For this purpose, a tight binding basis previously benchmarked against first principles calculations [2] is used to describe surface roughness and grain boundary effects on copper thin films with a thickness comparable to the values suggested by ITRS roadmap [3]. In contrast with traditional models, the results show that the tight binding method can quantify those scattering effects at low temperature without fitting any experimental parameters [4], [5].**

***Index Terms*—Grain-boundary, surface roughness, tight binding, copper interconnects**

I. Introduction

The improvements in the density of integrated circuits and device performance have been achieved through a long journey of device downscaling and increase in chip size. The tremendous push of the industry to aggressively scale devices has increased the resistivity of the wire metalization which negatively affects chip performance [6]. Therefore, a careful design of interconnects is essential to reducing these parasitic effects.

These unexpected parasitic effects are driving researchers to explore new materials to reduce the resistivity of interconnects [7], [8]. However, incorporating these materials into interconnect applications is still far from being ready for mass production on an industry level due to variability during fabrication [9] and high temperatures at high bias voltage [10]. Therefore, it is most likely that copper will continue to dominate as the principal material for interconnects in the next few years.

In general, the resistivity of copper interconnects has been successfully captured by two semi-classical models: Fuchs-Sondheimer (FS) [11] and Mayadas-Shatzkes model (MS) [12]. Making use of the Boltzmann's tranport equation, the FS model describes surface roughness and the MS model describes grain boundary effects. Recent technical advances have resulted in fabrication of interconnects below a 50 nm thickness, and well-documented literature shows large discrepancies between the semi-classical models and the experimental observations in this thickness region [13], [14], [15], [16], [17]. These discrepancies show the necessity of constructing a more robust model which goes beyond a semi-classical model, takes quantum effects into account, and can provide a correct description of the electrical resistivity for metal wires below a 50 nm thickness.

Recent efforts have established a fully atomistic approach that can overcome some of the limitations of the semi-classical models. One of the most relevant works has been introduced by M. Cesar et al. [18] who systematically studied the grain boundary effects on twin grain boundaries through a fully atomistic quantum approach. For this purpose, a quantum-transport analysis was used to calculate the resistance of grain boundaries by density functional theory (DFT) with the non-equilibrium Green's function formalism (NEGF) [19]. This parameter-free model was used to obtain the GB contribution and also the reflection coefficient of several copper twin GBs as described by the MS model [5]. The results obtained by this method agree very well with experimental data as shown in Refs. [20], [21]. However, the NEGF+DFT method is limited to modeling very small structures. In order to describe realistic structures as projected by ITRS [22], tight binding methods have been proposed [23] to describe metal wires and films. Additionally, this method has recently been shown to describe grain boundaries effects [24]. Making use of this method, this work proposes a study of the effects of surface roughness and grain boundary effects for copper interconnects at low temperature. These results are also benchmarked against experiments [13], obtaining a reasonable agreement with the reported results. The difference in surface roughness contributions between these modeling results and the experimental values may be because simulation approach does not include a full description of the surface geometry.

II. Method

The resistivity for copper interconnects is calculated in NEMO5 [25] by the NEGF method with a TB basis [ref] making use of the Landauer formalism. The resistivity for copper thin films such as the one shown in Fig.1 is simulated assuming a different number of grains. In this work, each grain is randomly oriented in the out-plane direction with an angle between 1° and 90°. Each grain has a constant length of 5 nm. Each film was constructed with 0.36 nm thickness which is periodic in the x direction. Each configuration has attached leads (source/drain) oriented in the [110] direction. The atomic position of each structure is obtained after an ionic relaxation is carried out by a force-field potential method based

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on the embedded atom model (EAM) [26] as implemented in LAMMPS.

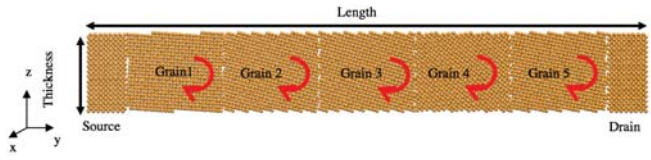

Fig. 1. Side view of one instance of copper interconnect with 5 grains as marked. In general, the copper interconnects are modeled by a system between 1 and 10 grains; each grain is 5 nm in length and 4-10 nm thick. Each particular grain has a specific orientation between 1^0 and 90^0

III. Results

The resistance for copper interconnects for thicknesses (T) between 4 and 10 nm is plotted in Fig.2. In the figure, each point corresponds to the average resistance for 10 different orientations between 1 and 900. The error bars in Fig.2 correspond to the standard deviation for those 10 configurations. The results in Fig.2 clearly show a linear relationship between the number of grains and the resistance. This result is expected since increasing the number of grains implies more grain boundary scattering. Fig.2 also shows that the resistance is larger for thinner copper thin films as reported by Ref. [13]. These results agree with the fact that that thinner structures will be more likely to have scattering against the atoms in the surface. In this study, the surface roughness is the result of the grain boundary orientation, however a realistic surface profile was not included in this study.

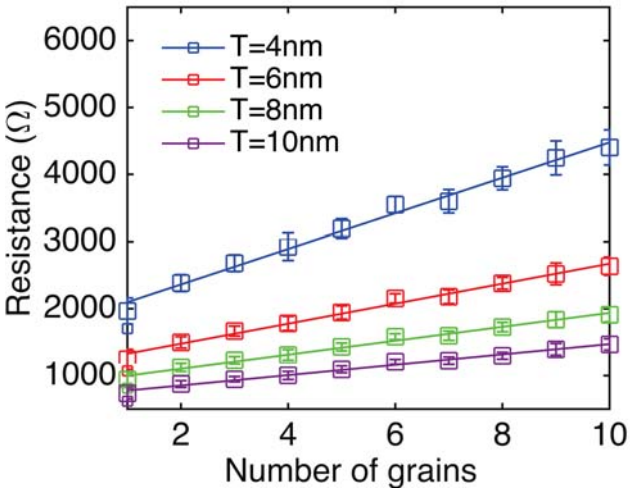

Fig. 2. Resistance for copper interconnects at zero temperature calculated with a TB basis for systems between 1-10 grains. Each point corresponds to a particular configuration with each grain randomly oriented.

In order to quantify the effect of the surface roughness and grain boundaries as a function of the length, the average resistance per device length was computed making use of a linear fit as shown in Eq.1. In this case, the device length corresponds to the number of grains times the grain size (5 nm). The results show a coefficient of determination of 99% for a linear relationship between length of the copper thin films and the average resistance of those orientations.

$$R = \rho \frac{L}{A} + R_c \tag{1}$$

where ρ is the resistivity, L is the total length of the thin film, A is the cross section, and R_c is the contact resistance. The results of the resistivity for a given thickness obtained by Eq.1 are shown in Fig.3

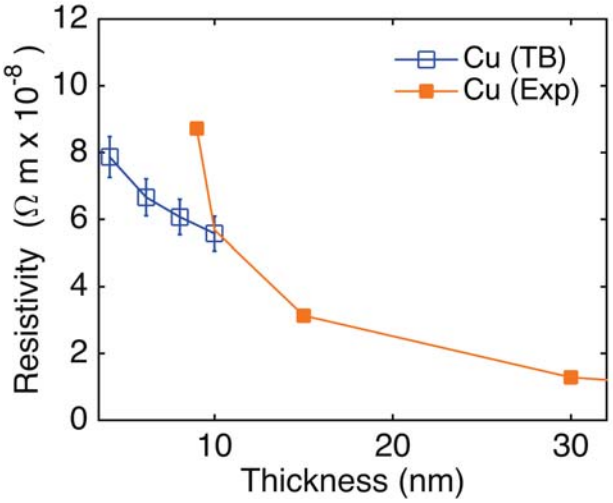

Fig. 3. Resistivity for copper interconnects with different widths. The blue points correspond to the values calculated with our TB models at zero temperature while the solid points correspond to the experimental values in Ref.[13] measured at 1.8 K

Our results show that the TB method describes the same trend as seen in experimental results for copper interconnects [13]. Some differences between the experimental results and the calculated TB values are observed. First, due to computational limitations a constant grain size of 5 nm was assumed, which is expected to be much smaller than the experimental value. Therefore, our grain boundary contribution is much larger than the experimental one. On the other hand, the large jump in the experimental results around 10 nm thickness could be due to an increase in the surface roughness which was not modeled in this work. While it is clear from the results that this TB model can describe the resistivity of copper thin films at low temperatures, some additional details of the surface geometry and the grain boundary size are required to better match the experimental data.

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REFERENCES

[1] C. G. Kang, S. K. Lim, S. Lee, S. K. Lee, C. Cho, Y. G. Lee, H. J. Hwang, Y. Kim, H. J. Choi, S. H. Choe, M.-H. Ham, and B. H. Lee, "Effects of multi-layer graphene capping on Cu interconnects," *Nanotechnology*, vol. 24, no. 11, p. 115707, mar 2013. [Online]. Available: http://stacks.iop.org/0957-4484/24/i=11/a=115707?key=crossref.a947ef1231ba6c115bc35b368ac3a7ce

[2] D. Valencia, E. Wilson, Z. Jiang, G. A. Valencia-Zapata, K.-C. Wang, G. Klimeck, and M. Povolotskyi, "Grain-boundary resistance in copper interconnects: From an atomistic model to a neural network," *Phys. Rev. Applied*, vol. 9, p. 044005, Apr 2018. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevApplied.9.044005

[3] "International roadmap for semiconductors, http://public.itrs.net/reports.html," 2014. [Online]. Available: http://public.itrs.net/reports.html

[4] K. Fuchs and N. F. Mott, "The conductivity of thin metallic films according to the electron theory of metals," *Mathematical Proceedings of the Cambridge Philosophical Society*, vol. 34, no. 01, p. 100, jan 1938. [Online]. Available: http://www.journals.cambridge.org/abstract{_}S0305004100019952

[5] A. F. Mayadas, "Electrical Resisitivity model for polycrystalline films: The case of specular reflection at external surfaces," *Applied Physics Letters*, vol. 14, no. 11, p. 345, 1969.

[6] J. M. Roberts, A. P. Kaushik, and J. S. Clarke, "Resistivity of sub-30 nm copper lines," in *2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM)*. IEEE, may 2015, pp. 341–344. [Online]. Available: http://ieeexplore.ieee.org/document/7325595/

[7] N. T. Cuong and S. Okada, "Suppression of conductivity deterioration of copper thin films by coating with atomic-layer materials," mar 2017.

[8] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Reviews of Modern Physics*, vol. 81, no. 1, pp. 109–162, jan 2009.

[9] C. G. Kang, S. K. Lee, Y. G. Lee, H. J. Hwang, C. H. Cho, J. S. Heo, H. J. Chung, H. J. Yang, S. E. Seo, and B. H. Lee, "Variability and feasibility of CVD graphene interconnect," in *Proceedings of 2011 International Symposium on VLSI Technology, Systems and Applications*. IEEE, apr 2011, pp. 1–2.

[10] C. G. Kang, S. K. Lee, Y. G. Lee, H. J. Hwang, C. Cho, S. K. Lim, J. Heo, H.-J. Chung, H. Yang, S. Seo, and B. H. Lee, "Enhanced Current Drivability of CVD Graphene Interconnect in Oxygen-Deficient Environment," *IEEE Electron Device Letters*, vol. 32, no. 11, pp. 1591–1593, nov 2011.

[11] E. Sondheimer, "The mean free path of electrons in metals," *Advances in Physics*, vol. 1, no. 1, pp. 1–42, 1952. [Online]. Available: https://doi.org/10.1080/00018735200101151

[12] A. F. Mayadas and M. Shatzkes, "Electrical-Resistivity Model for Polycrystalline Films: the Case of Arbitrary Reflection at External Surfaces," *Physical Review B*, vol. 1, no. 4, pp. 1382–1389, feb 1970. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevB.1.1382

[13] "Effects of nanoscale surface roughness on the resistivity of ultrathin epitaxial copper films," *Nanotechnology*, vol. 26, no. 7, p. 075704, feb 2015. [Online]. Available: http://stacks.iop.org/0957-4484/26/i=7/a=075704?key=crossref.8ae4bf44f337a12f6f01588c623cefb5

[14] H.-D. Liu, Y.-P. Zhao, G. Ramanath, S. Murarka, and G.-C. Wang, "Thickness dependent electrical resistivity of ultrathin (," *Thin Solid Films*, vol. 384, no. 1, pp. 151–156, mar 2001. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0040609000018186?via{\%}3Dihub

[15] S. M. Rossnagel and T. S. Kuan, "Alteration of Cu conductivity in the size effect regime," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 22, no. 1, p. 240, jan 2004. [Online]. Available: http://scitation.aip.org/content/avs/journal/jvstb/22/1/10.1116/1.1642639

[16] Y. P. Timalsina, X. Shen, G. Boruchowitz, Z. Fu, G. Qian, M. Yamaguchi, G.-C. Wang, K. M. Lewis, and T.-M. Lu, "Evidence of enhanced electron-phonon coupling in ultrathin epitaxial copper films," *Applied Physics Letters*, vol. 103, no. 19, p. 191602, nov 2013. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.4829643

[17] D. Choi, X. Liu, P. K. Schelling, K. R. Coffey, and K. Barmak, "Failure of semiclassical models to describe resistivity of nanometric, polycrystalline tungsten films," *Journal of Applied Physics*, vol. 115, no. 10, p. 104308, mar 2014. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.4868093

[18] M. César, D. Liu, D. Gall, and H. Guo, "Calculated Resistances of Single Grain Boundaries in Copper," *Physical Review Applied*, vol. 2, no. 4, p. 044007, 2014.

[19] Supriyo Datta, *Electronic transport in mesoscopic systems*. Cambridge: Cambridge University Press, 1997.

[20] T.-H. Kim, X.-G. Zhang, D. M. Nicholson, B. M. Evans, N. S. Kulkarni, B. Radhakrishnan, E. A. Kenik, and A.-P. Li, "Large discrete resistance jump at grain boundary in copper nanowire." *Nano letters*, vol. 10, no. 8, pp. 3096–100, 2010.

[21] L. Lu, Y. Shen, X. Chen, L. Qian, and K. Lu, "Ultrahigh Strength and High Electrical Conductivity in Copper," *Science*, vol. 304, no. 5669, 2004. [Online]. Available: http://science.sciencemag.org/content/304/5669/422

[22] (2009) International roadmap for semiconductors. [Online]. Available: http://www.itrs.net/Links/2009ITRS/Home2009.htm

[23] G. K. Hegde, "Modeling the atomic and electronic structure of Metal-Metal, Metal-Semiconductor and Semiconductor-oxide interfaces," *Theses and Dissertations Available from ProQuest*, jan 2013. [Online]. Available: https://docs.lib.purdue.edu/dissertations/AAI3613136

[24] D. Valencia, E. Wilson, Z. Jiang, G. A. Valencia-Zapata, K.-C. Wang, G. Klimeck, and M. Povolotskyi, "Grain-boundary resistance in copper interconnects: From an atomistic model to a neural network," *Physical review applied.*, vol. 9, no. 4, 2018.

[25] S. Steiger, M. Povolotskyi, H.-H. Park, T. Kubis, and G. Klimeck, "NEMO5: A Parallel Multiscale Nanoelectronics Modeling Tool," 2011. [Online]. Available: http://docs.lib.purdue.edu/nanopub/835

[26] Y. Mishin, M. J. Mehl, D. A. Papaconstantopoulos, A. F. Voter, and J. D. Kress, "Structural stability and lattice defects in copper: Ab initio , tight-binding, and embedded-atom calculations," *Physical Review B*, vol. 63, no. 22, p. 224106, may 2001. [Online]. Available: http://journals.aps.org/prb/abstract/10.1103/PhysRevB.63.224106