The Effect of Etching and Deposition Processes on the Width of Spacers Created during Self-Aligned Double Patterning

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***Abstract*—Topography process simulation has been used to study the interaction of etching and deposition processes for spacer creation for self-aligned double patterning (SADP). For the deposition process, the influence of the layer conformality was investigated. For the etching process, the directionality of the ion flux was varied. The simulations show that by an appropriate combination of the deposition and etching processes, spacers can be created with the desired critical dimension (CD) and a small deviation between the inner and outer spacer CD values. In addition to using the simulation flow for tuning the processes, it can be employed to investigate the influence of variations. As an example, we studied the effect of the across-wafer non-uniformity of the thickness of the deposited oxide layer. For the process sequence considered, the relative change of the spacer CD is 4 to 5 times larger than the relative change of the oxide thickness.**

Keywords—FinFET, self-aligned double patterning, topography process simulation, deposition, etching, process variations

I. INTRODUCTION

For the fabrication of 14 nm node FinFETs based on optical lithography, double patterning is currently the only industrial solution. As discussed in previous work, for instance by Evanschitzky et al. [1], optical lithography is challenged by variations, in particular by those of the focus distance and the illumination dose. These variations lead to variations of the feature size, quantified by the critical dimension (CD).

The basic principle of self-aligned double pattering (SADP) is shown in **Fig. 1**. First, the fin cores are patterned in a carbon layer, for instance using conventional single-step immersion lithography. Next, spacers are generated on these fin cores by deposition (for instance of oxide, which we chose for the simulation study in this work) followed by anisotropic back etching. Similar to other double patterning processes, this process flow results in a duplication of the number of features and in a reduction of the pitch to about one half. Moreover, since the feature size is defined by the thickness of the deposited layer and the thickness removed by etching, very small structures can be obtained, for which the assessment and minimization of the variations is particularly important.

The positions of the spacers have to follow the layout for instance of the SRAM cell. Previous work [2] investigated the impact of variations in the lithography process on the resulting CD values of the spacers. In this paper, we keep the lithography process fixed and vary the etching and deposition processes, in order to study the impact on the resulting CD values of the spacers.

II. SIMULATION METHODOLOGY

A. Deposition Process

For the oxide deposition process we consider a non-conformal process (such as used for instance in [3]) as well as a conformal one (for instance using TEOS).

The simulations of the deposition profiles for the non-conformal process were carried out with the physical deposition simulator DEP3D [4]. For these simulations, the reaction rate of reactive particles for each position on the structure surface is calculated. The particles are assumed to interact only with the surface but not with each other, as their mean free path is far larger than the feature size. After hitting the surface the particle reacts with a probability, which is given by the sticking coefficient. The smaller the sticking coefficient, the more uniform the particles spread over the feature surface and the higher is the conformality of the deposited layer. For modeling of the non-conformal deposition process we assumed a low-temperature oxide (LTO) chemical vapor deposition (CVD) process. For such a process, the sticking coefficient depends on temperature and varies between 0.2 and 0.5 [5]. For our simulation study we used a sticking coefficient of 0.5.

B. Etching Process

Oxide dry-etching mechanisms consist of a number of steps which as a net result lead to the removal of the oxide material [6]. These steps include adsorption of radicals, formation of intermediate species at the surface including passivation layers, and removal of material by purely chemical processes, physical sputtering, or ion-enhanced processes such

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as the ion-enhanced removal of intermediate species from the surface.

Therefore, several parameters are required in the simulation model to fully capture the etching process. For our study we simplified the etching process by assuming that the local value of the ion flux governs the local etch rate. Such a situation occurs for instance if the surface is saturated with intermediate species and the ion-enhanced removal of these species is the rate-limiting step.

The oxide etching process was modeled with the etching simulator ANETCH [7] assuming that the etching of the oxide is governed by the ion flux, as described above, where the angular distribution of the ion flux is modeled as a Gaussian distribution which is quantified by the parameter σ of the distribution. In the etching reactor, σ depends among others on the operation pressure and the substrate bias.

III. Simulation Results

A. Influence of the Process Characteristics

In the simulations, a quasi-2D structure was assumed (as shown in **Fig. 1**). **Fig. 2** and **Fig. 3** show simulation results for both types of deposition processes and for three different values of σ corresponding to a varying directionality of the ion flux for the etching process. An overview of the resulting spacer CD values is given in **Table I**. Choosing an appropriate combination of deposition (conformal vs. non-conformal) and etching (directionality of the ion flux which can be adjusted for instance by changing the substrate bias or the pressure in the etching reactor) allows one for instance to reduce the difference ΔCD between the CD values of the inner and outer spacers. For the processes studied, ΔCD=0 is achieved for conformal deposition and etching with σ=0.05 or σ=0.1, and ΔCD=1 nm is achieved for LTO deposition and etching with σ=0.8.

The CD values of the spacers depend on the conditions of the deposition and etching processes. The CD difference between the inner and the outer spacers is due to the fact that the feature-scale shadowing conditions are different for inner and outer spacers. This influences both the deposition and etching processes, as both depend on the local fluxes of species. For instance, for LTO deposition, when σ of the etching process is changed from 0.3 to 0.8, the width of the outer spacer changes to a larger extent than the width of the inner spacers, see **Figs. 3 (b), (c)**, as due to feature shadowing the broadening of the angular distribution is less visible to the parts of the layer forming the inner spacers than to those parts forming the outer spacers. For the CD values in **Table I**, also the footing of the spacers needs to be taken into account.

The demonstrated methodology allows further refinement by including the link to full equipment simulation for obtaining the boundary conditions (ion and neutral fluxes, angular and energy distribution of ions) depending on the equipment parameters (pressure, power, mass flows, …). In this way, tuning of the deposition and etching processes can be carried out with respect to achieve the desired CD values and a minimized difference between the CD values of outer and inner spacers. For such studies, the usage of advanced optimization programs, such as those based on genetic algorithms [8], will be beneficial.

B. Influence of Variations

In addition to exploiting the simulation flow for tuning the processes to achieve the desired result, the presented methodology can be used to study the impact of process variations on the variations of the CD values of the spacers. For the processes considered in this work, the process variations are likely to be dominated by the changes of quantities across the wafer rather than by changes from wafer to wafer due to temporal variations of the equipment.

1) Etching Process

For the etching process, as mentioned in section II, σ depends among others on the operation pressure and the substrate bias. Its value depends on the full setup of the reactor and the local quantities (electrical, thermal, fluid-mechanical, and chemical). Therefore, σ is not constant across the wafer. To find the variations across the wafer, equipment simulations are needed.

2) Deposition Process

For the deposition process, variations of the sticking coefficient due to variations of the temperature can occur. Besides that, the deposition rate can vary due to a varying temperature or varying concentrations of the species contributing to deposition. Variations of the sticking coefficient or variations of the deposition rate lead to variations of the spacer profiles. To determine these variations across the wafer, equipment simulations or measured data are needed.

As an example for demonstrating the effect of a deposition rate varying across the wafer, we consider a variation of the oxide thickness (defined as thickness in planar regions of the topography) deposited in the CVD process. The other quantities of the simulation flow (σ for the etching process, sticking coefficient for the deposition process) are kept constant.

The simulations considered before (**Fig. 2, Fig. 3**, **Table I**) are based on an oxide thickness of 20 nm. **Table II** shows the CD values of the spacers obtained when this thickness is reduced by 5 % and by 10 %, corresponding to an oxide thickness of 19 nm and 18 nm, respectively. The spacer geometries for the 10 % reduction are shown in **Fig. 4**. This geometry can be compared to **Fig. 3 (c)**, which gives the simulation result for the same deposition and etching parameters, except for the oxide thickness.

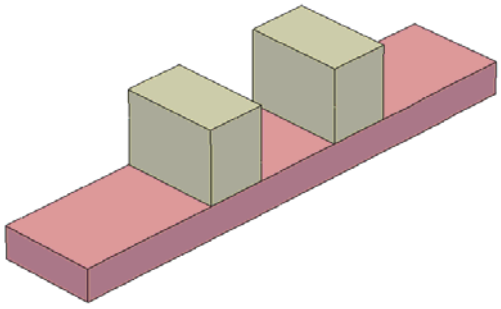
For both 5 % and 10 % reduction of the oxide layer thickness, the relative change of the spacer CD is about 4 to 5 times larger than the relative change of the oxide thickness. For instance, for the 5 % reduction of the oxide layer thickness, the width of the inner spacer changes by 25 % (from 10 nm to 7.5 nm, see **Table II**). In consequence, tight control of the deposition process with respect to uniformity is needed in order to achieve acceptable variations of the spacer CD which determines the CD of the fin to be etched using the spacer as a mask.

TABLE I. CD VALUES (NANOMETERS) FOR INNER SPACERS / OUTER SPACERS FOR DIFFERENT DEPOSITION AND ETCHING PROCESSES

	σ = 0.05	**σ = 0.1**	**σ = 0.3**	**σ = 0.8**
Conformal deposition	18.5 / 18.5	18.5 / 18.5	24 / 18	fail / 14.5
LTO deposition	12 / 16	12 / 16	10 / 14	10 / 9

TABLE II. CD VALUES (NANOMETERS) FOR INNER SPACERS / OUTER SPACERS FOR DIFFERENT THICKNESSES OF THE LTO LAYER USED FOR SPACER CREATION

	d=20 nm σ = 0.8	**d=19 nm σ = 0.8**	**d=18 nm σ = 0.8**
LTO deposition with thickness d	10 / 9	7.5 / 7	6 / 5



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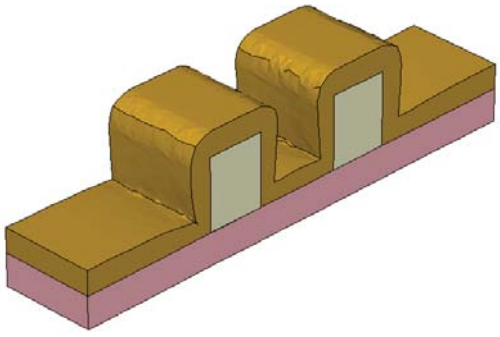

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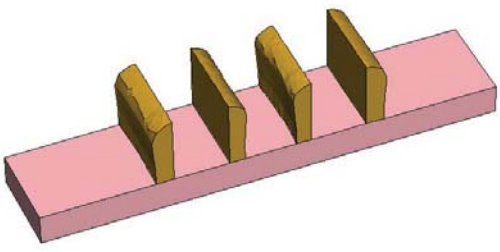
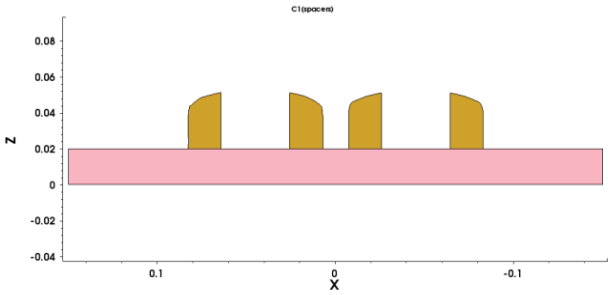
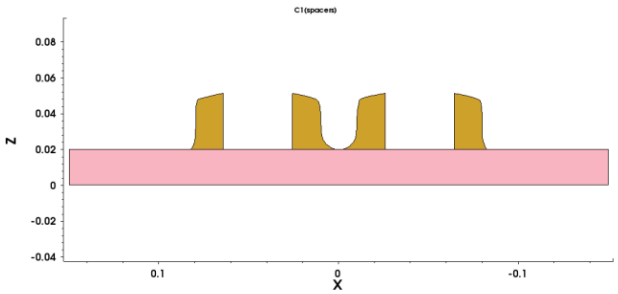


(c)

Fig. 1. Sequence for creating the SADP spacers. (a): Carbon lines as patterned by the lithography step. (b): Deposition of an oxide layer. (c): Back etching to create the spacers.



(a)



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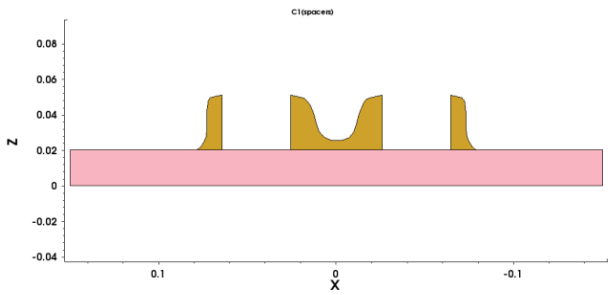
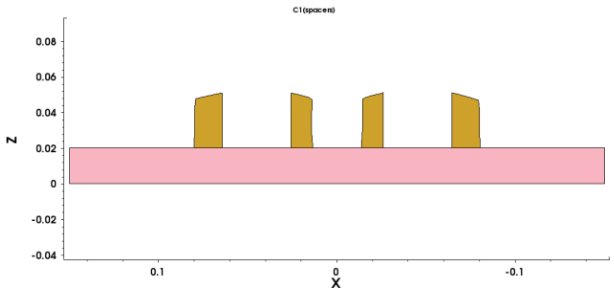
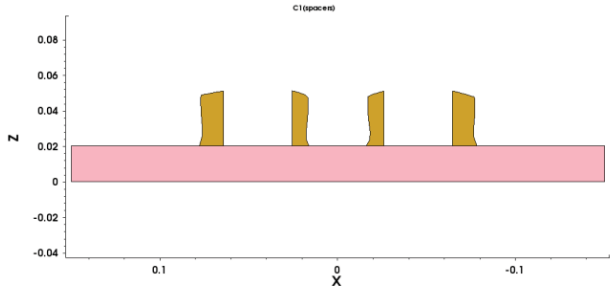


(c)

Fig. 2. Spacer geometries for a conformal deposition process and an etching process with varying σ of the angular flux distribution of the ions (a: σ=0.05, b: σ=0.3, c: σ=0.8).



(a)



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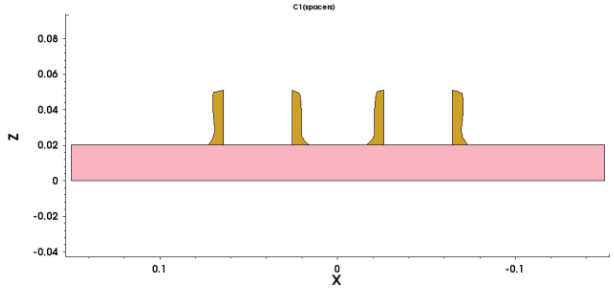

(c)

Fig. 3. Spacer geometries for an LTO deposition process and an etching process with varying σ of the angular flux distribution of the ions (a: σ=0.05, b: σ=0.3, c: σ=0.8).

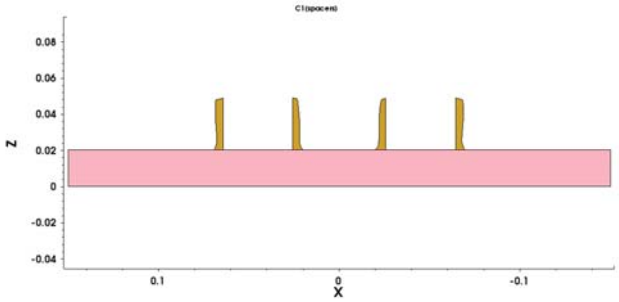

Fig. 4. Spacer geometry for an LTO deposition process and an etching process with σ=0.8 where the thickness of the layer deposited by CVD is reduced by 10 % compared to the process for which the result is shown in Fig. 3 (c).

IV. Conclusions

By means of topography process simulation, we have demonstrated the interaction of etching and deposition processes for spacer creation for SADP. For the deposition process, we investigated the influence of the layer conformality. For the etching process the directionality of the ion flux was varied. By an appropriate combination of etching and deposition, spacers can be created with the desired CD and a small deviation between the inner and outer spacer CD values.

In addition to employing the simulation flow for tuning the processes, we can use it for investigating the influence of variations. As an example, we studied the influence of the across-wafer non-uniformity of the thickness of the oxide deposited by CVD. For the process sequence studied in our examples, the relative change of the spacer CD is 4 to 5 times larger than the relative change of the deposited oxide thickness. Therefore, tight control of the across-wafer non-uniformity of the oxide thickness is required. In this context, simulations can support the determination of fin CD variations, when the deposition uniformity is known from measurements or equipment simulations.

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