A Carrier Lifetime Sensitivity Probe Based on Transient Capacitance: A novel method to Characterize Lifetime in Z2FET

F. Adamu-Lema
School of Engineering
University of Glasgow
Glasgow, United Kingdom
Fikrua.adamu-lema@glasgow.ac.uk

M. Duan
School of Engineering
University of Glasgow
Glasgow, United Kingdom

V. Georgiev
School of Engineering
University of Glasgow
Glasgow, United Kingdom

Prf. A. Asenov
School of Engineering
University of Glasgow
Glasgow, United Kingdom

I. INTRODUCTION

The Z2FET [1] (Fig.1) has a potential for application in memory cells without connection to external charge storage components. Since its invention and experimental demonstrations, essential progress has been made in analyzing its transient and DC properties via electrical characterization [2] and TCAD simulations [3, 4, 6]. However, until now no attempt has been made to investigate the transient capacitance (*C-t*), which, can be used to characterize the carrier lifetime ruling the dynamic operation of the Z2FET. The carrier lifetime is one of the most important parameters, which directly determines the Z2FET retention time (Fig. 2). In this work, using simulation, we analyze the impact of carrier lifetime on transient capacitance in the gated region of the Z2FET (Fig.1) in order to provide guidelines of its experimental measurement and characterization.

II. THE DEVICE AND METHODOLOGY

The fabricated testbed of Z2FET has silicon body thickness (t_{Si}=7nm) and a buried oxide of 25 nm. In the simulation domain, the bulk silicon (substrate) is set to be t_{Bulk}=500 nm (Fig. 1). The Synopsys [5] TCAD tool Sentaurus Device simulator was used in this work. The simulation deck is calibrated to the experimental data as presented in [2-4]. Since the thickness of Si, both the t_{Si} and t_{Bulk} in the structure, has an impact on the transient capacitance, we first separate the front gate SOI section of the device from the whole structure.

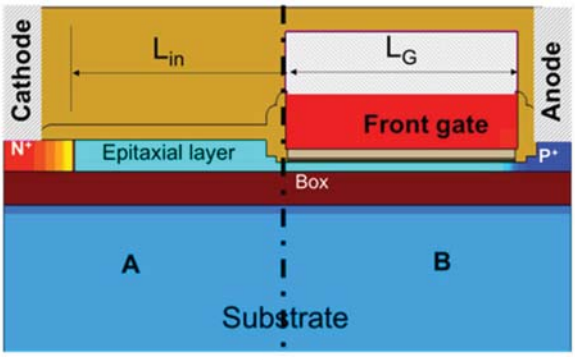

Fig.1: Generic device structure showing geted (B) SOI section and ungated (A).

In order to understand the effect of a carrier lifetime in the Si-body and SOI substrate, different lifetimes (τ_{tsi}, τ_{bulk}) are used respectively in the simulations. Two different scenarios have been considered: Firstly, the Si-body and the substrate thicknesses are kept the same as in the simulation deck. Secondly, we have considered 150 nm Si-body thickness and 500nm substrate thickness. For transient capacitance simulation, we apply front gate voltage (pulse) of V_{FG}=2 V at t=0 s and run the transient capacitance simulations. For comparison, the total gate capacitance is calculated using equations (1) presented on the following page.

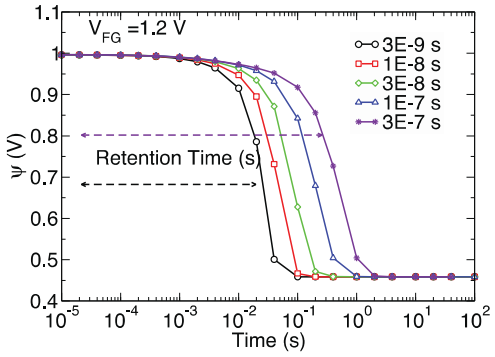

Fig. 2: Figure of Merit: Correlation of life time effect and retention time.

III. DISCUSSION

The generic device structure is illustrated in Fig.1 , which shows the two main regions of the Z2FET device. The gated region and the ungated region are denoted by (L_G) and L_{in} respectively which control the electron and hole potential barriors by blocking holes and electrons which are enjected from the highly doped Anode and Cathode terminals respectivly [6]. The channel under the front gate is very low doped. For normal memory operation of an n-type Z2FET, both gates are biased at V_{FG}>0 and V_{BG}<0 respectively.

Fig.2 shows the retention time as a function of carrier life time that is defined in the whole device structure [7]. Obviously, carriers lifetime can directly affect the key figure of merit of Z2FET, like retantion time. Therefore, exploration of an effective method to characterize a carrier lifetime is of great importance.

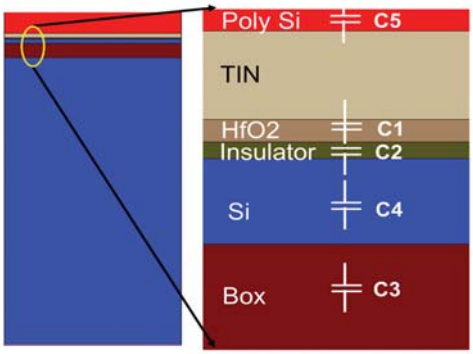

Fig.3: Illustration of vertical gate capacitors in the gated SOI section B as

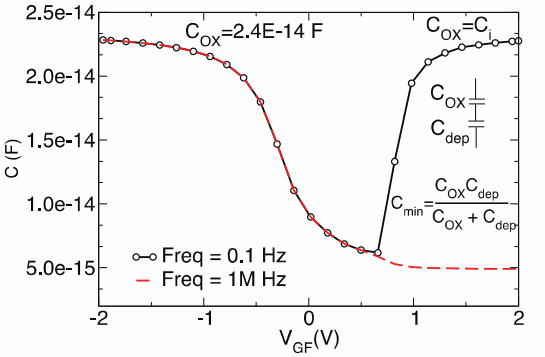

Fig.4: Simulated C-V, where the simulated C_{ox}=2.4E-14F, which is comparable with the the calculated value of 2.6E-14 F, value (see Fig 8)

A tipical C-V curve and inversion capacitence as a function of frequency are shown in Fig. 4 and 5 respectivly. The transient capacitance simulation depicting the transient capacitance values at deep depletion (t<10 µs) and after getting back to the equilibrum condition (C_{min}) is presented in Fig.6

For the original physical thickness of the silicon body and bulk, the simulation data shows that transient capacitance curve doesn't change with different carrier lifetimes in the Si body (Fig.7d), but it is sensitive to the change in carrier life-time in the bulk (Fig.7c). The transient response of the MOS capacitance to a pulse in V_{GF} can be defined by using differential equations [9] given in Fig 8(2, 3) for Si-body and substrate regions respectively. The equation relates the rate of change of in depletion layer to the rate of surface electron density in the inversion region. The total rate of change in surface density will be the contribution from both equations.

Closer look at equation (2 and 3) in Fig. 8 below shows that the rate of change of surface electron density is near zero in the thin silicon-body (Fig. 7). The main reason for this is that, the depletion width in thin body SOI is near constant (it is fully depleted all the time). Further observation of the electron profile in Fig. 7(a, b) also show that, the depletion width in the Si-body, before (W_{Tsi}) and after recovering to the C_{min} (W_{fsi}) is almost the same.

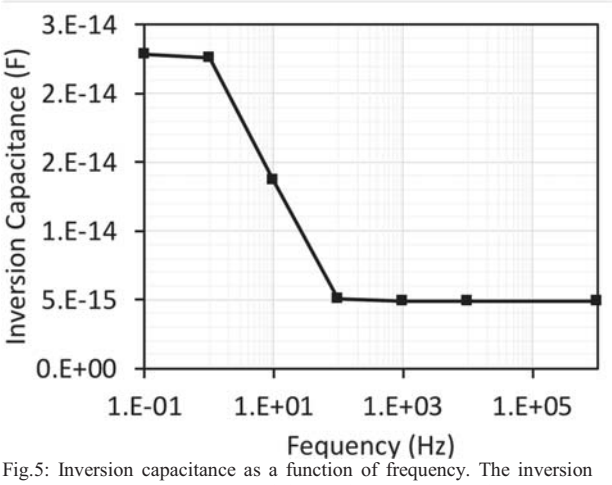

Fig.5: Inversion capacitance as a function of frequency. The inversion capacitance starts at V_{FG}=1 V and the graph is extracted at the maximum capacitance where V_{FG}=2 V.

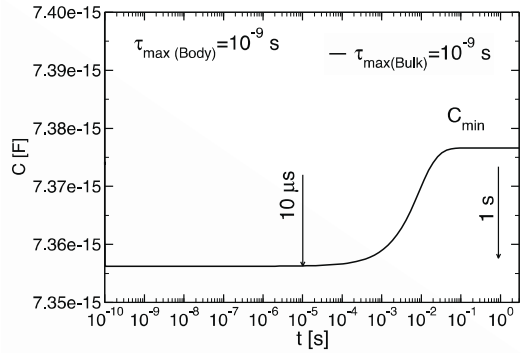

Fig. 6: Recovery of the capacitance from deep depletion ($W_{initial}$) to the final (W_{final}) where the capacitance is comparable to C_{min} as shown in Fig. 4 at high frequency and the calculated value is well approximated by the simulation result ~7.4E-15F (see equation 1 below).

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \cdots$$

$$C_1 = \frac{\varepsilon_{HK}}{t_{HK}} \quad C_2 = \frac{\varepsilon_{in}}{t_{in}} \quad C_3 = \frac{\varepsilon_{sio2}}{t_{sio2}} \qquad (1)$$

$$C_d = \frac{A\varepsilon_{Si}}{W_d}, C_{ox} = C_i = C_T = 2.6 \times 10^{-14}\, F$$

$$C_{min} = \frac{C_{Ox} \times C_d}{C_{Ox} + C_d} = 7.4 \times 10^{-15} F$$

$$\frac{dN_S}{dt} = \frac{n_i}{2\tau_1}(W_{TSi} - W_{fSi} + C) \qquad (2)$$

$$\frac{dN_S}{dt} = \frac{n_i}{2\tau_2}(W_{Bulk} - W_{fB} + C) \qquad (3)$$

n_i - intrinsic carrier concentration
N_s - surface density of electrons in the inversion layer
τ - The carrier life time
W_{Bulk}, W_{Tsi} - initial depletion width (Deep depletion)
W_{Bf}, W_{fsi} - final depletion layer width in equilibrium
g - constant rate of carrier generation per unit area

Fig.8: Equation (1) used to estimate the gate oxide capacitance. The transient response of the MOS capacitance to a pulse in V_{GF} can be defined by deferntial equations in 2 and 3 [9,10].

On the other hand, the electron density in the substrate is proportional to the change of the width from deep-depletion condition ($W_{B\text{-initial}}$) to the depletion layer at equilibrium (W_{Bf}) in which the capacitance recovers to the theoretical capacitance level (C_{min}). Clearly, the carrier lifetime in the bulk has much stronger effect than the lifetime in the thin Si-body of the Z2FFT structure.

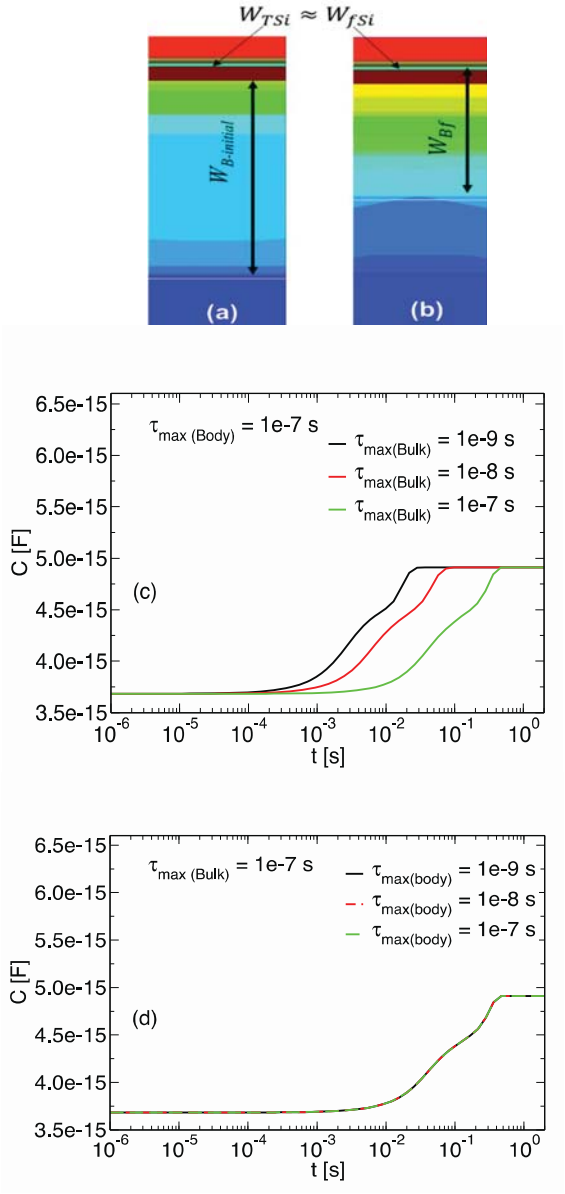

Fig. 7 Charge distribution at different simulation times for Si body thickness and bulk of 7 nm and 500 nm respectively. The *C-t* curve (please see c) shows the effect of life time on the *C-t* profile. Keeping constant the life time in Si-body (τ_{tsi}) and changing life time in the bulk (τ_{bulk}) does affect the *C-t* curve as shown in top-right. While keeping constant τ_{bulk} and sweeping across τ_{tsi} doesn't affect the transient capacitance (please see d).

In order to highlight, that the carrier life time in the bulk is more dominant, we have performed transient capacitance simulation for different thickness combination than in the previous setup shown in Fig. 7. So, by increasing the thickness of the silicon thin-body from 7 nm to 150 and kept the substrate to 500 nm as shown in Fig.9, we observe that the transient capacitance is still changing more when the carrier lifetime in the substrate is varying from 10^{-7} s to10^{-9} s (Fig. 9a).

As a result of an increase in Si-body thickness, the change of lifetime in Si-body start to have impact (Fig. 9b) when compared data in Fig. 7d, which implies that carrier lifetime in both sections becomes significant and the significance is proportional the thickness in both sections. This is consequential to transient capacitance, and eventually retention time of Z2FET.

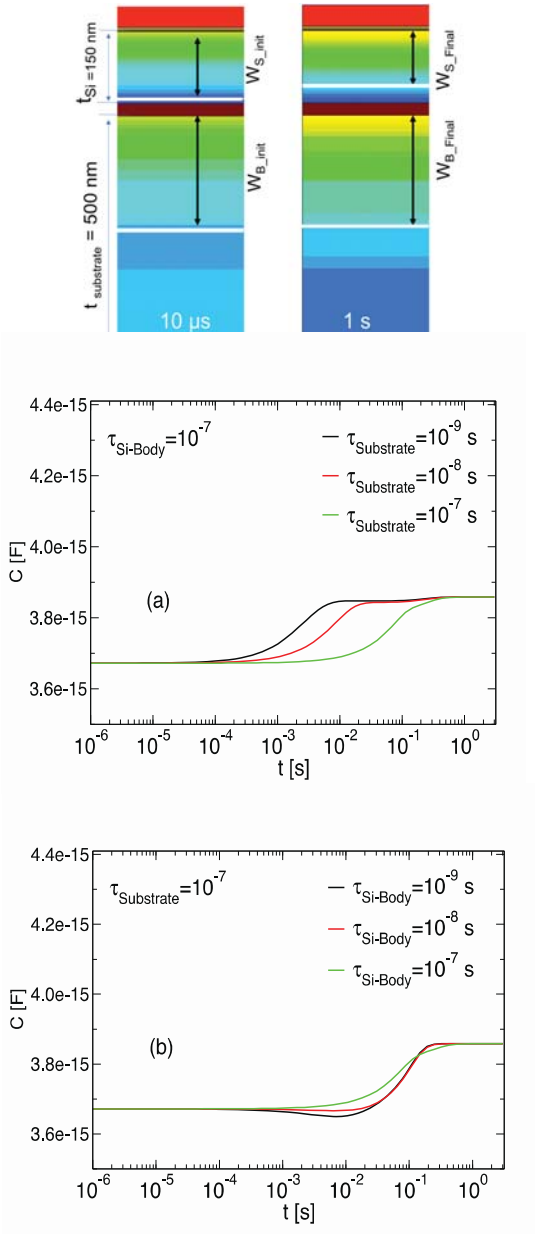

Fig.9 The depletion width recovered from deep depletion ($W_{initial}$) to W_{final} at t=1s to reach C_{min}.

SUMMARY

In this work, we have reported the correlation between the retention time, carrier lifetime and transient capacitance properties in the Z2FET. The carrier's lifetime plays an important role in Z2FET performance. Retention time of the Z2FET is dominated by the lifetime in the substrate. The traditional transient C_{min} method has been adopted to simulate Z2FET's carrier's lifetime. Our results show that the overall vertical capacitance of Z2FET is dominated by the parasitic substrate capacitor. In order to effectively characterize/measure carriers' lifetime of the channel Si-body thickness should be adjusted with respect to substrate thickness.

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REFERENCES

[1] J. Wan, C. Le Royer, A. Zaslavsky and S. Cristoloveanu. "Progress in Z2-FET 1T-DRAM: Retention time, writing modes, selective array operation, and dual bit storage., *Solid-State Electronics, Volume 84, June 2013, Pages 147-154.*

[2] K. C. Huang et al. "A High-Performance, High-Density 28nm eDRAM Technology with High-K/Metal-Gate.", *IEEE International Electron Devices Meeting (IEDM),* Washington, DC, pp. 24.7.1-24.7.4, 2011.

[3] M. Bawedin, S. Cristoloveanu, and D. Flandre, "A capacitorless 1TDRAM on SOI based on dynamic coupling and double-gate operation," *IEEE Electron Device Letters*, VOL. 29, pp. 795-798, 2008.

[4] C. Navarro, *et al*. "Extended Analysis of the Z2 -FET: Operation as Capacitorless eDRAMIEEE", *IEEE Transaction On Electron Devices*, VOL. 64, Nov. 2017

[5] Synopsys Inc. Sentaurus Device User Guide, version K-2015.06, 2015.

[6] S. Cristoloveanua,et al., "A review of the Z2FET 1T-DRAM memory: Operation mechanisms and keyparameters"*, Solid State Electronics*, 143 (2018) 10–19

[7] M. Duan, F. Adam-Lema, B. Cheng, C. Navarro, X. Wang, V. P. Georgiev, F. Gamiz, C. Millar, A. Asenov,"2D-TCAD Simulation on Retention Time of Z2FET for DRAM Application", *SISPAD, pp. 325,* 2017

[8] F. Adamu-Lema ; M. Duan ; C. Navaro ; V. Georgiev ; B. Cheng ; X. Wang ; C. Millar ; F. Gamiz ; A. Asenov, "Simulation based DC and dynamic behaviour characterization of Z2FET" *SISPAD*; PP. 317 ,2017

[9] W. M. Gosney, "Dynamic storage time measurements on metal oxide semiconductor-random access memory circuits," *in Lifetime Factors in Silicon, ASTM STP 712, Amer. SOC. Testing and Materials*, pp.58-70, 1980.

[10] Z. Radzimski, J. Honeycutt, and G. A. Rozgonyi "Minority -Carrier Lifetime Analysis of Silicon Epitaxy and Bulk Crystals with Nonuniformly Distributed Defects", *IEEE Transaction On Electron Devices*,, VOL. ED-35, NO. I Jan 1988