Transistor Optimization with Novel Cavity for Advanced FinFET Technology

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***Abstract*—We present a novel cavity engineering work -- we named this cavity as dual-curvature cavity, which improves pFET electrical performance. This new cavity shape design minimizes the source/drain leakage penalty from deeper cavity depth while enabling the transistor performance benefits from larger eSiGe. In addition, this new cavity shape minimizes the penalty of deeper cavity on SDB (single diffusion break) devices through minimizing the facet effect in SDB structure. This work demonstrates that this new cavity shape could improve p-type transistor performance by 4% on top of the Fin shape optimization.**

Keywords: Dual-curvature cavity, FinFET, SDB, DDB

I. INTRODUCTION

Larger eSiGe benefits transistor performance as it not only enhances mobility through placing stronger strain on channel but also reduces contact resistance through providing larger contact area [1-6]. Since eSiGe volume is linearly correlated to cavity depth, deeper cavity depth is expected to benefit transistor performance from larger eSiGe volume. However, deeper cavity opens up extra junction leaking path that increases the S/D leakage current. Meanwhile, the SDB device, as shown in Fig. 1, provides the advantage of further die area reduction by about 10% compared to DDB (double diffusion break) device. However, the SDB device comes with facet eSiGe. It leads to smaller eSiGe and make the transistor vulnerable to short channel effect (SCE) as result of the lateral encroachment of S/D implantation. In advanced FinFET technology, the narrow FIN is adapted to suppress the transistor leakage. However, narrower FIN leads to smaller eSiGe width which, on the other hand, compromises transistor performance. In this paper, a novel cavity is presented that enables larger eSiGe on the narrower FIN and co-optimizes the DDB and SDB device performance.

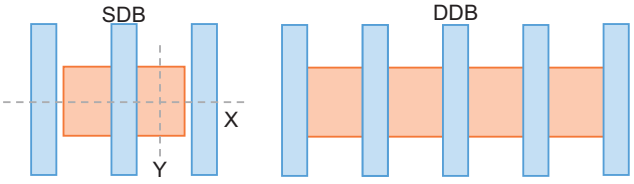
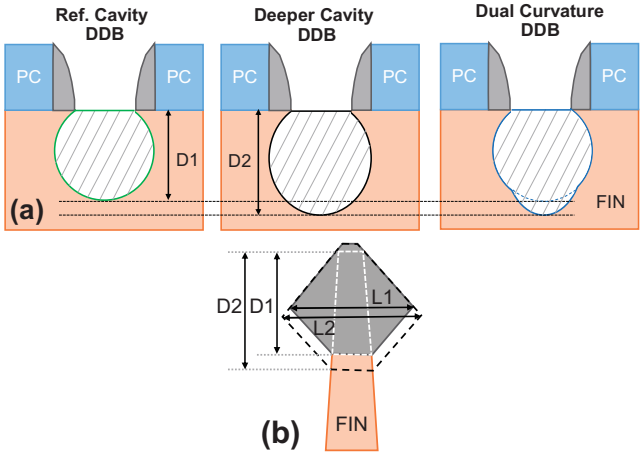


Fig. 1: the schematic of SDB and DDB layout. The vertical blue rectangle array is gate and the larger orange rectangle is active.

II. EXPERIMENTS

This work is conducted in a mature 14nm FinFET production line. After Fin and dummy poly gate formation, spacer is deposited. Then, the area for p-type transistors is patterned and a ball-shaped cavity is formed. In this work, both the deeper cavity and the reference cavity are conventional ball-shaped cavity, but the deeper cavity is formed with longer etch time to have cavity depth deeper while maintaining the same cavity proximity. A dual-curvature cavity is formed based on the reference ball-shaped cavity, through adding an additional anisotropic etch process to form a new smaller cavity in the gate canyon at the bottom of the reference ball-shaped cavity. Fig. 2(a) shows the schematic drawing of a deeper cavity, a dual-curvature cavity and the reference cavity on DDB devices. Fig. 2(b) shows that eSiGe volume increases linearly with cavity depth and comparable eSiGe volume is expected between deeper cavity and dual-curvature cavity in this work since their cavity depth are comparable. Fig. 2(c) shows the corresponding eSiGe on SDB devices. Facet EPI occurs because there is no sidewall seed layer on one side of the cavity. The starting point of eSiGe growth is comparable between dual-curvature cavity and the reference cavity, and both are higher than that on the deeper cavity. Fig. 3 shows the TEM images of DDB and SDB of dual-curvature cavity after cavity etch.



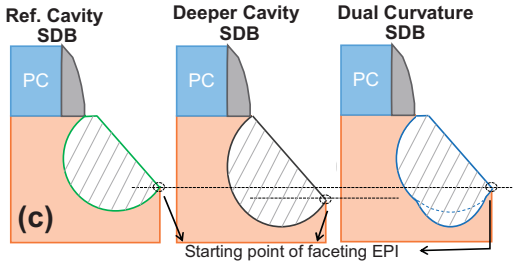


Fig. 2: (a) the X-cut schematics of reference ball-shaped cavity deeper cavity and dual-curvature cavity. D1 and D2 are the corresponding cavity depth; (b) the Y-cut schematic of corresponding eSiGe in (a); (c) the schematics of eSiGe on the corresponding SDB devices on wafers with the three cavities in (a).

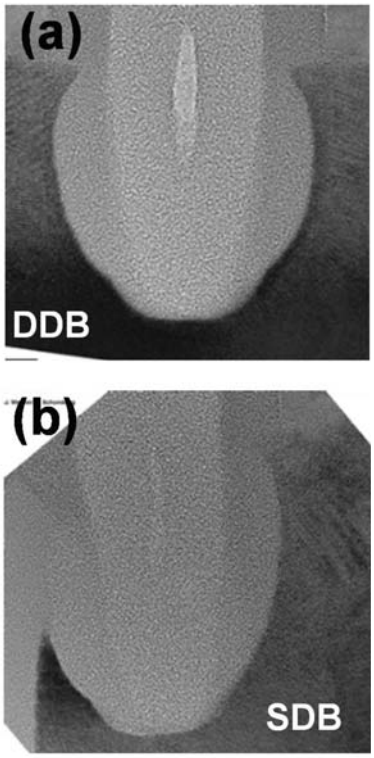


Fig. 3: TEM images of Dual curvature cavity post cavity etch (a) DDB and (b) SDB

III. RESULTS AND DISCUSSION

Fig. 4 shows the ET response of DDB and SDB devices to cavity depth split with ball-shaped cavity. In Fig. 4(a), the DDB device performance improves 3% as cavity goes deeper, which is attributed to the eSiGe volume increase. For SDB devices in Fig. 4(b), I_{off} increases faster than I_{on} as the cavity goes deeper and leads to a 4% performance degradation. Fig. 4(c) shows the DDB and SDB DIBL delta between the reference cavity and the deeper cavity. Higher DIBL degradation in SDB devices suggests that SDB device is more prone to SCE, which is attributed to deeper dopant in source/drain implantation in SDB devices as a result of the facet EPI shown in Fig. 2(c).

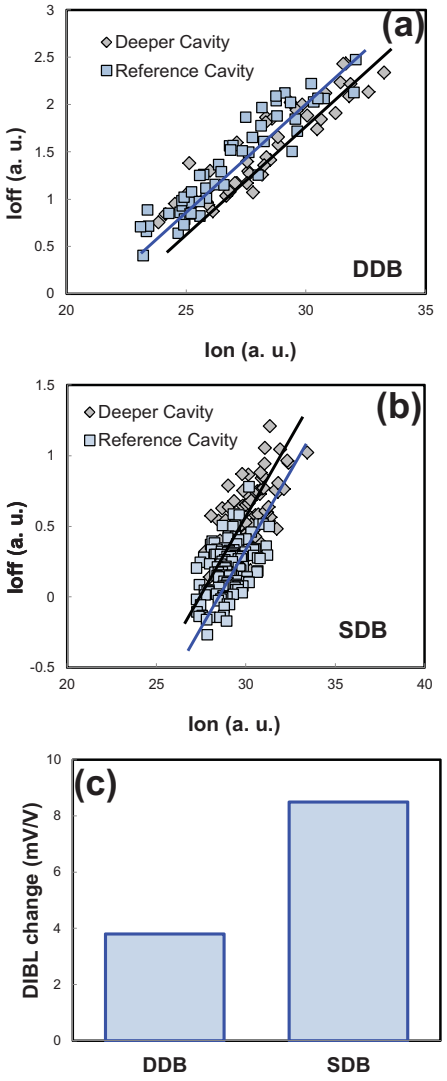
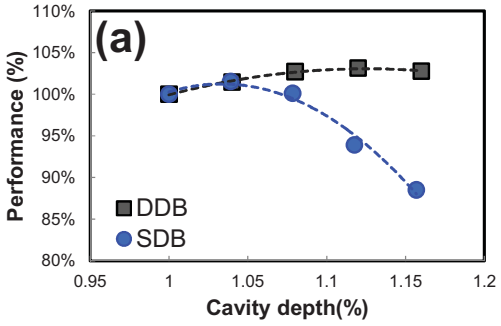


Fig. 4: Ion vs. Ioff for (a) DDB and (b) SDB devices. (c) DIBL increase from the reference cavity to the deeper cavity.

The plots of Fig. 5-7 are from calibrated TCAD simulation work. As cavity depth goes deeper, SDB device performance decreases while DDB devices keeps slightly increase. Fig. 5(b) shows DIBL is a function of cavity depth. The DIBL of SDB device increases faster than that of DDB due to the facet eSiGe profile leading to more junction encroachment by deeper S/D implantation. The reference cavity depth in this work has already been well optimized to a sweet spot that maximizes the device performance on DDB devices and minimizes the impact on SDB devices.



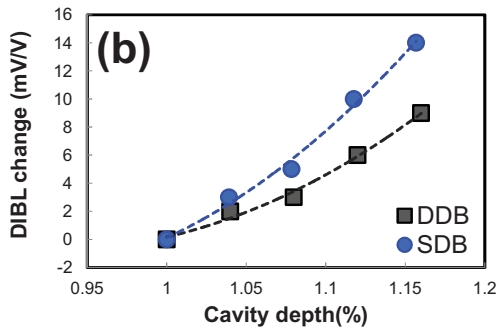


Fig. 5: (a) Device performance and (b) DIBL change as a function of cavity depth with ball shaped cavity based on TCAD simulation

Fig. 6 shows DDB devices with dual-curvature cavity could achieve a higher device performance than the reference ball-shape deeper cavity and the improvement is from DIBL reduction. Compared with deeper cavity, dual-curvature cavity enjoys the benefits from a comparable eSiGe volume increase but suffers less from the leakage increase at the cavity bottom due to the larger separation between cavity and gate (Fig. 2(a)). That advantage is maintained at narrower Fin devices. The corresponding plots for SDB devices are shown in Fig. 7 (a) and (b). The rolling down of device performance suggests the cavity depth is deeper than the sweet point for SDB devices. As expected, narrower Fin improves DIBL and thus the device performance through better SCE control. In both Fin groups, dual-curvature cavity demonstrates a better resistance to performance and DIBL degrade as cavity depth goes deeper, which is attributed to the less facet EPI growth that reduced implementation depth. Fig. 7 (c) shows corresponding leakage contour plots, showing dual-curvature cavity and narrower Fin effectively suppress the leakage.

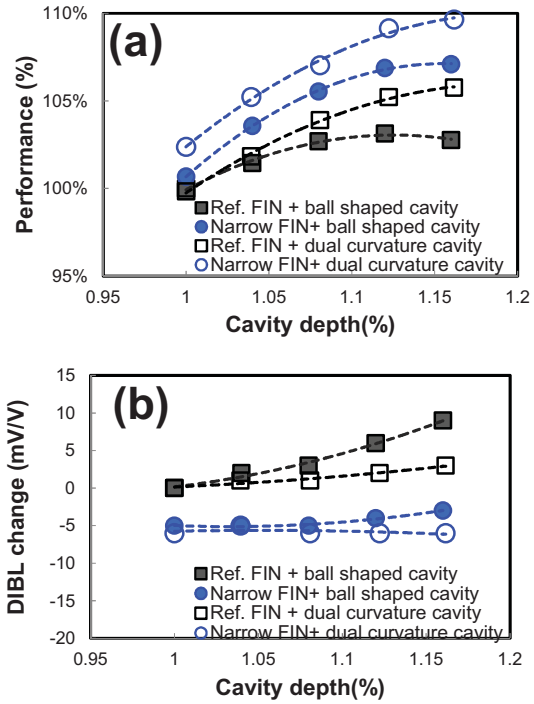


Fig. 6: The DDB device performance and DIBL as a function of cavity depth from calibrated TCAD simulation work.

Fig. 8 shows the electrical data of the reference ball-shaped cavity on the reference Fin and the narrower Fin, as well as the dual-curvature cavity on the narrower Fin. For DDB devices, 10% performance improvement is observed on narrower Fin and additional 4% performance improvement was observed on dual-curvature cavity split. While for SDB devices, 13% performance improvement is observed on narrower Fin and no further device degradation was observed on dual-curvature cavity split when cavity depth go deeper.

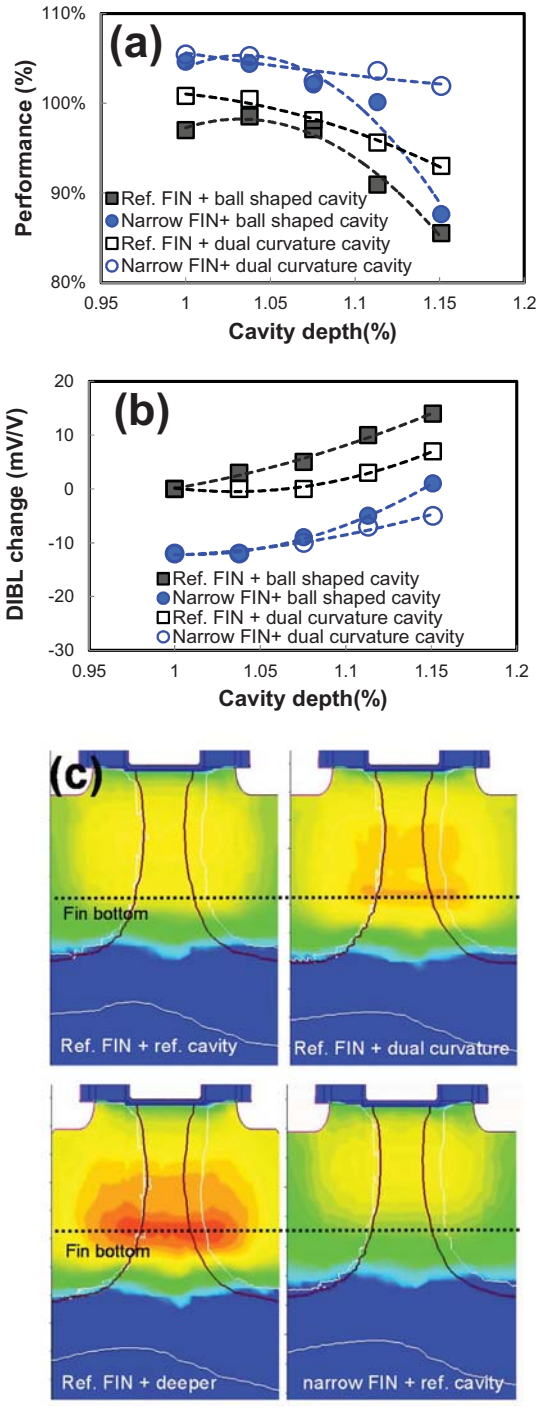


Fig. 7: (a) The SDB device performance and (b) DIBL as a function of cavity depth from calibrated TCAD simulation work. (c) Leakage contour plots for deeper cavity, dual-curvature cavity and narrow Fin.

To sum up, dual-curvature cavity could boost device performance for DDB performance while maintaining SDB

device performance and that benefit is maintained on a higher performance baseline as Fin goes narrower.

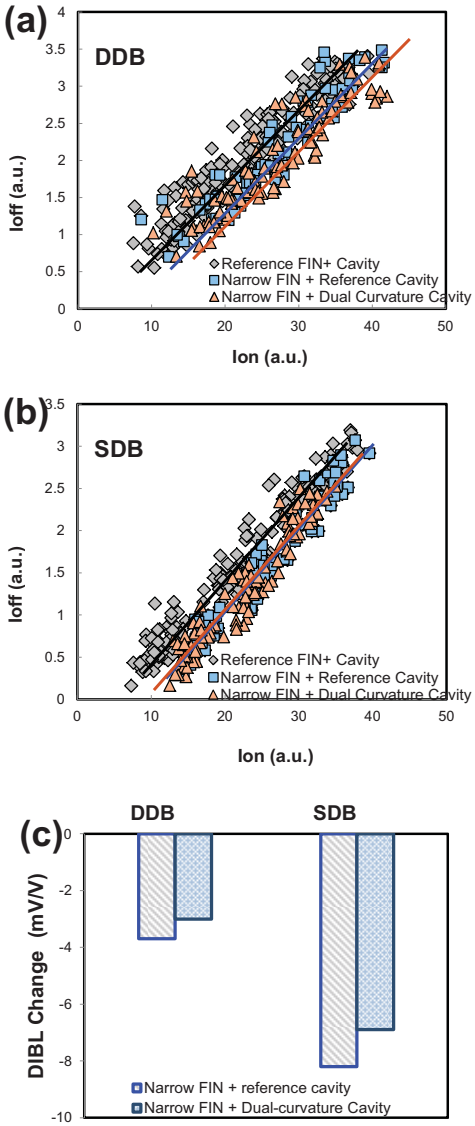


Fig. 8: Ion vs. Ioff for (a) DDB and (b) SDB devices and (c) DIBL of DDB and SDB devices.

IV. SUMMARY

In this work, we present a novel dual-curvature cavity that could improve device performance on top of a well optimized ball-shaped cavity. Device performance is further improved as Fin goes narrower and the advantage of dual-curvature cavity is maintained in the new Fin baseline.

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