14nm FinFET Device Boost via 2nd Generation Fins Optimized for High Performance CMOS Applications

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***Abstract*—3D TCAD (Technology Computer Aided Design) process and device simulation is used to show that taller and thinner fins at the 14nm device node enable significant DC and RO performance gains for both nFET and pFET short channel devices through improvement in charge inversion and leakage current control. In particular, simulations identify a maximum in the DC and RO performance as a function of the Fin Ratio, defined as the top fin width (TCD) over the bottom fin width (BCD). At long channel, TCAD simulation demonstrates that mobility degradation observed in nFET hardware devices (but not in pFET devices) is due to the effect of quantum confinement in the fin.**

Keywords—fin dimension, fin ratio, DC and RO performance, mobility, charge inversion, leakage control, quantum confinement

I. INTRODUCTION

To deliver a device technology platform with improved performance, many critical features in the device must be optimized simultaneously. These include optimization of the fin profile, cavity depth and proximity, S/D implantation and epitaxy, as well as contact resistance reduction. In this paper, TCAD simulations show the performance improvement obtained using the second generation fin profile at the 14 nm node, in which the fin height (FH) is increased and the critical dimensions at the fin top (TCD) and fin bottom (BCD) are reduced relative to the first generation fin profile. Earlier TCAD simulations demonstrate that the ideal fin shape for optimal short channel performance is rectangular [1]. However, because of manufacturing constraints, this shape is difficult to achieve and practical fin shapes are actually trapezoidal. Therefore, in order to optimize the DC and AC performance of short channel devices, TCAD simulation is needed to tune the Fin Ratio (TCD/BCD). Also, from TCAD simulation it is evident that the ideal fin shape for short channel performance is not always well-suited for long channel operation. Due to the quantum confinement effect, TCAD simulations in fact confirm the degradation in the mobility of the long channel nFET devices observed in hardware.

II. SIMULATION APPROACH

Using 3D TCAD tools [2], the full fabrication process flow is simulated, as shown in Fig. 1, and includes all major steps of the gate-last process for bulk FinFETs [3]. Deck calibration steps include detailed matching to TEM images, SIMS data, IV and CV curves, and electrical performance parameters Vth, Idlin, Idsat, Idoff, Ron, and Cov. Continuum models are used for dopant and defect diffusion, while dopant implantation is performed with Monte Carlo methods to reproduce accurately the ultra-shallow junction profiles and to account properly for point defect generation and damage accumulation. Current transport is determined from self-consistent solutions to the drift-diffusion model and Poisson's equation, where the quantum confinement effect in the channel is taken into account by means of the density gradient (DG) method. The low-field mobility is described by the Lombardi model and includes degradation effects due to surface acoustic phonon and surface roughness scattering with orientation dependence. The high-field mobility is based on the Caughey-Thomas formula. In the pFET, the mechanical stress arising from SiGe epitaxial layers is also simulated, with the effect on the hole mobility computed from 6x6 k·p theory [4].

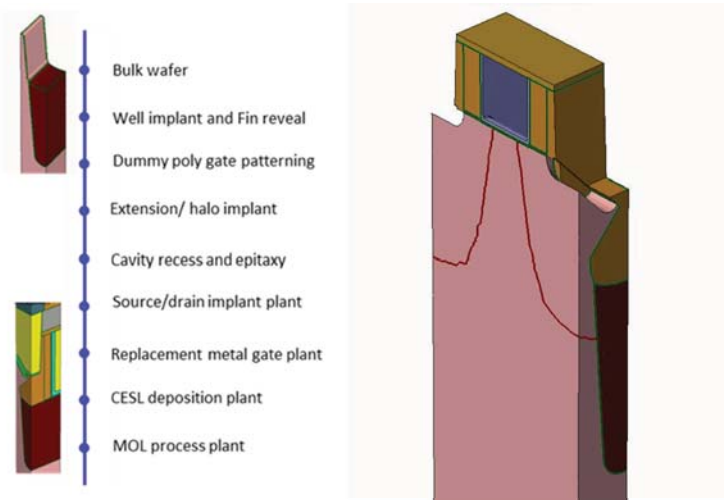

Fig. 1. Left: Process flow of gate-last CMOS sequence for bulk FinFETs. Right: Final simulated structure.

III. SHORT CHANNEL DEVICE SIMULATION RESULTS

The simulations are performed on two fin profiles: the first generation fin profile (Fin 1) and second generation fin profile (Fin 2), as illustrated in Fig. 2. To achieve a more rectangular fin (Fin 2), the FH of Fin 1 is increased by 2 nm, while the TCD and BCD are reduced by 1.5 and 3 nm, respectively. The improvement in the gate capacitance Cgg for Fin 2 relative to Fin 1 is readily observed in Fig. 3, in which Cgg is plotted versus Vg for both the nFET and pFET. By integrating the capacitance over the applied voltage for each fin and then plotting the ratio (Fin 2/Fin 1) of the integrals, the inversion

gain of the second generation fin over the first generation fin as a function of Vg can then be determined, as shown in Fig. 4. At Vg=0.8 V, the inversion gain is 8.0% and 8.4% for the nFET and pFET, respectively.

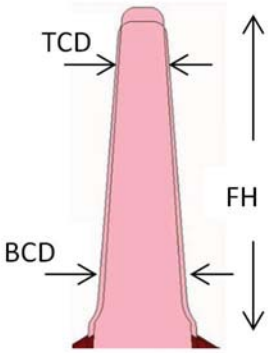

Fig. 2. Illustration of two fin profiles: Fin 1 and Fin 2. In Fin 2, FH is increased by 2 nm, while TCD and BCD are reduced by 1.5 and 3 nm, respectively.

In terms of the device performance, Fig. 5 shows the Ieff vs. Isoff performance for nFET to be improved by 5%, while pFET is improved by 7%. Overall RO performance is improved by 5%, while Ceff [shown in Fig. 7] is increased by 2% due to the taller fin and to the higher inversion because the fin is thinner. As shown in Fig. 6, DIBL is reduced by 6 mV for nFET and 7 mV for pFET, which can be explained by the tighter gate control on the channel due to the smaller fin CD, resulting in improvement in leakage control. While Fig. 7 shows that the total Cov (nFET and pFET combined) is reduced by about 1%, owing to a smaller overlap region between the gate and drain in Fin 2, the higher combined Cgg results in higher Ceff. Meanwhile, Fig. 8 shows Ron to increase by 4% for nFET and to decrease by 6% for pFET. [Ron behavior is explained in Section IV.] In addition, simulated nFET and pFET DC performance versus the Fin Ratio (TCD/BCD) are depicted in Figs. 9 and 10. For trapezoidal fins, a maximum in the performance always occurs due to the trade-off between high inversion/leakage control (thin fins) and high channel conductance (thick fins). Notably, as BCD is reduced, the performance improves strongly, with the location of the performance maximum moving to higher Fin Ratio.

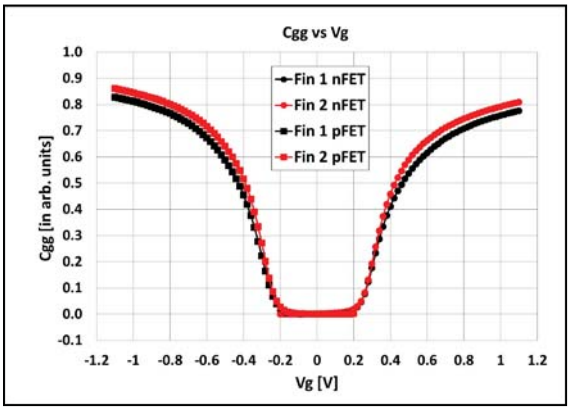

Fig. 3. Cgg vs. Vg for the nFET and pFET. Fin 2 shows higher capacitance and thus higher charge inversion than Fin 1.

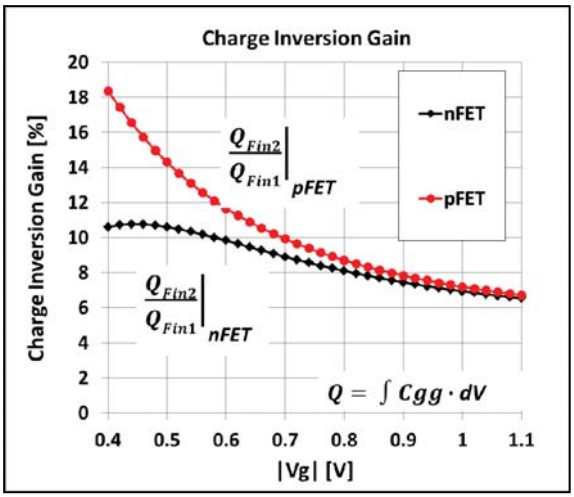

Fig. 4. Charge inversion gain (Fin 2/Fin 1) vs Vg for nFET and pFET, in which Vg is shown on an absolute scale.

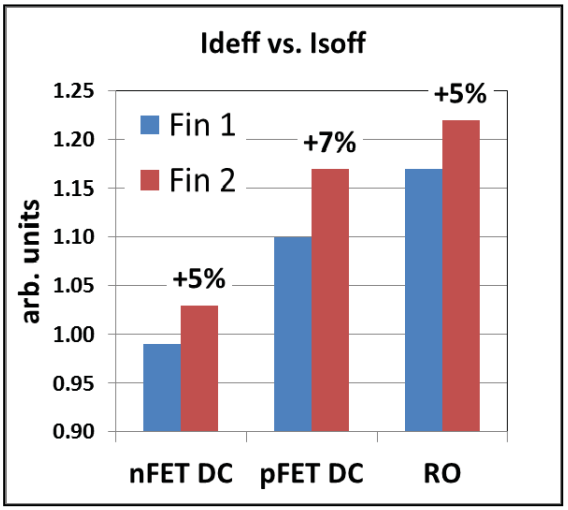

Fig. 5. The DC performance for Fin2 is improved by 5% and 7% for nFET and pFET, respectively. The RO performance is improved by 5%, where the values are normalized to the hardware targets.

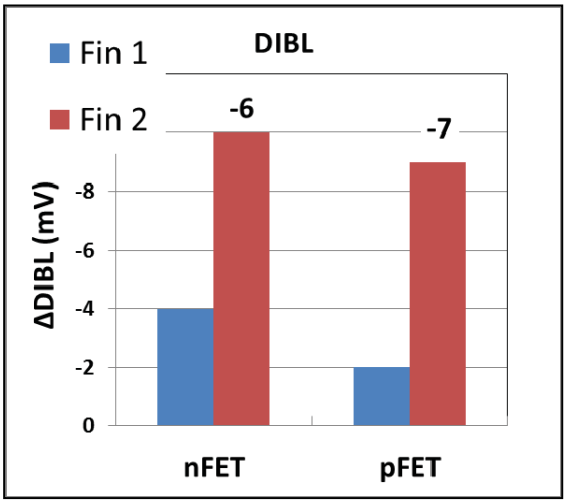

Fig. 6. The nFET and pFET for Fin 2 show 6 mV and 7 mV DIBL reduction, respectively, over Fin 1.

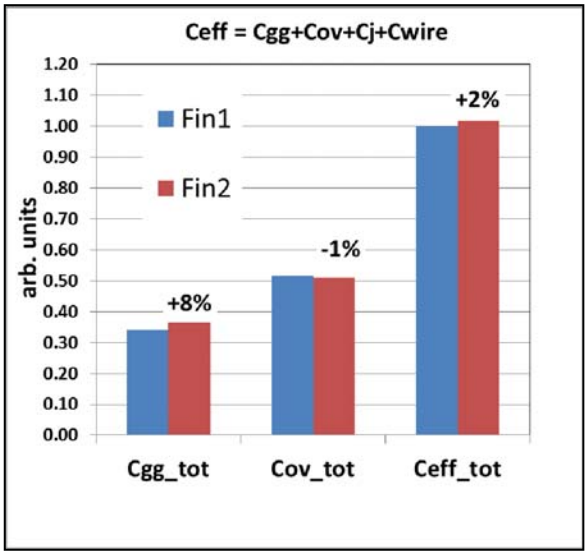

Fig. 7. Fin 2 shows 8% increase in total Cgg and 1% decrease in total Cov, resulting in an overall 2% increase in Ceff. The Cjunction and Cwire capacitance components are small and not included here.

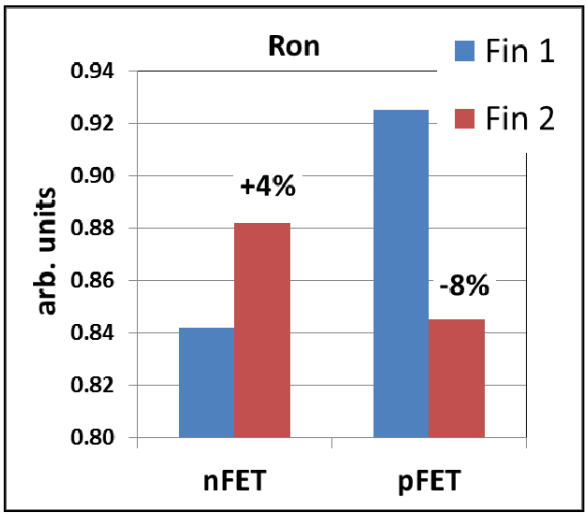

Fig. 8. Fin 2 shows a 4% Ron increase for nFET and an 8% Ron decrease for pFET.

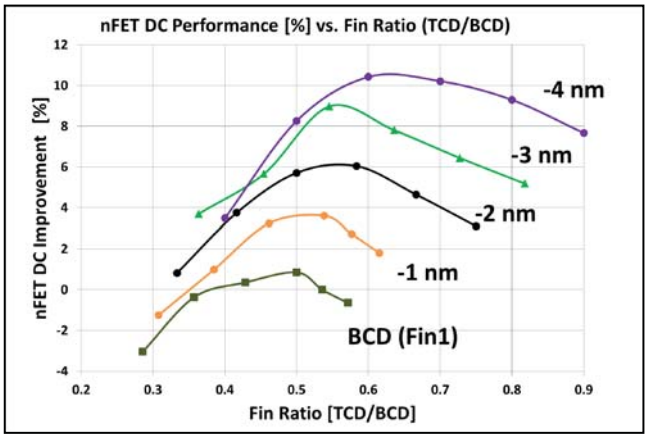

Fig. 9. nFET DC performance versus Fin Ratio.

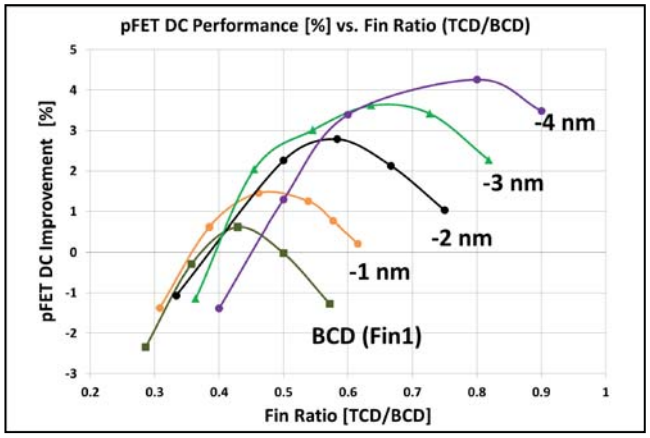

Fig. 10. pFET DC performance versus Fin Ratio.

IV. Long Channel Device Simulation Results

To investigate the reason regarding the Ron behavior reported in Fig. 8, we studied the long channel mobility of both nFET and pFET devices using the IV/CV methodology. As shown in Figs. 11 and 12, the simulated nFET peak mobility is degraded by 14%, while the pFET peak mobility is degraded by only 3%. The simulations are confirmed by the hardware data, also presented in Figs. 11 and 12, which show degradation of 18% in the peak nFET mobility measured for Fin 2 compared to Fin 1, while the peak pFET mobility measured for Fin 1 and Fin 2 is unchanged, consistent with the TCAD simulation result. Because the same mobility models were used for simulation of Fin 1 and Fin 2, the difference in the mobility behavior is therefore intrinsic, attributable only to the change in the fin geometry.

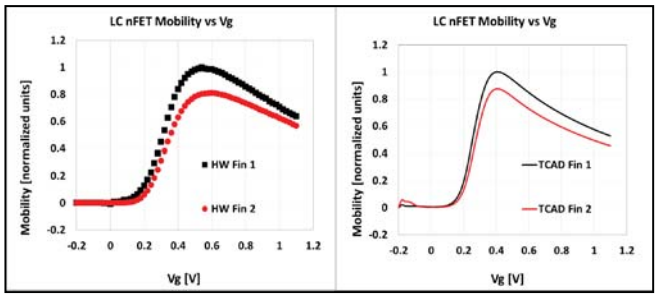

Fig. 11. TCAD simulation of IV/CV method shows a 14.6% reduction in the LC electron mobility for Fin 2 relative Fin 1, consistent with the 21.8% mobility reduction measured in hardware.

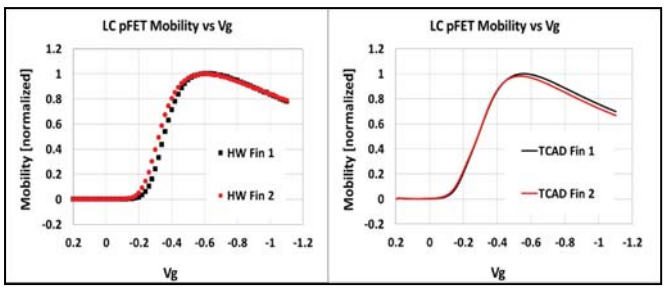

Fig. 12. TCAD simulation of IV/CV method shows a 3.2% reduction in the LC hole mobility for Fin 2 relative Fin 1. This result is consistent with hardware, which shows comparable mobility for Fin 1 and Fin2.

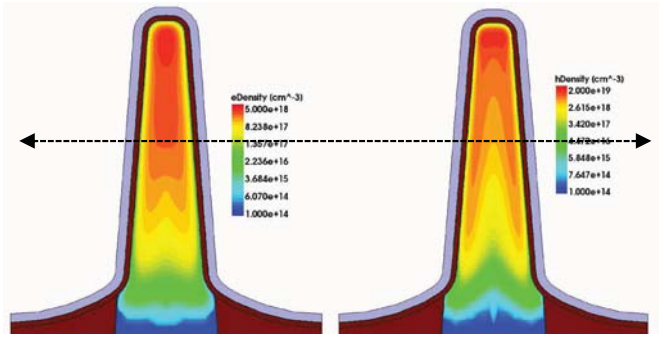

Fig. 13. Current density distribution inside of nFET (left) and pFET (right) at the peak mobility condition.

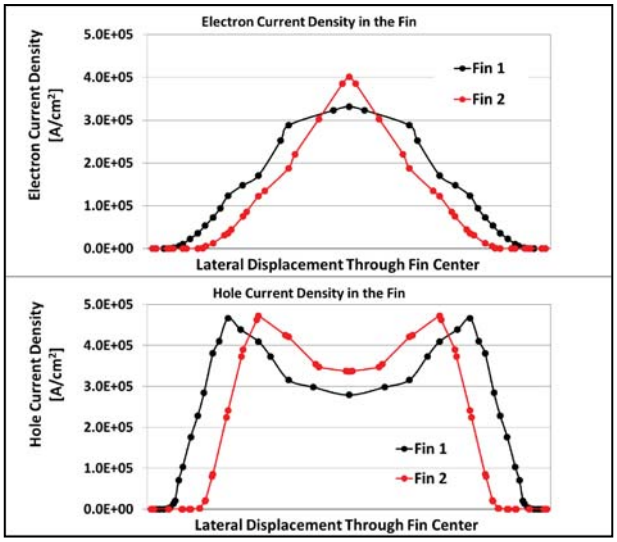

Fig. 14. Electron and hole current densities along cutline in Fig. 13.

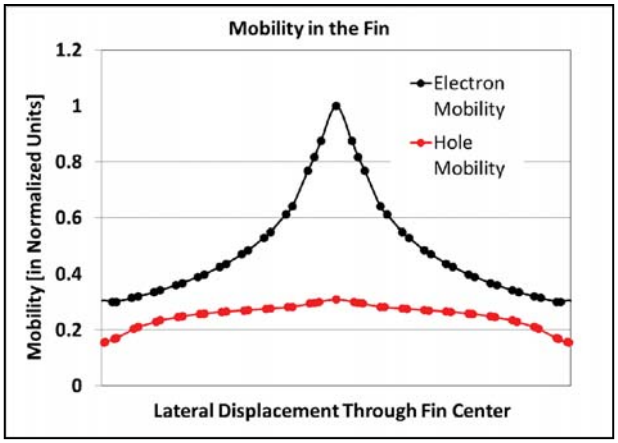

Fig. 15. Electron and hole mobilities along cutline in Fig. 13, showing highest mobility at the center of the fin.

In Figs. 13 and 14, cross-sectional and line plots of the electron and hole current densities in the center of the fin at the peak mobility condition (that is, at Vg = 0.4V for nFET and Vg = −0.5V for pFET, respectively, as shown in Figs. 11 and 12) are presented. From these figures, it is clear that the peak electron current density is located at the fin center, while the peak hole current density is located close to the silicon/oxide interface. Due to the relatively lighter effective mass for the electrons, the quantum confinement effect is able to push the electrons away from the oxide/silicon interface toward the fin center. Meanwhile, in the case of the holes, the relatively higher effective mass of the holes makes the holes less sensitive to the effect of the quantum confinement and the holes therefore remain closer to the silicon/oxide interface [5]. In Fig. 15, the electron and hole mobilities are plotted along the same cutline drawn in Fig. 13. Both the electron and the hole mobility are found to be highest at fin center, due to the occurrence of less surface acoustic and surface roughness scattering. Indeed, a semi-empirical formula [4] shows that the acoustic and surface roughness scattering rates are damped by a factor *exp (-x/lcrit)*, where x is the distance from the interface and lcrit is the critical distance parameter (on the order of 10 nm). Therefore, when the fin is thinned, both the electron and hole mobilities are degraded. However, as shown in Fig. 14, only the nFET is impacted, because the electron current density is highest at the fin center, while the hole current density is highest near the fin sidewall. Finally, because of the quantum confinement, TCAD simulation reports that Vt for Fin2 shifts higher (7 and 5 mV for LVT nFET and pFET, respectively).

V. Summary

Significant DC and RO performance improvement for 14nm nFET and pFET devices using the second generation fin is demonstrated using TCAD. The performance was optimized over a wide range of fin geometries using simulation to tune the Fin Ratio. TCAD was also used to reproduce the testing methods for mobility extraction in long channel devices. The differing mobility behaviors for nFET and pFET reported by hardware were successfully explained by application of semi-classical models for quantum confinement and surface mobility degradation at the silicon/oxide interface.

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