MSDRAM, A2RAM and Z²-FET performance benchmark for 1T-DRAM applications

Joris Lacord
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
joris.lacord@cea.fr

Mukta Singh Parihar
Univ. Grenoble Alpes, IMEP-LAHC, INP, Minatec, CNRS
Grenoble, France
pariharm@minatec.grenoble-inp.fr

Carlos Navarro
Granada University
Granada, Spain
carlosnm@ugr.es

François Tcheme Wakam
Univ. Grenoble Alpes, CEA, LETI & IMEP-LAHC
Grenoble, France
francois.tchemewakam@cea.fr

Maryline Bawedin
Univ. Grenoble Alpes, IMEP-LAHC, INP, Minatec, CNRS
Grenoble, France
bawedinm@minatec.grenoble-inp.fr

Sorin Cristoloveanu
Univ. Grenoble Alpes, IMEP-LAHC, INP, Minatec, CNRS
Grenoble, France
sorin@enserg.fr

Fransisco Gamiz
Granada University
Granada, Spain
fgamiz@ugr.es

Jean-Charles Barbé
Univ. Grenoble Alpes, CEA, LETI
Grenoble, France
jean-charles.barbe@cea.fr

***Abstract*— In this study, we propose a benchmark of performance between three promising 1T-DRAM device structures on SOI substrate: MSDRAM, A2RAM and Z²-FET. For a fair comparison, TCAD simulation with the same basic calibration and typical 28FDSOI technological parameters was used. The merits and limitations of each variant are discussed.**

Keywords: 1T-DRAM, memory, FDSOI, TCAD simulation, Benchmark

I. INTRODUCTION

The classical DRAM (Dynamic Random Access Memory) cell is composed of a transistor and a capacitor (1T-1C) and needs to be billion-times cloned, leading to mandatory aggressive scaling. As in CMOS technology, scaling is still feasible, but is more and more complex and costly. A disruptive solution could be the single-transistor DRAM (1T-DRAM), proposed more than 25 years ago [1]. In general, 1T-DRAMs take advantage of the floating-body effects usually considered in CMOS technology as parasitic and detrimental. '1' state is defined by the presence of charge stored in the floating body and provides high current. State '0' is achieved by removing the charges (usually majority carriers) from the body and features lower current. However, 1T-DRAMs have not yet reached the market mainly for two reasons: writing mechanisms were too demanding in power/voltage/reliability and/or the limited compatibility with standard CMOS process.

The aim of this paper is to compare 3 promising 1T-DRAM structures on SOI: MSDRAM [2], A2RAM [3] and Z²-FET [4]. To perform a fair benchmark, as no similar experimental data (for same technology node or process maturity) and no compact model are available for each structure, we used TCAD simulations with the same basic model calibration. To be realistic, we based our structure definition on 28FDSOI technology [5] and, to be compatible with CMOS platform, we focus on low voltage (~+/-1V) operation. These 1T-DRAM structures will be compared through read current margin and ratio, retention time and read window.

II. 1T-DRAM STRUCTURES SIMULATED WITH TCAD

A. MSDRAM

MSDRAM structure [2] (Fig.1-a) is a typical transistor fabricated on SOI substrate, with a silicon film thick enough to prevent supercoupling effect [6]. '1' state is defined by the presence of charges stored in the silicon body and programming is performed through charge generation by band to band tunneling. Reading is achieved by using back gate voltage to activate the back channel: for '1' state, current flows through this inversion layer.

B. A2RAM

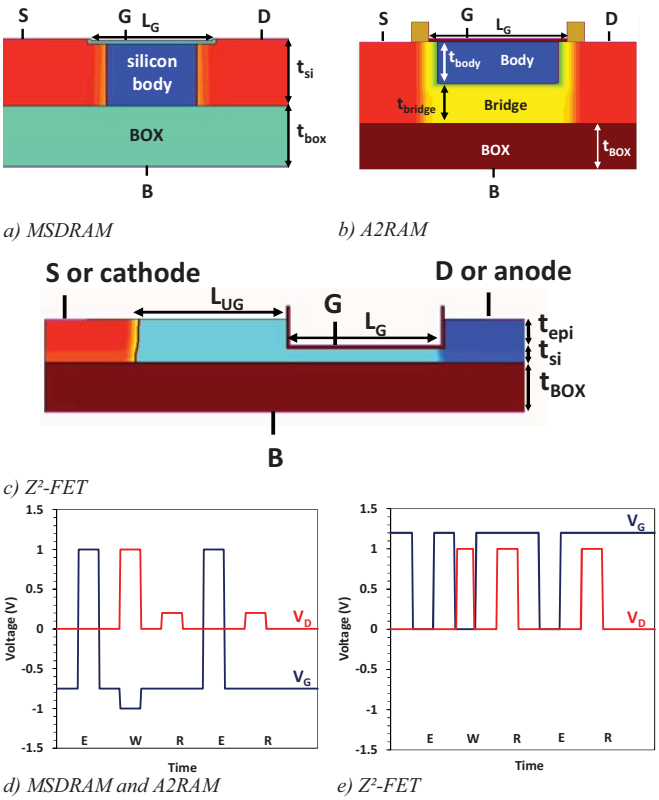
A2RAM structure [3] (Fig.1-b) is also a transistor on SOI with a thick silicon film but its source and drain are shorted by a doped layer called bridge. Its operation is the same as for MSDRAM, except reading which occurs through the physical bridge, instead of the gate-induced back inversion channel.

C. Z²-FET

Z²-FET device (Fig.1-c) is a partially gated PIN diode on SOI [4]. As in other 1T-DRAMs, information is stored by charge collection under the gate. For programming, the device is turned on, then the gate polarization is increased to build potential barrier and so carriers are retained under the gate. The presence of charge, corresponding to '1' state produces a shift of the switching voltage, used to read information. The device turns on in '1' state and remains blocked in '0' state.

D. TCAD simulation methodology

To guarantee a fair comparison, we use same basic simulation setup for each structure: drift diffusion, doping dependent mobility, SRH recombination and Band-to-Band tunneling



a) MSDRAM *b) A2RAM*

c) Z²-FET

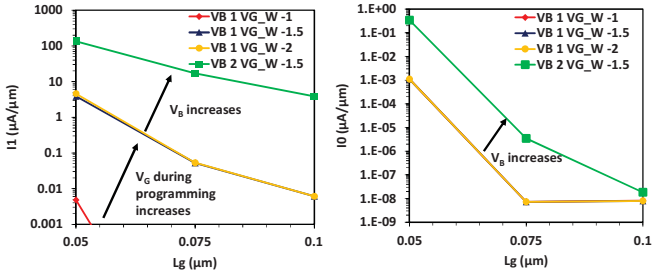
d) MSDRAM and A2RAM *e) Z²-FET*

Fig.1: TCAD structure of a) MSDRAM, b) A2RAM, c) Z²FET and corresponding memory pattern d) and e).

with non-local path model (necessary for A2RAM and MSDRAM programming). Note that this methodology has already been used for A2RAM in [7], and demonstrated a sufficient agreement with experimental measurements for benchmark purpose. Current margin and ratio are evaluated using the following memory sequence: erase (E) – Write (W) – Read (R) – Erase (E) – Read (R), shown on Fig.1-d) for A2RAM and MSDRAM and on Fig.1-e) for Z²-FET. The '1' state read current I_1 is extracted during the first read operation, while '0' state read current I_0 is determined during the second read operation. To guarantee the memory initial state, the cell is first erased. Read window is evaluated during writing or erasing the cell and then monitoring the read current for several polarizations. Retention time is extracted in the worst case for each structure. All simulations are performed at room temperature.Finally, to be consistent with industrial process, we based our structure definition on the 28FDSOI platform [5], so we use EOT=1.2nm, buried oxide thickness t_{BOX}=25nm, minimum gate length of 20nm and maximum silicon film thickness of 25nm (corresponding to the silicon thickness in raised source/drain area of 28FDSOI technology).

III. MEMORY PERFORMANCE EVALUATION BY TCAD

In this section, we evaluate read currents of '1' state I_1 and '0' state I_0 for each 1T-DRAM structure and variable lengths. We also assess the impact of polarization and speed of operation, with a common starting point: 1V maximum and 200ns for each operation (pulse width on Fig.1-e). To allow



a) b)

Fig.2: MSDRAM read currents I_1 a) and I_0 b) for different gate lengths L_G and polarizations. Each operation occurs during 200ns.

1T-DRAM operation in a matrix environment, read currents need to satisfy I_1-I_0>6µA/µm and I_1/I_0>40 [7-9]. We also evaluate the retention time defined as the time required to reduce the current margin (I_1-I_0) by a factor of 2 in the worst case. For MSDRAM and A2RAM, '0' state is unstable and is more degraded during a continuous reading. For Z²-FET, '0' state is unstable but degradation occurs during hold operation.

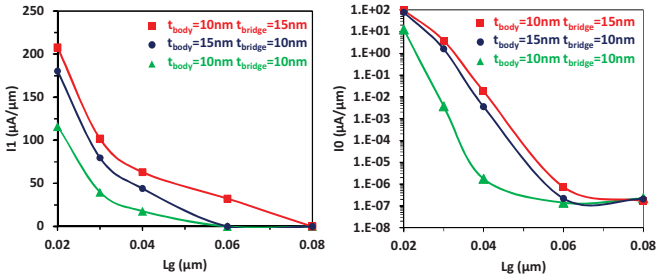
A. MSDRAM

Fig.2 shows the MSDRAM (Fig.1-a with t_{si}=25nm) read current for '1' state I_1 (a) and for '0' state I_0 (b) as a function of the gate length, L_G, for several polarization values. As expected, both read currents increase for shorter gate, which is detrimental for I_0: for L_G=50nm, I_0 is too high for competitive 1T-DRAM operation. If polarizations are limited to 1V (red curve), the I_1 value is very low and too close to I_0. This means that very few holes are stored during programming. To improve I_1, we increase the front-gate voltage during programming (V_{G_W}): I_1 increases up to few µA/µm, still below 6µA/µm to allow matrix operation but is the same for V_{G_W}=1.5 and 2V. This implies that the amount of charge stored while programming (W) saturates at 1.5V: the low I_1 value is not due to programming operation. We finally increase the back-gate voltage V_B to 2V to enhance the inversion layer at the back interface and improve I_1 (green curve): this is efficient but it also leads to a (too) strong increase of I_0 (green curve on Fig2.b), leading to insufficient I_1/I_0 ratio.

The retention time does not exceed the microseconds in this range of polarization. We evaluated MSDRAM performance in "fast" operation condition (not shown here), meaning that each operation occurs during 1ns: as expected, MSDRAM performances are degraded compared to the Fig.2.

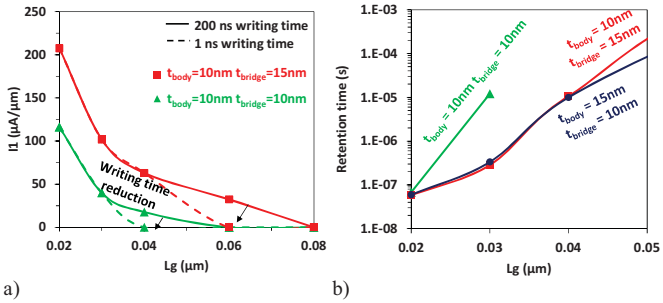
B. A2RAM

For A2RAM structure (Fig.1-b), we consider 3 combinations of bridge and body thicknesses (t_{bridge} and t_{body}): two with t_{si}=25nm (t_{body}=10nm t_{bridge}=15nm and t_{body}=15nm t_{bridge}=10nm) and one with t_{si}=20nm (t_{body}=t_{bridge}=10nm). We simulate them by TCAD using the memory sequence of Fig.1-d and plot on Fig.3 the variation of I_1 (a) and I_0 (b) as a function of gate length. It is noticed that I_1 and I_0 increase for shorter gate: I_1 because the bridge is shorter, so its resistance decreases and I_0 because of the rise of transistor leakage due



a) b)

Fig.3: A2RAM read currents I_1 a) and I_0 b) for gate length L_G variation and different polarizations. Each operation occurs during 200ns and polarizations are limited to +/-1V.



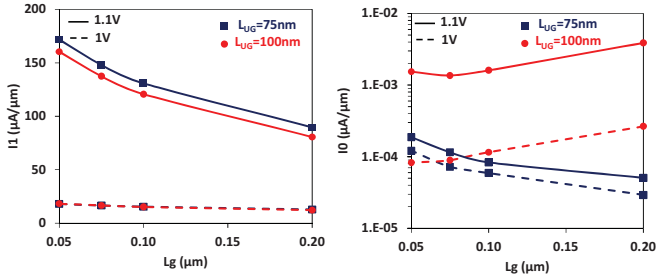
a) b)

Fig.4: With polarization limited to +/-1V a) A2RAM read current I1 for 200ns and 1ns writing time; b) A2RAM retention time.

to short channel effects. This also explains why I_0 decreases for thinner silicon film and why I_1 decreases for lower t_{bridge}. A more complete sensitivity analysis of A2RAM is performed in [7]. Fig.3 shows the scalability of A2RAM and demonstrates that operation is guaranteed for gate length between 30 and 60nm (interesting for integration density), with I_0 below the µA/µm and I_1 superior to 10µA/µm. Fig.4-a shows the variation of read current I_1 with gate length for faster A2RAM operation, especially writing (during 1ns). As expected, I_1 is lowered in fast operation, but A2RAM functioning is still guaranteed (I_0 remains unchanged in fast operation) only for t_{si}=25nm. Simulations performed for increasing polarization up to +/-1.2V during programming result in slightly improved A2RAM performances. We finally evaluate the retention time (Fig.4-b): it reaches 10µs only for t_{si}=20nm and L_G=30nm or t_{si}=25nm and L_G=40nm. In other cases, retention time is below the µs.

C. *Z²-FET*

For Z²-FET, we simulate by TCAD the structure of Fig.1-c with t_{si}=7nm and t_{epi}=15nm using the memory sequence of Fig.1-e. Fig. 5 shows the variation of I_1 (a) and I_0 (b) for different gate lengths, two values of ungated region length L_{UG} and variable operating voltage. As Z²-FET presents same memory performances for slow and fast operations (respectively 200ns and 1ns for each operation) [10-11], Fig.5 shows only fast operation results. At 1V (dashed curves), I_1 doesn't depend on L_G and L_{UG} and is around 20µA/µm; combined with I_0 below 1nA/µm, these configurations allow sufficient performance for 1T-DRAM operation. Then, if the operating voltage is increased up to 1.1V (lines on Fig.5),



a) b)

Fig.5: Z²-FET read currents I1 a) and I0 b) for gate length L_G variation and different operating voltages for fast operation (1ns).

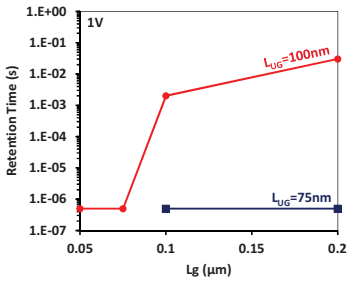


Fig.6: Z²-FET retention time versus gate length.

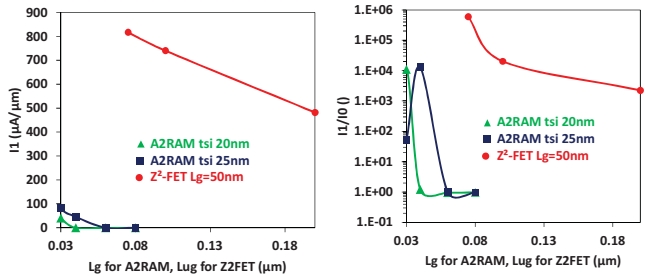
I_1 is improved by a factor of 6, around 160µA/µm, with a slight degradation of I_0 (still around the nA/µm): current margin is largely improved while current ratio is slightly degraded. Note that a more complete memory performance analysis of Z²-FET was performed in [10-11]. Fig. 6 shows the variation of Z²-FET retention time: to exceed 1ms with 1V as operating voltage, $L_G \geq 0.1$µm and $L_{UG} \geq 0.1$µm are requested. Figs. 5 and 6 demonstrate that Z²-FET needs longer device length than A2RAM and MSDRAM to operate as a 1T-DRAM.

D. *Summary*

In this section, we show that MSDRAM in FDSOI doesn't present sufficient performance to be interesting for 1T-DRAM application. Both A2RAM and Z²-FET can be used as 1T-DRAM in fast operation condition. Operation is possible at 1V for A2RAM for a narrow range of technological parameters (L_G, t_{body} and t_{bridge}) while Z²-FET needs larger footprint. However, Z²-FET performance is largely improved for a slight increase in operating voltage. To conclude on this benchmark, next section compares in exactly same condition Z²-FET and A2RAM to determine the more promising structure.

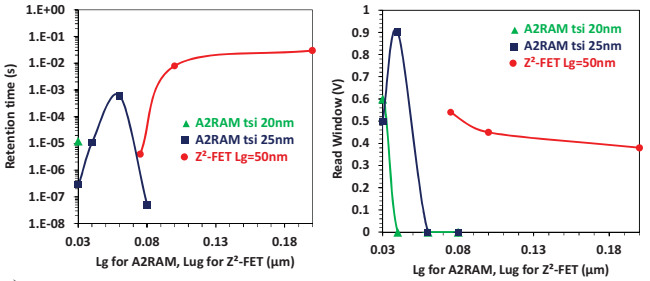
IV. A2RAM AND Z²-FET DIRECT BENCHMARK

In previous section, we demonstrated that A2RAM and Z²-FET 1T-DRAM performances are globally similar if we limit polarization to +/-1V in fast operation. We consider here two A2RAM structures (t_{si}=20 and 25nm) and one "scaled" Z²-FET (with L_G =50nm). We still assume fast operation but we allow a slight increase of polarization up to +/-1.2V. We report on Fig. 7 I_1 (a) and I_1/I_0 ratio (b) for A2RAM (with L_G variation) and for Z²-FET (with L_{UG} variation and L_G=50nm). Note that we choose to vary L_{UG} for Z²-FET because this



a) b)

Fig.7: Z²-FET and A2RAM read currents I1 a) and I1/I0 ration b) for length (L_G or L_{UG}) variation, 1.2V operating voltage and fast operation (1ns).



a) b)

Fig.8: Z²-FET and A2RAM retention time a) and read window b) for length (L_G or L_{UG}) variation, 1.2V operating voltage and fast operation (1ns).

length impacts more the performance. It highlights that, with a slight increase of polarization, Z²-FET largely outperforms A2RAM in terms of read current and margin, but still with larger footprint: source to drain distance is L_G in A2RAM case while it is L_G+L_{UG} for Z²-FET.

From Fig. 4-a and Fig. 6, we know that for operation at -/+ 1V, retention time is largely higher in case of Z²-FET (>10ms) compared to A2RAM (<100µs). If we increase operating polarization, retention time remains unchanged for A2RAM while it is improved for Z²-FET (Fig.8-a). It is due to the increase of polarization, which make stronger potential barriers and higher I_1 read current (Fig .5-a), even with a shorter gate length. We finally evaluate the read window for both structures (Fig. 8-b). It corresponds to the range of gate voltage V_g for A2RAM and of drain voltage V_d for Z²-FET usable to read the information with I_1>6µA/µm and I_1/I_0>40. A2RAM read window is larger than in Z²-FET (~900mV vs ~450mV) but information can be read on a larger range of lengths for Z²-FET (contrary to A2RAM) with a slight variation of performance. This last remark suggests a larger sensitivity to variability concerns for A2RAM structure.

CONCLUSION

In this paper, we compared through TCAD simulations the memory performance of three 1T-DRAM structures (MSDRAM, A2RAM and Z²-FET) for low voltage (1V) and fast operation. We demonstrated that MSDRAM does not present sufficient read current and retention time to be interesting for 1T-DRAM applications. The Z²-FET and A2RAM present similar memory performance, even if Z²-FET allows reaching longer retention time than A2RAM but with a larger footprint. Therefore, we finally extended the benchmark of Z²-FET and A2RAM with a slight increase of operating voltage up to +/-1.2V. We showed that Z²-FET outperforms A2RAM in terms of read current margin and ratio and retention time but still with larger length. We also remarked that A2RAM performances are more sensitive to technological parameters (t_{si} and L_G) than Z²-FET, suggesting a higher sensitivity to variability concern. As opposed to A2RAM, which needs additional specific process steps to build the bridge, Z²-FET is fully compatible with standard CMOS process in 28FDSOI [12]. We can consider Z²-FET as the most promising structure for 1T-DRAM applications.

ACKNOWLEDGMENT

The research leading to these results has received funding from the European Union's Horizon 2020 research and innovation program (grant agreement 687931 REMINDER).

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