

Analysis of the Effect of Field Enhancement at Fin Corners on Program Characteristics of FinFET Split-Gate MONOS

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Abstract—The effect of field enhancement at Fin corners on program characteristics of FinFET Split-gate metal oxide nitride oxide silicon (SG-MONOS) is analyzed. The program characteristics using source-side injection (SSI) are found to be insensitive to the variation of the curvature radius at Fin corners, which shows the robustness of FinFET SG-MONOS to Fin shape variation in the fabrication process.

Index Terms—FinFET, MONOS

I. INTRODUCTION

There is an increasing need of high reliability and performance of microcontroller units with embedded Flash memories (eFlash) for automotive application to realize autonomous driving. Split-gate metal oxide nitride oxide silicon (SG-MONOS) has a long history of achievements as highly reliable and high speed eFlash [1]. A memory cell of SG-MONOS consists of a control-gate (CG) and a memory-gate (MG) as shown in Fig. 1. A silicon nitride layer sandwiched between top and bottom oxide layers is placed under MG for charge storage.

SG-MONOS has the advantage of fast program speed which is realized by source-side injection (SSI) [2]. High lateral electric field is generated in the weak-gate-control region between CG and MG during program operation as shown in Fig. 1 and Table I, which enables efficient hot carrier injection into the nitride layer as shown in Fig. 2.

To push the progress in the memory capacity and performance by scaling, FinFET SG-MONOS as shown in Figs. 3 and 4 is under development [3]. FinFET devices have a superior gate controllability and immunity to short-channel effects compared to conventional planar ones.

There are several research reports on MONOS-type memories with FinFET process [4]–[6]. In these studies, Fowler-Nordheim (FN) tunneling or channel hot electron (CHE) was used to program MONOS memories. An improvement of FN program speed by several orders of magnitude has been observed by reducing the curvature radius at Fin corners [6], because charge injection at Fin corners are enhanced by electric field enhancement owing to geometric effect. The effect of the field enhancement on program characteristics

using the CHE program or the SSI program, however, has not fully been investigated yet.

In this paper, the effect of the field enhancement at Fin corners on SSI program characteristics of FinFET SG-MONOS is analyzed using 3D TCAD simulation. Dependencies of the program speed on curvature radius at Fin corners are analyzed.

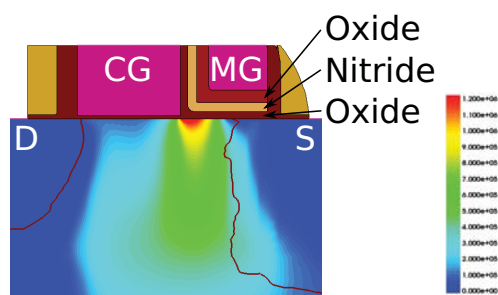


Fig. 1. Lateral electric field in V/cm in SG-MONOS just after applying program bias shown in Table I.

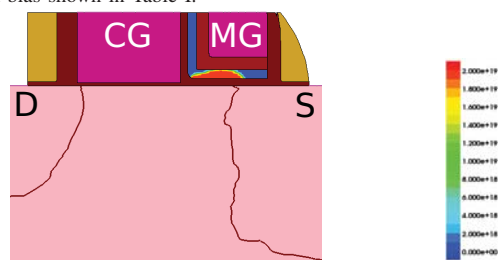


Fig. 2. Trapped electron density in cm^{-3} in the silicon nitride layer at program time $t = 1 \times 10^{-7}$ s.

TABLE I
OPERATION CONDITIONS OF SG-MONOS. VDD : LOGIC POWER SUPPLY, PHV : POSITIVE HIGH VOLTAGE, NHV : NEGATIVE HIGH VOLTAGE.

Operation	D	CG	MG	S
Read	VDD	VDD	0	0
Program	VDD	VDD	PHV	PHV
Erase	VDD	0	NHV	PHV

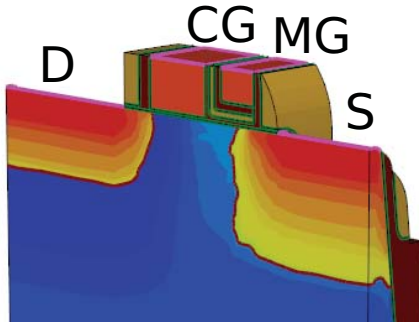


Fig. 3. A cut section view of FinFET SG-MONOS.

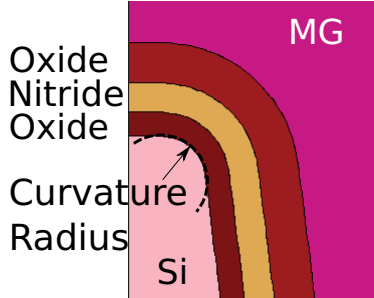


Fig. 4. A cross section view in the vicinity of Fin corner.

II. MODELING

Hot carrier injection and charge trapping in the nitride layer are key mechanisms for SSI program of SG-MONOS. Fiegna hot carrier injection model [7] is used to simulate the injection. The energy level and the density of trap states in the nitride layer are set to 1.5 eV below the conduction band and $2 \times 10^{19} \text{ cm}^{-3}$, respectively [8]. 3D TCAD simulation is carried out using Sentaurus Device [9].

III. RESULTS AND DISCUSSION

The simulation models described above are verified by comparing measured and simulated program characteristics as shown in Fig. 5. As the program time proceeds, the number of trapped electrons in the nitride layer increases, resulting higher threshold voltage of MG. The validity of the simulation models is confirmed over the wide range of program time.

Simulated program characteristics with various curvature radii at Fin corners are shown in Fig. 6. Although vertical electric field in the bottom oxide at Fin corners is enhanced, program speed is not affected by reducing the radius.

The insensitivity is caused by two mechanisms: (1) SSI current is primarily determined by the lateral electric field, and (2) a self-limiting process [11] works effectively in MONOS-type memories.

The SSI current is primarily determined by the lateral electric field because electrons gain kinetic energy from the lateral electric field to surmount the energy barrier between the silicon channel and the bottom oxide. The lateral electric field on the surface of the Fin is insensitive to the radius as shown in Fig. 7. The electron injection current is, therefore, insensitive to the radius as shown in Fig. 8.

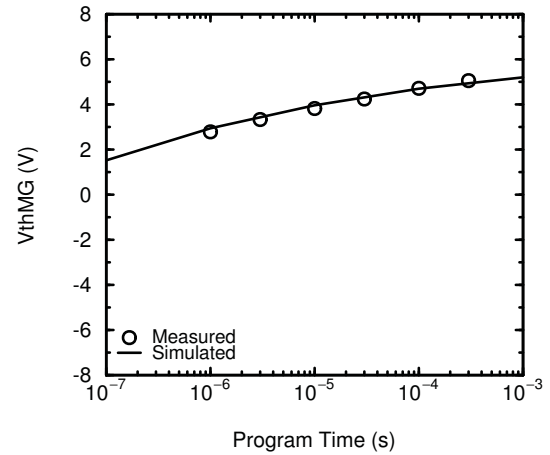


Fig. 5. Measured and simulated program characteristics of FinFET SG-MONOS.

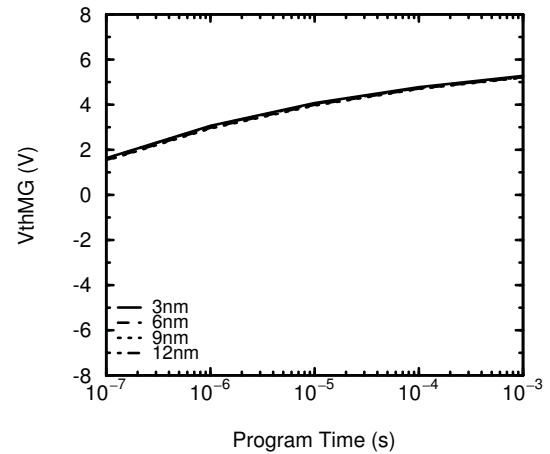


Fig. 6. Simulated program characteristics of FinFET SG-MONOS with various curvature radii.

Compared with FN tunneling current, the SSI current is less sensitive to the variation of the radius, which shows the robustness of SSI program to Fin shape variation in the fabrication process. The SSI current is compared with FN tunneling current [10] in Fig. 9. The FN tunneling current varies by several orders of magnitude with changing the radius because the effect of field enhancement is amplified by the exponential dependence of the FN tunneling current on the vertical electric field. This is consistent with the improvement of the program speed with FN tunneling by reducing the radius [6].

Another factor to the insensitivity is a self-limiting process [11]. The trapped electrons in the nitride layer alleviate the vertical electric field in the bottom oxide. Although the field enhancement is observed just after applying program bias as shown in Fig. 10, the traps located at the corners are preferentially occupied by the trapped electrons as shown in Fig. 11, which reduces the field enhancement. The self-

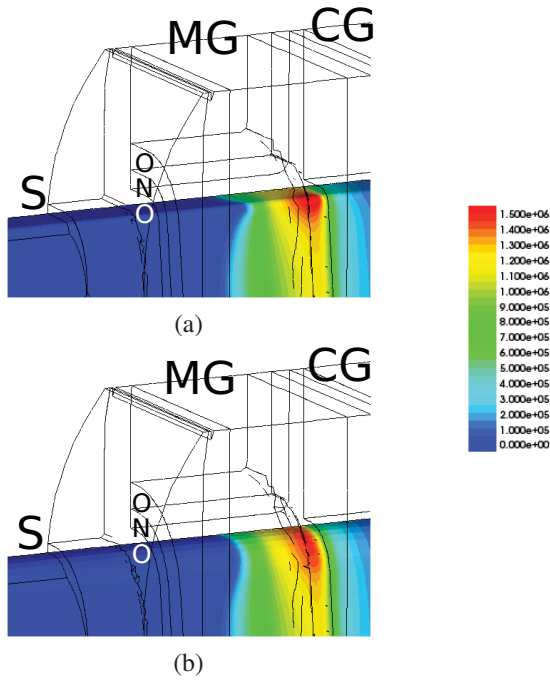


Fig. 7. Lateral electric field in V/cm on the surface of the Fin just after applying program bias. (a) $r = 3$ nm, (b) $r = 12$ nm.

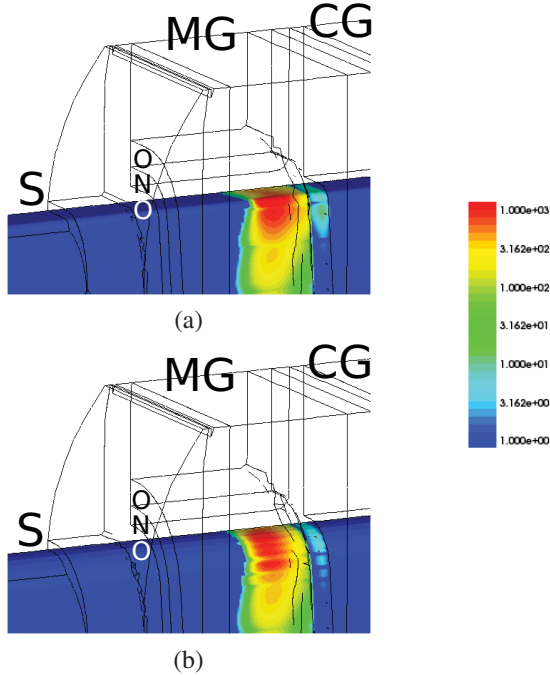


Fig. 8. Electron injection current density in A/cm^2 on the surface of the Fin just after applying program bias. (a) $r = 3$ nm, (b) $r = 12$ nm.

limiting process works effectively in MONOS-type memories because the injected electrons are localized in the vicinity of the injection point. In floating-gate-type (FG-type) memories, the injected electrons move freely in the floating gate to keep the electrostatic potential of the floating gate flat.

The effect of the self-limiting process is confirmed by

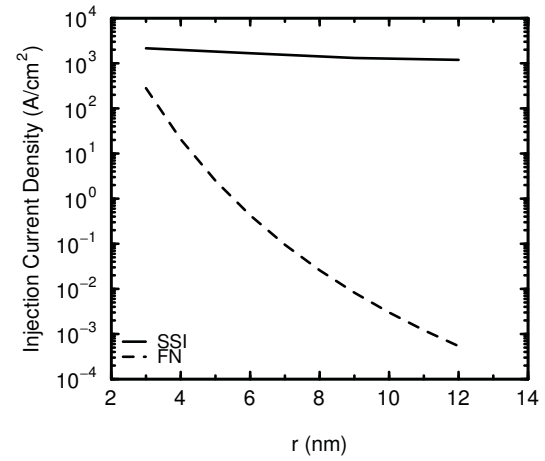


Fig. 9. Maximum electron injection current density just after applying program bias as a function of the curvature radius at Fin corners r .

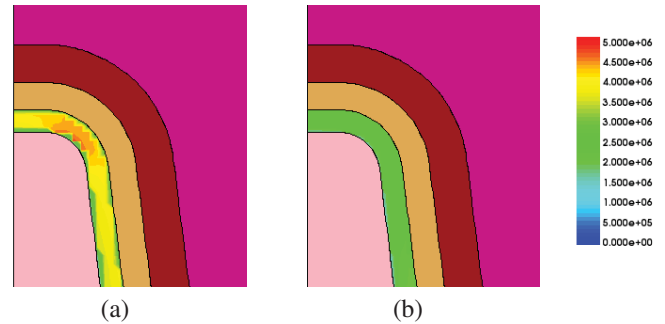


Fig. 10. Electric field magnitude in V/cm in the bottom oxide film (a) just after applying program bias, and (b) at program time $t = 1 \times 10^{-8}$ s.

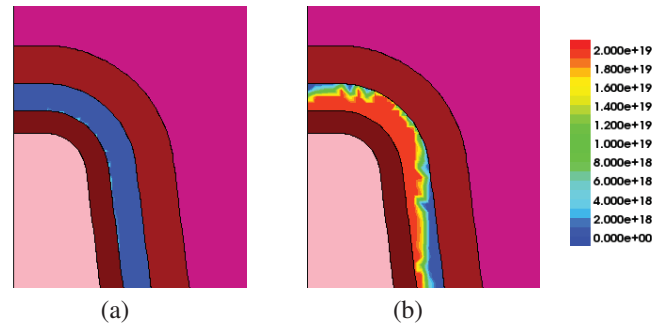


Fig. 11. Trapped electron density in cm^{-3} in the silicon nitride film (a) just after applying program bias, and (b) at program time $t = 1 \times 10^{-8}$ s.

comparing simulation results of MONOS-type and FG-type memories. Transfer characteristics of FinFET SG-MONOS after program operation are insensitive to curvature radius as shown in Fig. 12, which implies that the trapped electrons in the nitride layer alleviate the field enhancement in the bottom oxide. On the other hand, transfer characteristics of FinFET FG-type memory which has a conductive floating gate instead of the nitride layer show higher sensitivity on the curvature radius after program operation as shown in Fig. 13. The electric fields in the bottom oxides at the corners of

MONOS-type and FG-type memories are compared in Fig. 14. The self-limiting process mitigates the field enhancement in MONOS-type memories in 10 ns, while it is much slower in FG-type memories. These results suggest that MONOS-type memories are more robust to Fin shape variation in the fabrication process compared to FG-type memories.

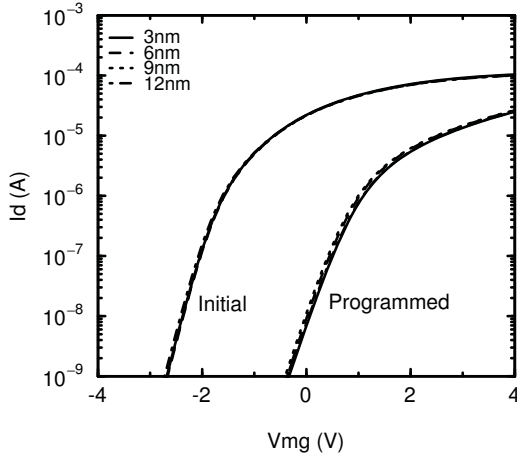


Fig. 12. Simulated transfer characteristics of FinFET SG-MONOS after program with various curvature radii. The program time is 1×10^{-7} s.

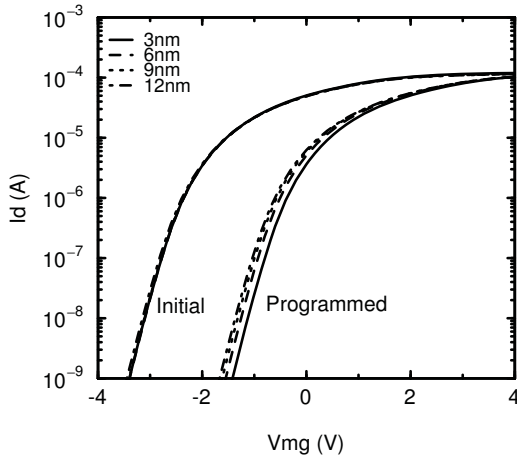


Fig. 13. Simulated transfer characteristics of FinFET split-gate floating-gate-type memory after program with various curvature radii. The program time is 1×10^{-7} s. The MG voltage during program is reduced in accordance with the reduction of the equivalent oxide thickness.

IV. CONCLUSION

The effect of field enhancement at Fin corners on program characteristics of FinFET SG-MONOS was analyzed. The program characteristics using SSI were found to be insensitive to the variation of the curvature radius at Fin corners, which shows the robustness of FinFET SG-MONOS to Fin shape variation in the fabrication process.

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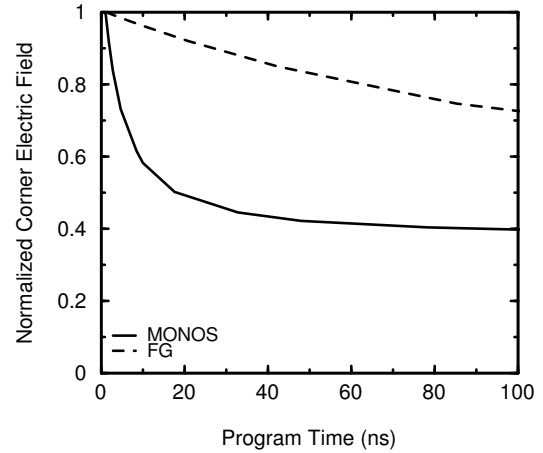


Fig. 14. Normalized electric field in the bottom oxide film at the Fin corners of MONOS-type and FG-type memories.

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