PCM compact model: Optimized methodology for model card extraction

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***Abstract*—To achieve high yield on product embedding PCM memory, it is mandatory to provide to designers accurately calibrated PCM compact model. To achieve this goal, it is mandatory to develop standardized model card extraction methodology. In this paper, we present a PCM model card extraction flow based on a minimal set of static and dynamic measurements. Based on this measurement, characteristics are first obtained and model card parameters extracted without any loop back, i.e. each parameter is extracted only once on a given characteristic. After this extraction procedure, model card values are validated through a comparison with an extra characteristics SET-Low characteristic not used for the extraction.**

Keywords—phase change random access memory; PCRAM; PCM; model extraction; compact model; resistive memory.

I. Introduction

In the resistive memory landscape, Phase Change Memory technology (PCM) is often seen as the most mature and well suited for embedded applications [1]. To successfully yield first products with embedded PCM, designers have to run extensive simulation campaign using PCM compact model. The main requirements for a compact model is to be fast, robust and accurate, so that designers are able to simulate correctly memory arrays. In this aim, we have already proposed a compact model of PCM (to appear in [2]), which is fully continuous, based on comprehensive rate equations and validated versus experimental data.

Compact model links technology development to circuit simulation by the mean of model card parameters. Thus any PCM technology evolution has to be taken into account by the compact model through model card extraction. In this context, the aim of this paper is to present an efficient model card extraction flow for our PCM compact model. The extraction methodology relies on a minimal set of static and dynamic measurements. Based on this measurement, characteristics are first obtained and model card parameters extracted without any loop back, i.e. each parameter is extracted only once on a given characteristic. The remainder of the paper is organized as follow: section II presents the specific the measurements that have to be performed together with the compact model main equations. Section III describes the model card extraction method, based upon validation on experiments, and finally section IV gives some concluding remarks.

II. Specific Electrical Characterizations and the Developped Compact Model

A. Test Structure

All measurements presented in the following are acquired on a wall-type PCM test structure [3] composed of a bipolar selector and a resistive element (1B1R). The PCM cell is a wall-type structure, with a Ge-enriched GST material. A TEM cross-section as well as an equivalent schematics of the test structure is shown in Fig. 1.

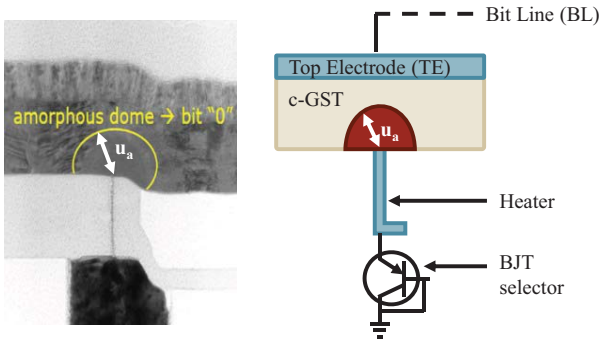

Fig. 1. TEM cross section of the test structure on the left hand side and equivalent schematics on the right hand side.

B. Measurement setup

The sketch of the transient measurements is presented in Fig. 2. A sequence of PROG pulses with increasing voltage and fixed time frame, as sketched Fig. 2.a) is called a staircase-up. This measurement is performed from both SET and RESET state, under several temperatures. It is used to plot programming current versus programming voltage (I-V), and read resistance against programming current (R-I) from both states. This measurement is also performed for several pulse widths, which allows to plot the SET Low characteristics that is the resistance versus current for several pulse widths. The last characterization (Fig. 2.b)) is performed by raising gradually the falling time of the programming pulse, identical otherwise. The read resistance as a function of the fall time (R-FT) is called Rampdown SET, and is used to study the quenching time.

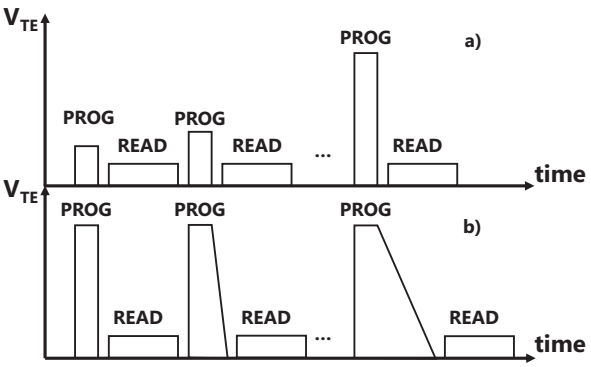

Fig. 2. Chronograms of the applied voltages. a) staircase-up measurement; b) quenching time measurement. The resistance during the reading pulse (READ) and the current during the programming pulse (PROG) are measured.

C. Compact model equations and parameters

Our fully continuous compact model [2] is based on rate equations of phase fractions. The device resistance is computed using phase resistances in series weighted by their respective phase fraction [4], as in equation (1):

$$R_{PCM} = (F_c + F_m)R_c + (1 - F_m - F_c)R_a + R_{heater} \quad (1)$$

The model relies on two explicit state variables, which are F_c and F_m, standing respectively for crystalline and melted fraction, the remaining part being considered as amorphous. Thus, equation (1) continuously links a semiconducting crystalline conduction [5] to a Poole-Frenkel type amorphous conduction [6]–[9], which are expressed in equations (2)-(4):

$$R_c = R_{c0} \exp\left(\frac{E_{ac}}{kT}\right) \quad (2)$$

$$R_a = \left[\frac{A_{kPF}}{F_c \cdot u_{a,max}} exp\left(-\frac{\Phi_{PF} - \beta_{PF}\sqrt{F}}{kT}\right)\right]^{-1} \quad (3)$$

$$F = \frac{U}{u_{a,max}(1 - F_c - F_m)} \quad (4)$$

The internal temperature is computed using equation (5) at the hottest spot of the GST using a first order differential equation [10], [11], and this approximation is corrected using several geometrical considerations, such as phase-dependent thermal resistances [12] shown in equation (6):

$$R_{th} * C_{th}\frac{\partial T}{\partial t} + T = R_{th} * \frac{U^2}{R_{PCM}} + T_{amb} \quad (5)$$

$$R_{th} = R_{thc}(F_c + F_m) + R_{tha}(1 - F_m - F_c) \quad (6)$$

Melting transition (resp. crystallization) is computed as a solution of the first order differential equation (7) (resp. (8)):

$$\tau_m \frac{\partial F_m}{\partial t} + F_m = \left[1 + \exp\left(\frac{T_m - T}{\sigma_m}\right)\right]^{-1} \quad (7)$$

$$\frac{\partial F_c}{\partial t} = (1 - F_m - F_c) \cdot \frac{v_g(F_c, F_m)}{\tau_{set}(T)} \quad (8)$$

The crystallization time τ_{set} follows a non-Arrhenius behavior [13]. Equation (9) is used to help control the retention time, and the fitting equation (10) is used to increase the growth speed for low amorphous fraction. This effect is introduced in the model to consider the temperature gradient inside the PCM cell neglected by our simple temperature calculation:

$$\tau_{set}(T) = \tau_{0LT} exp\left(\frac{E_{aLT}}{kT}\right) + \tau_{0HT} exp\left(\frac{E_{aHT}}{kT}\right) \quad (9)$$

$$v_g(F_c, F_m) = b \cdot (1 - F_m - F_c) \cdot e^{1 - b(1 - F_m - F_c)} \quad (10)$$

U is the voltage, T is the temperature and k is the Boltzmann constant. All other parameters are detailed in Table I.

TABLE I. PHYSICAL AND FITTING PARAMETERS

Symbol	Description	Value
Conduction parameters		
A_{kPF}	Poole-Frenkel conduction prefactor	$3.10^{-12}\Omega^{-1}$.m
β_{PF}	Poole-Frenkel constant	$9\mu eV.V^{-0.5}.m^{0.5}$
Φ_{PF}	Poole-Frenkel Activation Energy	0.15eV
u_{amax}	Maximum size of the amorphous dome	48nm
R_{c0}	Crystalline resistance at 0K	3kΩ
E_{ac}	Activation energy of the crystalline conduction	0.04eV
R_{heater}	Resistance of the heater	2.3kΩ
Thermal parameters		
C_{th}	Effective thermal capacitance	$10^{-16}J.K^{-1}$
R_{thc}	Crystalline effective thermal resistance	$1.5K.\mu W^{-1}$
R_{tha}	Amorphous effective thermal resistance	$5.8K.\mu W^{-1}$
Melting parameters		
T_m	Melting temperature	740K
σ_m	Spread of the melting temperature	67K
τ_m	Characteristic melting time	1ns
Crystallization parameters		
τ_{0LT}	Crystallization time prefactor for low temperature	2.10^{-39}s
E_{ALT}	Activation energy for low temperature	3eV
τ_{0HT}	Crystallization time prefactor for high temperature	300ns
E_{AHT}	Activation energy for high temperature	0.01eV
b	Fitting parameter	10

The whole characterizations have been modeled with this only set of parameters.

III. MODEL CARD EXTRACTION FLOW

The flow chart of the proposed extraction methodology is presented in table II. The first step of the extraction is the modeling of the crystalline and the melted conductions, through the fitting of the current-voltage characteristic for the SET state. The second and third steps are focusing on the I-V characteristics of the RESET state, in logarithmic scale for the fitting of the subthreshold conduction and the threshold switching. Crystalline and amorphous conductions are not intertwined and could be fitted in parallel. However, it is mandatory to fit them carefully prior to the other steps. Self-heating and melting parameters are extracted in step 4 on the resistance versus current characteristics from the SET state. It could also be extracted on the R-I characteristics from the RESET state, because both characteristics are superimposed in this regime. Then step 5 is performed to model crystallization dynamics, using the resistance vs. fall-time characteristics. The

last step is used to verify the good consistency of the extraction flow, by checking whether SET Low is accurately modeled.

TABLE II. SUMMARY OF THE EXTRACTION STEPS

Step	Fitting target & extracted parameters	Experimental data
1	Crystalline & melted conduction R_{c0}, E_{ac}, R_{heater}	I-V from SET state in temperature
2	Amorphous conduction A_{kPF},$u_{a,max}$,Φ_{PF}	I-V from RESET state at different temperatures
3	Threshold switching R_{tha}	I-V from RESET state at different temperatures
4	Self-heating & melting R_{thc}, T_m, σ_m	R-I from SET state at different temperatures
5	Crystallization dynamics τ_{0HT}, E_{aHT}, b	R-FT at different temperatures
6	SET Low crystallization Verification	R-I from RESET state at different pulse width

The extraction strategy is sequential. Except from steps 1 and 2 that can be switched independently, all extractions steps depend on the previous one.

The current-voltage characteristics of the crystalline state is plotted in Fig. 3. The impact of the selector is not de-embedded, the voltage seeable in all the Fig. 3 and Fig. 4. On the contrary the strategy is to previously extract the transistor model card on a dedicated selector-only structure and simulated both models in series when extracting PCM's model card. The dynamic resistance at high voltage is the heater resistance R_{heater}. The temperature impact is limited, so E_{ac} is small. R_{c0} then models the low voltage resistance.

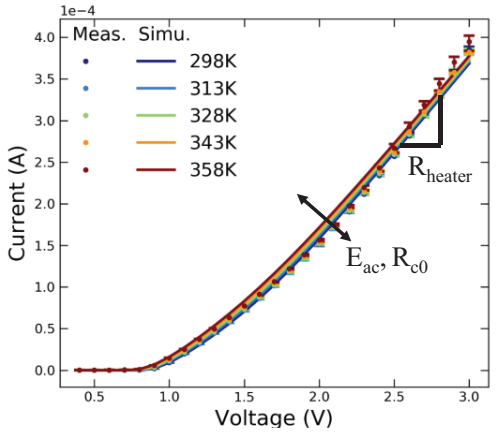

Fig. 3. Current versus voltage (I-V) during a staircase-up from SET state for several temperatures allowing the extraction of the crystalline conduction parameters (R_{c0}, E_{ac}, R_{heater}).

Current versus voltage in amorphous state for several temperatures is presented in logarithmic scale in Fig 5. Φ_{PF} tunes the spread of the curves, $u_{a,max}$ the slope (the slope does not change in temperature), and A_{kPF} the level of the ambient curve. R_{tha} is then chosen so that the threshold switching is triggered at the correct voltage. The temperature dependence of the threshold switching is not well fitted above 328K, the model triggers earlier than the silicon. It seems that some thermal dissipation is not accurately taken into account.

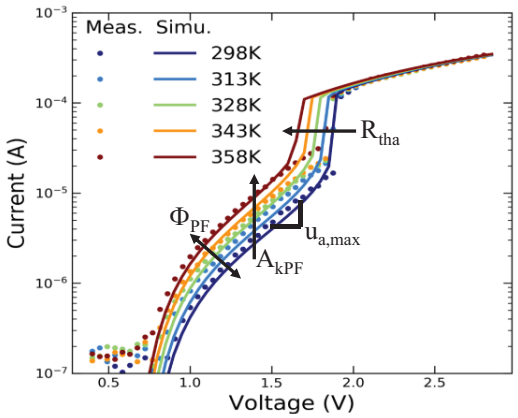

Fig. 4. Current versus voltage (I-V) during a staircase-up from RESET state for several temperatures allowing the extraction of the Poole-Frenkel parameters (A_{kPF},$u_{a,max}$,Φ_{PF}). The threshold switching is fitted with the amorphous thermal resistance parameter R_{tha}.

The high field part of the staircase-up measurement is shown in Fig. 5. It equates to a staircase-down measurement and exhibits melting characteristics. The model parameter accountable for the internal temperature at high field (in melted phase) is R_{thc}. Since all conduction-related parameters are previously extracted (E_{ac} and Φ_{PF} have been extracted on the external temperature dependence), the spread between the curves is due to self-heating, so R_{thc}. We assume that the state achieved at the highest current (i.e. 350µA) is fully amorphous, whereas the state in which the cell is programmed after a 150µA-long-square-pulse is perfect crystal. This may have to change in the future, if over-programming is taken into account. The couple of parameters (T_m,σ_m) are then extracted in the transition, T_m shifts the transition and σ_m steeps it.

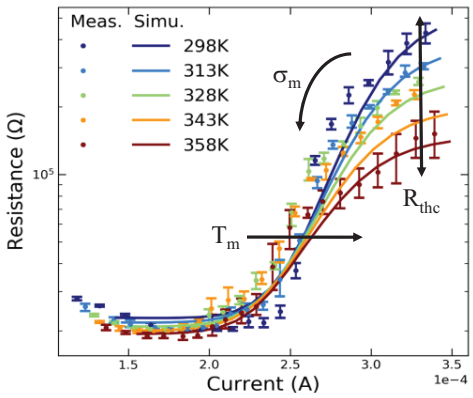

Fig. 5. Resistance versus current (R-I) during a staircase-up from SET state for several temperatures allowing the extraction of the thermal (R_{thc}) and melting parameters (T_m, σ_m)

The Rampdown SET characteristic is used to extract the crystallization parameters, i.e. τ_{0HT}, E_{aHT} and b. It is presented in Fig. 6, where ther resistance versus fall time is plotted for several temperatures. τ_{0HT} fits the average time of crystallization, and b the rapidity of the transition. The parameter E_{aHT} is used to fit the faster transition at high temperature, but it does not seem to be the case so it is set to 0, so that the ambient temperature does not affect the speed of the transition.

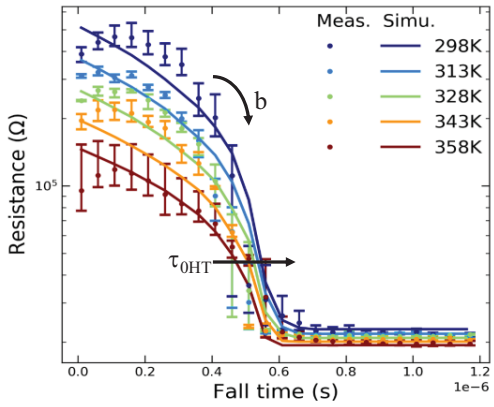

Fig. 6. Resistance versus fall time (R-FT) during a Rampdown SET for several temperatures allowing the extraction of the crystallization dynamics parameters (τ_{0HT}, E_{aHT}, b).

Once all parameters are extracted, it is mandatory to verify that the model is also valid for SET low dynamics. The resistance versus current measured during a staircase-up with a variation of the pulse width is shown in Fig. 7. In the low current regime, the resistance level depends on the pulse width, shorter pulses allow less crystallization. The model is accurate from 600ns.

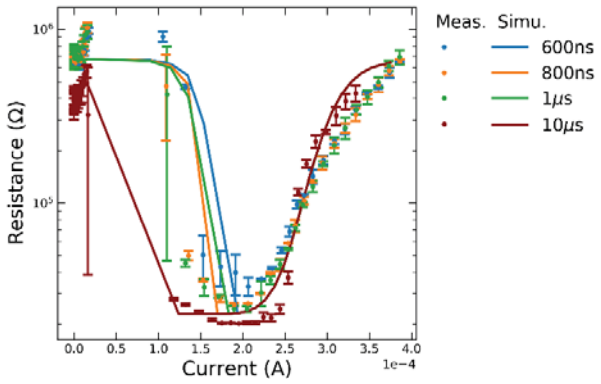

Fig. 7. SET Low: resistance versus current (R-I) during a staircase-up for several pulse widths validating of the accuracy of the extraction.

IV. Conclusion

An optimized PCM model card extraction method has been successfully developed, based on a minimal set of fast acquired transient measurements. The proposed flow is logically constructed, so that each parameter is extracted only once, on one characteristic. The simulation versus measurements presents a good agreement for all characteristics where the parameters are extracted. Moreover, an extra characteristics have been accurately fitted with the same model card, which validates the accuracy of the extraction.

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