On the NBTI of Junction-less Nanowire and Novel Operation Scheme to Minimize NBTI Degradation in Analog Circuits

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***Abstract*—Nano-wire (NW) transistor is expected to be used in sub-5nm technology nodes for its better electrostatic control. Junction-less (JL) NW is a feasible candidate, as steep source/drain junctions are not required. In this paper, Negative-Bias-Temperature-Instability (NBTI) of JL-NW is studied through calibrated TCAD simulation. It is found that JL NW has 20 times less NBTI degradation (in terms of oxide/channel fixed charge generation) than regular NW because of 40 times less hole carrier concentration at the oxide/channel interface and absence of field enhanced degradation. A novel operation scheme is then proposed to reduce NBTI degradation in analog circuit by switching the source and drain terminals periodically. The concept is verified through TCAD simulation of NW current mirror and it is found that NW NBTI degradation can be further reduced by 25% to 35% by using the novel scheme.**

Keywords—NBTI, Junctionless Nanowire, Reliability, TCAD Simulation, Analog Circuit, Current Mirror

I. INTRODUCTION

Nano-wire (NW) transistor is expected to be used in sub-5nm technology nodes for its better electrostatic control [1]. Junction-less (JL) NW, which has uniform doping in source/channel/drain regions, is expected to be easier to fabricate than regular NW as steep source/drain junctions are obviated [2]. The manufacturing cost is also expected to be lower in certain situations based on cost-of-ownership analysis [3]. It also has less temperature dependence for mobility and less dopant fluctuation induced channel length variation [4].

Negative-Bias-Temperature Instability (NBTI) means that the p-MOSFET's threshold voltage (V_{TH}) becomes more negative after ON-state operations (V_{GS} -V_{TH} < 0), resulting in lower drain current over time. It has been demonstrated that normally-on (V_{TH}>0) p-type JL FinFET is more immune to NBTI [5][6]. However, there is no detailed theoretical investigation on the NBTI of JL transistor nor JL NW. In this paper, through TCAD simulation, we study the NBTI in both normally-on and normally-off (V_{TH} < 0) p-type JL NW and the mechanism leading to less NBTI in JL NW than regular NW. After understanding the NBTI mechanism in NW, a novel operation scheme is proposed to minimize the NBTI degradation in analog circuits and verified through TCAD simulations [7].

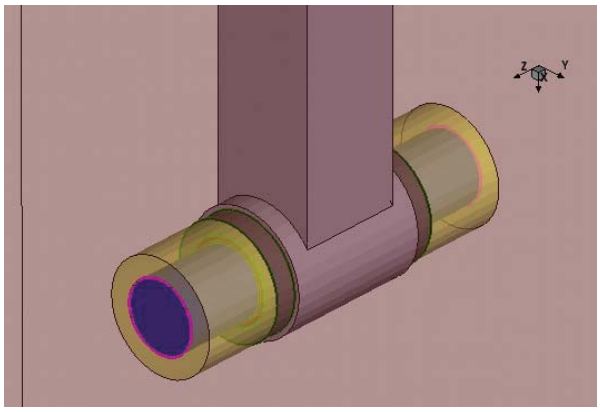

Fig.1. 3D NW structures used in the simulation. Diameter is 7nm and the gate length is 14nm. Total simulation domain is 1μm^3 to allow accurate simulation of hydrogen diffusion.

II. SIMULATION SETUP

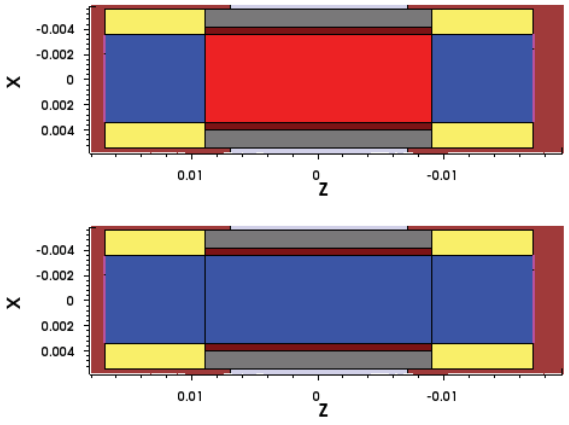

Fig. 2. 2D cross section of the nanowire in Fig. 1. Top is Regular nanowire and bottom is Junction-less nanowire. Both have gate underlap of 2nm. Blue: 10^{20}cm^{-3} p-doped. Red: undoped.

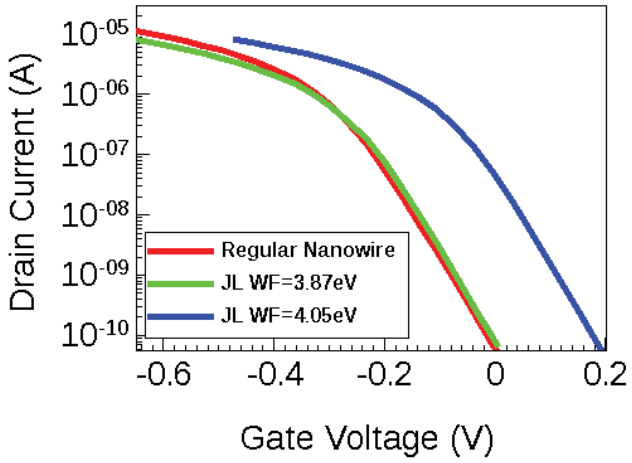

Fig. 3: I_DV_G curves of Regular Nanowire, Junction-less Nanowire (WF = 3.87eV is normally off; WF = 4.05eV is normally on). V_{DS} = -0.65V.

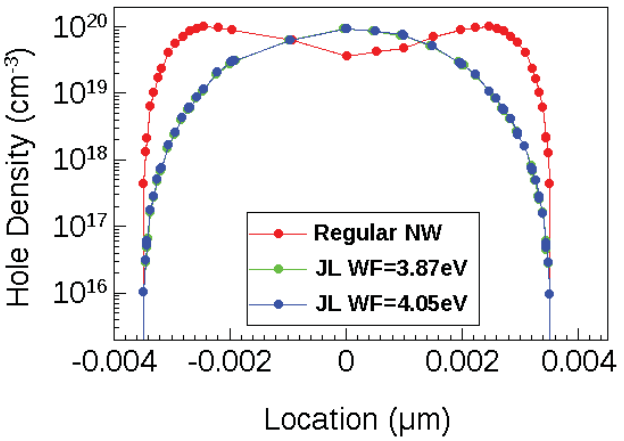

Fig. 5. Hole density along the diameter of the nanowires (0μm is the center of the NW) at V_G=-0.6V.

NBTI is due to electro-chemical reactions. The details of the model can be found in [8] and the model parameters used in the simulations have been calibrated to FinFET experiment [9]. In short, NBTI may be described by the following reversible electro-chemical reaction equations:

$$\text{Si-H } (1^{st} \text{ interface}) + \text{hole} \Leftrightarrow Si^{+} + H \quad (1)$$

$$\text{X-H } (2^{nd} \text{ interface}) + H \Leftrightarrow Si + H_2 \quad (2)$$

(1) represents the reaction at the gate interfacial oxide/channel interface (1^{st} interface) and (2) represents the reactions at the interfacial oxide/high-k oxide interface (2^{nd} interface). In order to model the NBTI, in addition to Poisson equation, and electron/hole continuity equations, hydrogen atom and molecule diffusion equations are also solved. Density gradient equation is also solved to account for quantum confinement effect. Multi-State-Configuration (MSC) in SDevice is used to model the changing of the interface states (Si-H, X-H, Si^{+}, Si etc.) [7]. All of them are solved self-consistently.

Figures 1 and 2 show the 3D structure used and their 2D cut planes, respectively. To attain accurate simulation, large enough simulation domain ($1\mu m^3$) is constructed to model the hydrogen atom and molecule diffusion (Fig. 1 and 2).

The S/D have $10^{20}cm^{-3}$ p-type doping. The channels of regular and JL NW have zero and $10^{20}cm^{-3}$ p-type doping, respectively. Gate workfunction (WF) of regular NW is 4.05eV. WF of normally-on and normally-off JL NW are 4.05eV and 3.87eV, respectively. Normally-off JL's gate WF is chosen to match the V_{TH} of regular NW (Fig. 3). Ballistic mobility is turned on and calibrated to sub-band Boltzmann transport simulation [10].

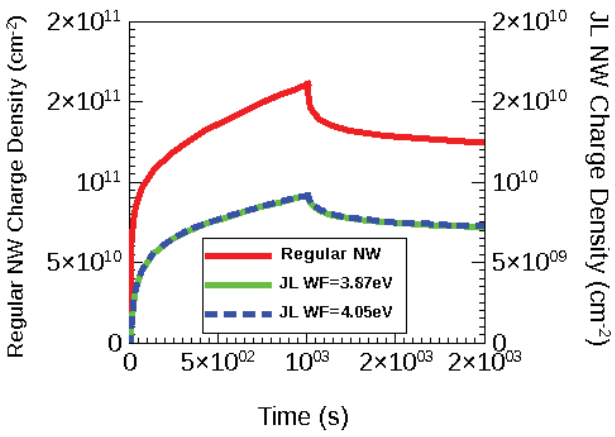

Fig. 4. Average Oxide/Channel interface charge density due to NBTI as a function of time. V_{DS} = 0V and V_G = -0.65V (-0.47V for WF = 4.05eV) during stress (0-1000s) and V_G = 0V (0.18V for WF = 4.05eV) during recovery (1000s-2000s). Left axis scale is 10X of right axis scale. Temperature = 300K.

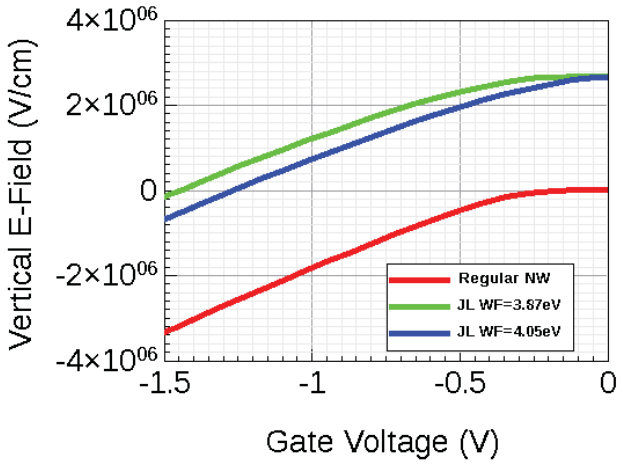

Fig. 6. Electric field perpendicular to Oxide/channel interface as a function of gate voltage applied to the nanowires. Positive (negative) value means the field is pointing from oxide (channel) to channel (oxide).

III. Junctionless Nanowire NBTI

Firstly, degradation due to NBTI in regular NW is compared to that of normally-off JL NW with the same V_{TH} (Gate WF = 3.87eV, Fig. 3). The devices are stressed at V_G = -0.65V with V_D = V_S = 0V at 300K for 1000s and then relaxed at V_G = 0V for another 1000s. As shown in Fig. 4, JL NW has 20 times less oxide/channel interface charge generation by NBTI. This trend is consistent with the FinFET experimental result in [6].

This is due to two reasons. One is that the peak hole density is at the center of the wire in JL case while it is closer to the oxide/channel interface in regular NW when the NW is at ON-state. As a result, JL has 40 times less hole density (Fig. 5) at the oxide/channel interface. According to (1), holes are required to react with Si-H bonds at the oxide/channel interface to initiate degradation. Therefore, lower hole density at the interface reduces NBTI in JL NW.

Another reason is due to the lack of field enhancement in JL NW. As shown in Fig. 6, the electric field always points from oxide into the channel even the gate voltage is as large as 1.4V. Therefore, there will be no field enhancement to help holes tunnel through the Si-H bond barrier for chemical reactions.

Normally-off JL NW needs unusual gate WF or special channel engineering [11]. It is thus important to study also the normally-on JL NW which might be used in some circuitries. For fair comparison, the stress and relax gate voltages are set to -0.47V and 0.18V respectively so that they are compared at the same gate overdrive (V_G-V_{TH}) and leakage current. Figures 4, 5 and 6 show that it has similar results as normally-off JL NW.

IV. Novel Scheme to Reduce NBTI in Analog Circuits

For space applications [12] and Internet-of-Things, it is mandatory to reduce the degradation due NBTI to extend the circuitry lifetime without replacement. Unlike digital circuits, analog circuits are usually stressed in *ON*-state continuously for long time. To alleviate NBTI degradation, it is proposed to operate the transistor by swapping/switching periodically the source and drain terminals in the circuit.

Figure 7 shows the circuit schematic of a current mirror. The transistor on the right is biased at ON-state continuously during normal operation. It should be noted that it is also biased in saturation mode with $|V_{GD}| < |V_{TH}|$. As a result, the gate oxide electric field near the source is much larger than the electric field near the drain and, thus, NBTI occurs mostly near the source.

If this is a critical circuit, extra circuitry can be added so that the source and drain will be swapped periodically. During half of the period, one terminal of the transistor will act as the source and degrade faster than the other terminal, which acts as the drain. In the other half of the period, NBTI degradation occurs faster at the source terminal which was previously the drain. As a result, NBTI degradation will distribute more evenly from source to drain along the oxide/channel interface than without the switching scheme. Moreover, since the effect of NBTI degradation is by increasing the $|V_{TH}|$, and thus

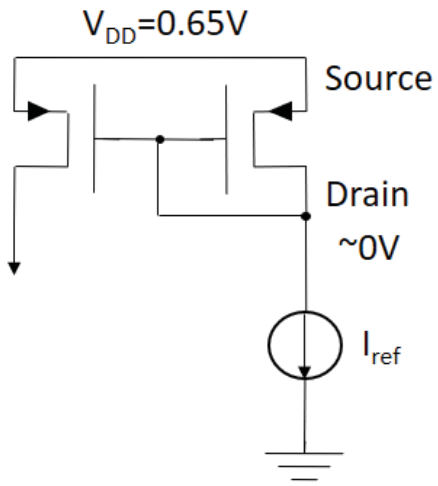

Fig. 7: A typical current mirror circuit. The right transistor is biased at saturation mode with V_{DS} = V_{GS} ~ -V_{DD}. The proposed switching scheme is to alternate the Source and Drain of the right transistor through switches.

degrades the drive current and transconductance, it has much smaller effect if it occurs at the drain side for transistor in saturation mode. Therefore, such switching scheme is expected to reduce the impact on NBTI on analog circuits as degradation at the source side is reduced (due to more even distribution), while the increase of degradation at the drain side has minor impact on transistor performance.

Such scheme is simulated using TCAD on both the regular and JL NW in Figures 1 and 2. Without switching, as shown in Fig. 8, both NW experience monotonic increase of NBTI degradation (increase of interface negative fixed charge). By

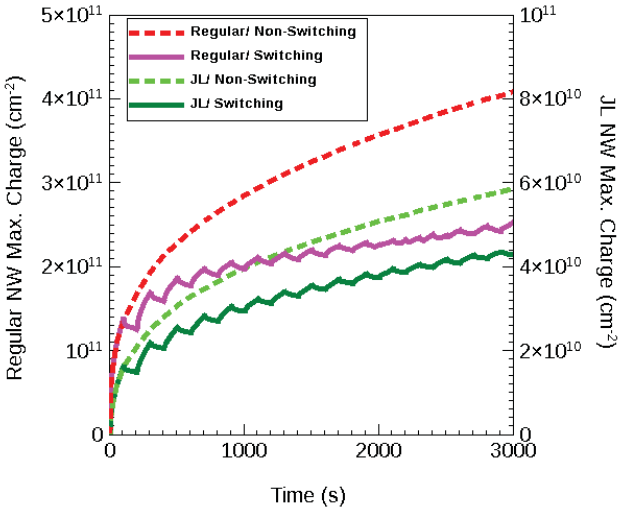

Fig. 8. Maximum Oxide/Channel interface charge density due to NBTI as a function of time for the right transistor in Fig. 7. V_G = -0.65V. For non-switching cases, V_D = -0.65V and V_S = 0V. For switching cases, V_D (V_S) switches between -0.65V (0V) to 0V (-0.65V) every 100s.

using the switching scheme (swapping source and drain every other 100s, i.e. period = 200s), Fig. 8 shows that the peak interface charge due to NBTI can be reduced by 25% and 35%, respectively, for JL and regular NW. This means that by using the switching scheme, the circuit lifetime will be extended if NBTI is the dominant degradation mechanism.

Fig. 9 plots the interface change distribution due to NBTI degradation from source to drain at time = 3000s. It shows that the source side interface charge is reduced significantly in the switching scheme as expected. Although the drain side charge increases in the switching scheme, since V_{TH} and I_D depend more on the source side charge, this scheme gives 25% less degradation in V_{TH} based on I_DV_G simulation.

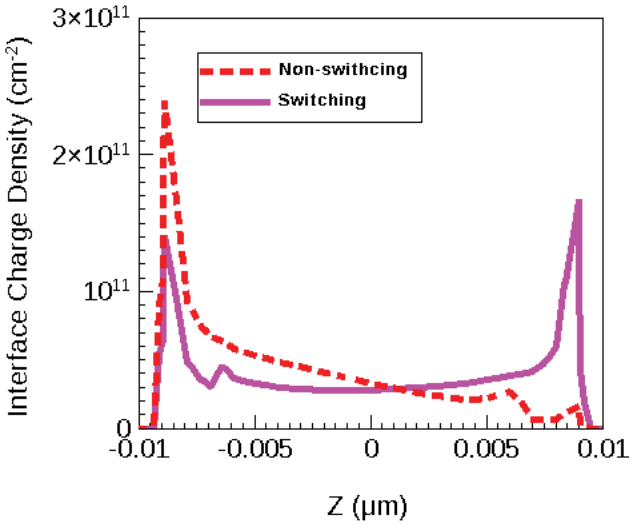

Fig. 9. Oxide/Channel interface charge density due to NBTI from source to drain for switching and non-switching cases. Both taken at time = 3000s of Fig. 8.

V. Conclusion

Using TCAD simulations with NBTI parameters calibrated to FinFET experiments and ballistic mobility calibrated to sub-band Boltzmann transport simulations, we show that both normally-off and normally-on JL NW have much better NBTI immunity than regular NW. With the framework developed, we propose and simulate a novel switching scheme to alleviate the impact of NBTI degradation in analog circuit resulting in 25%-35% less fixed charge generation.

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