Modeling of Process (Ge, N) Dependence and Mechanical Strain Impact on NBTI in HKMG SiGe GF FDSOI p-MOSFETs and RMG p-FinFETs

N. Parihar[1], R. Tiwari[1], C. Ndiaye[2], M. Arabi[2], S. Mhira[2], H. Wong[3], S. Motzny[3], V. Moroz[3], V. Huard[2] and S. Mahapatra[1]

[1]Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India
[2]STMicroelectronics, 850 rue Jean Monnet 38926, Crolles, France [3]Synopsys Inc., Mountain View, CA 94043, USA
*Phone: +91-222-572-0408, Email: souvik@ee.iitb.ac.in

***Abstract*— A physical framework is used to model time kinetics of Negative Bias Temperature Instability (NBTI) in Si and SiGe FDSOI p-MOSFETs and p-FinFETs. The effects of Germanium (Ge%) in the channel and Nitrogen (N%) in the High-K Metal Gate (HKMG) gate stack are explained. Mechanical strain effects in terms of STI to active distance (SA) for FDSOI and channel length (L) scaling for FinFET are explained. Band structure is calculated to correlate the process (Ge%, N%, strain) impact on device degradation. The model is included in Sentaurus Device TCAD to predict NBTI kinetics in Si and SiGe FinFETs.**

Keywords— NBTI, FDSOI, FinFET, GF, RMG, SiGe channel, mechanical strain, layout, L scaling, RD model

I. Introduction and Background

Negative Bias Temperature Instability (NBTI) is a serious reliability concern for p channel FDSOI MOSFET and FinFET devices [1], [2]. Modeling of threshold voltage shift (ΔV_T) time kinetics during and after NBTI stress is of importance, as it can be used to extrapolate the measured data from accelerated short time DC and/or AC stress to end of life (EOL) at use condition. Although the physical mechanism is debated [3], [4], the model of [5] can predict NBTI kinetics over different technologies [5] -[10]. It uses uncorrelated contributions from interface (ΔV_{IT}) and bulk (ΔV_{OT}) trap generation and hole trapping (ΔV_{HT}) in pre-existing traps to calculate overall ΔV_T. It has been used to predict ΔV_T stress and recovery kinetics during and after DC and AC stress in Gate First (GF) HKMG planar devices having different gate stack N% [5], Replacement Metal Gate (RMG) HKMG SOI FinFETs for wide temperature (T) range [6], and RMG HKMG Si and SiGe bulk FinFETs having different Ge% and N% [7], [8]. The Si capped SiGe planar MOSFETs having different cap and quantum well (QW) thickness and Ge% in QW [9], and FDSOI devices with different Ge% and N% [10] have also been modeled. All of this is achieved by using only 9 technology dependent adjustable model parameters [5].

II. Scope of this Work and Experimental Details

The framework of [5] is used to analyze NBTI in HKMG Si and SiGe GF p-FDSOI [10] and RMG p-FinFET [7] devices with different Ge%, N% and mechanical strain (STI to active distance for FDSOI, L dependence for FinFET). Fig.1 shows the schematic of the model framework used to model the ΔV_T kinetics. Reaction-Diffusion (RD) model is used for interface trap generation (ΔN_{IT}), and Transient Trap Occupancy Model (TTOM) is used for charge occupancy of these traps and their contribution (ΔV_{IT}), and analytical equations are used for both ΔV_{HT} and ΔV_{OT}. The model is validated against experimental data obtained by ultra-fast (UF) 10μs delay measurement method. ΔV_{IT} is shown to dominate EOL ΔV_T at use condition for both FDSOI and FinFET technologies. Si-H bond dissociation that results in ΔN_{IT} generation is modeled using an inversion layer hole and oxide electric field (E_{OX}) driven process [11], Fig.2, and it depends on tunneling effective mass (m_T), barrier height (φ_B), polarization factor (α), and T activation (E_{AKF1}). The m_T and φ_B values for Si and SiGe 100 (FDSOI) and 110 (FinFET) surfaces are obtained by band structure calculations using the tight binding approach [12], with mechanical strain obtained from measurements for FDSOI and calculated using Sentaurus Process [13] for FinFET. Sentaurus Device [14] is enabled for calculating ΔN_{IT} kinetics using RD model. The TCAD based framework is used to predict the NBTI time kinetics for Si and SiGe p-FinFETs under different stress bias (V_{GSTR}) and T.

III. Modeling of NBTI in FDSOI MOSFET

The framework of Fig.1 is used to study different FDSOI processes (Table-I) and mechanical strain due to varying SA. Higher stress is seen for longer SA due to relaxation of strain near STI, as illustrated in Fig.3. Fig.4 and Fig.5, respectively, show the modeling of time kinetics during and after DC stress. The model subcomponents and overall prediction for a fixed V_{GSTR} and T (Fig.4 (a) and Fig.5 (a)), and overall prediction for multiple V_{GSTR} at a fixed T are shown (Fig.4 (b) and Fig.5 (b)). The ΔV_{IT} shows power law time dependence with time exponent of ~1/6 during stress. During recovery, a fraction of ΔV_{IT} recovers fast by capturing electrons from the substrate and the remaining ΔV_{IT} recovers slowly by trap re-passivation [5]. The ΔV_{HT} saturates at long time and recovers fast, while ΔV_{OT} shows power law time dependence with time exponent ~1/3 and recovers slowly. Fig.6 shows the model prediction and subcomponents for (a) fixed V_{GSTR} and T, and (b) overall prediction for different V_{GSTR} at a fixed T during AC stress. The hole trapping contribution is negligible for AC stress and explained in [5]. Fig.7 and Fig.8, respectively, show the time kinetics during and after DC stress for different processes under two different SA. The degradation reduces as SA is increased (due to increase in mechanical strain). Fig.9 shows the measured and modeled ΔV_T at fixed time versus SA for different Ge% and N% (Processes: P2 to P5) along with

underlying subcomponents. Somewhat higher ΔV_{OT} than ΔV_{IT} is seen at higher V_{GSTR} for stress, and ΔV_{HT} is negligible. Both ΔV_{OT} and ΔV_{HT} remain constant for different SA, while ΔV_{IT} reduces and controls the SA dependence of ΔV_T. Fig.10 shows the V_{GSTR} dependence of fixed time ΔV_T for processes having different Ge%. The higher voltage acceleration factor (VAF) of ΔV_{IT} and relatively higher ΔV_{OT} (VAF for ΔV_{OT} is high [5]) contribution increases the overall VAF for higher Ge%. Fig.11 shows the V_{GSTR} dependence of ΔV_T and the subcomponents for Si (Process P0) and SiGe (Process P5). ΔV_{IT} dominates the degradation for lower V_{GSTR} conditions. As VAF is higher for ΔV_{OT} compared to ΔV_{IT} (Fig.11), the EOL ΔV_T is dominated by ΔV_{IT} for all process conditions; refer to Fig.12. Further, the similarity of stress and recovery kinetics of ΔV_T and the body coefficient (m) suggest role of ΔN_{IT}, as shown in Fig.13. It is therefore important to model the process dependence of ΔV_{IT}.

IV. Modeling of NBTI in FinFET

Fig.14 and Fig.15, respectively, show the model prediction of measured time kinetics along with model subcomponent for lowest dataset during and after DC stress for different V_{GSTR} and T. Power law time dependence is seen at longer time with exponent (n) of ~1/6 and ~1/3 respectively for ΔV_{IT} and ΔV_{OT}, and ΔV_{HT} is negligible for SiGe devices due to unfavorable defect band alignment and increase in valence band offset [7], [15]. The time kinetics during and after AC stress is modeled in Fig.16 and Fig.17 respectively. Similar analysis is done for different Ge% and N%. Fig.18 shows the V_{GSTR} dependence of fixed time ΔV_T at different T for Si and SiGe with different Ge% and N%. Model subcomponents are shown for the lowest dataset. ΔV_T reduces but VAF increases with increase in Ge%, while ΔV_T increases but VAF reduces with increase in N%. The T dependence of VAF (lower VAF at higher T) is higher for higher Ge% but lower for higher N%. Higher Ge% in the channel reduces all subcomponents and hence ΔV_T, while high N% increases ΔV_{IT} and ΔV_{HT} but reduces ΔV_{OT} [7]. However, the increase in ΔV_{IT} is higher than the reduction in ΔV_{OT}, so the overall ΔV_T increases with increase in N%. The EOL ΔV_T is found to be dominated by ΔV_{IT}, as shown in Fig.19, except for very high Ge% that is not under active consideration. The ΔV_{HT} contribution is negligible for all processes. Fig.20 shows the time evolution of DC stress kinetics for different L in SiGe devices. The mechanical strain from SiGe (Ge=50%) Source/ Drain (S/D) increases at lower L, which reduces the ΔV_{IT} and hence ΔV_T as explained below. The V_{GSTR} dependence of ΔV_T is modeled in Fig.21. The VAF increases with reduction in L (due to increase in strain), similar trend has been shown for Si FinFETs as explained in a companion paper [16].

V. Physical Mechanism

Inversion layer holes tunnel to interfacial Si-H bonds that are already stretched due to polarization in E_{OX}, get captured and make them weak, and are subsequently broken by thermal activation, Fig.2 [11]. The bond dissociation depends on the pre-factor (k_{FIT}), field acceleration (Γ_E) as well as T activation energy (E_{AKF1}); Γ_E consists of a T independent factor (Γ_0) and its T dependence enters by the polarization term (α) [11]. Both k_{FIT} and Γ_0 depend on the valence band (VB) barrier height (φ_B) and tunnel effective mass (m_T). Band structure (Fig.22) calculations suggest increase in φ_B with increase in Ge% while m_T remains almost unchanged for the range of Ge% studied here, and these hold for both (100) and (110) surfaces. Fig.23 (a) plots the change in φ_B as a function of Ge%, calculated for Ultra-Thin-Body (UTB) and for (100) surface (FDSOI). As a consequence, both k_{FIT} and Γ_0 reduce at higher Ge% as shown respectively in Fig.24 (a) and Fig.25 (a), causing lower ΔV_{IT}. However, overall Γ_E increases with Ge% due to higher α [7]. Higher α also results in increased T dependence of VAF for SiGe devices; see Fig.18. Note, higher Γ_E for ΔV_{IT} and higher (relative) ΔV_{OT} contribution (with higher VAF) increases the VAF of ΔV_T at higher Ge% across different SiGe technologies [7]-[10]. Higher N% reduces φ_B and m_T (from gate leakage modeling [17]), resulting in higher k_{FIT} (Fig.24 (b)) and ΔV_{IT}, and is consistent with [18]. N% causes negligible change in Γ_0 (Fig.25 (b)); the change in VAF with N% is due to the change in k of the IL (increased k at higher N%), which changes the IL field [7] (VAF changes while Γ_E does not change).

For (100) surface (FDSOI devices), the top hole (TH) band lifts up with uniaxial compressive strain (UCS) and increases φ_B, see Fig.23 (b). The m_T for the TH band increases initially with UCS but shows no further change at higher values (above 1GPa) [19]. Lower ΔV_{IT} at high SA (Fig.8) is due to the lower k_{FIT} (higher φ_B, and higher m_T for lower strain values) owing to higher strain (Fig.9). For (110) surface (sidewall of FinFETs), the φ_B remains almost unchanged but m_T increases with strain [19] and hence reduces the k_{FIT} significantly. Both increase in φ_B and/or m_T results in a reduction of k_{FIT} and an increase in Γ_0, as shown in Fig.26.

VI. TCAD Implementation and Simulations

The earlier RD model implementation [20] is enhanced by proper Si-H bond dissociation mechanism (Fig.2) and density gradient (quantum corrected) hole density to calculate kinetics of ΔV_{IT} at the channel/IL and IL/HK interfaces (Fig.27). Band structure calculated parameters (k_{FIT} and Γ_0) are used. TCAD can predict the stress time kinetics (Fig.28) and fixed time ΔN_{IT} versus V_{GSTR} at different T (Fig.29) for Si and SiGe p-FinFETs. Only 2 free parameters are needed for RD model, as other 2 are obtained from band structure calculations, reducing the adjustable parameters of full framework (Fig.1) to 7.

VII. Conclusion

EOL ΔV_T in Si and SiGe p-FDSOI and p-FinFETs at use condition is dominated by ΔV_{IT}. Both ΔV_T and ΔV_{IT} reduce at higher Ge% and compressive strain but increase at higher N%. Band structure calculations explain the process impact of Si-H bond dissociation that governs ΔV_{IT}. TCAD implementation of the framework helps calculation of ΔV_{IT} kinetics using proper parameters, 3D electrostatics and quantum effects.

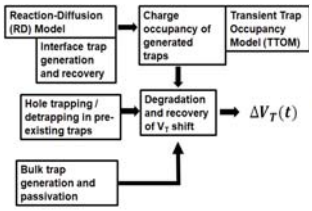


Fig.1. Schematic of a comprehensive NBTI modeling framework consisting of uncorrelted ΔV_{IT}, ΔV_{HT} and ΔV_{OT} components.

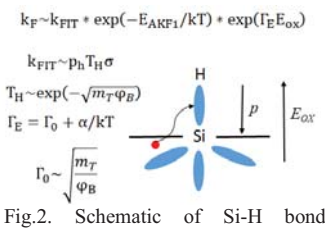


Fig.2. Schematic of Si-H bond dissociation at the channel/IL interface. Inversion layer holes tunnel into interfacial Si-H bonds aided by the oxide electric field (E_{OX}).

Process	Channel Germanium (in %)	TIN Thickness (nm)	Nitridation Level
P1	0	45	High
P2	25	45	High
P3	30	45	High
P4	30	10	Low
P5	34	10	Low

Table-I:. Process description of all FDSOI devices analyzed, having different channel Ge% and N% in gate stack (N% changed by TiN thickness).

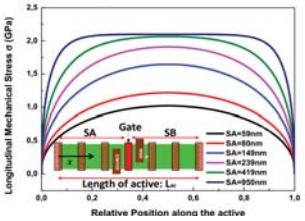


Fig.3. Stress profiles along the active for various STI to Gate length (SA).

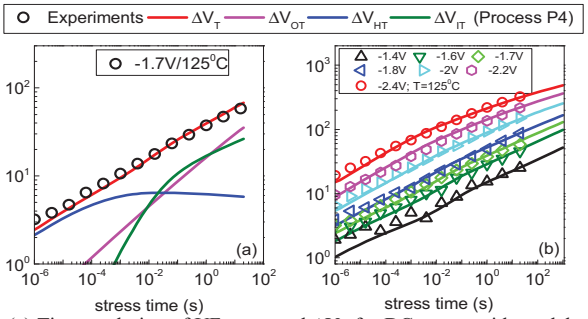


Fig.4 (a) Time evolution of UF measured ΔV_T for DC stress, with model prediction and different subcomponents at fixed V_{GSTR} and T. (b) Model prediction of UF measured ΔV_T for DC stress for multiple V_{GSTR}.

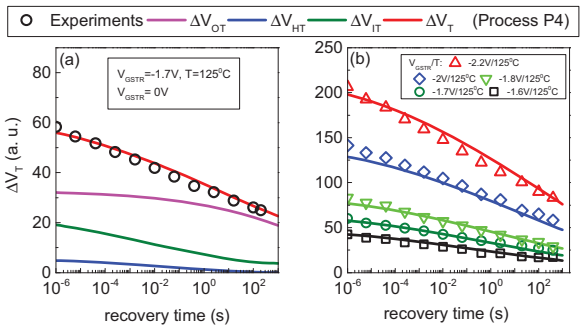


Fig.5 (a) Time evolution of UF measured ΔV_T for recovery after DC stress, with model prediction and different subcomponents at fixed V_{GSTR} and T. (b) Model prediction of UF measured ΔV_T for recovery after DC stress for multiple V_{GSTR}.

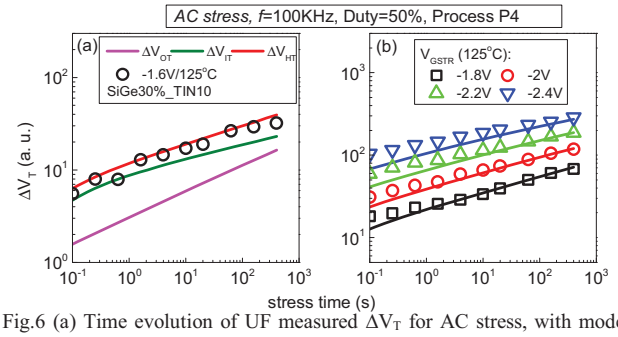


Fig.6 (a) Time evolution of UF measured ΔV_T for AC stress, with model prediction and different subcomponents at fixed V_{GSTR} and T. (b) Model prediction of UF measured ΔV_T for AC stress for multiple V_{GSTR}.

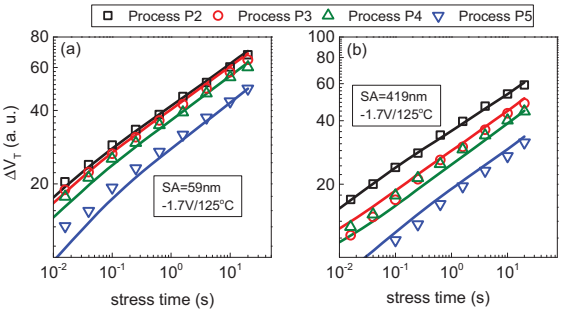


Fig.7. Model prediction of UF measured ΔV_T for DC stress for different Ge% in the channel and N% in the gate stack for (a) SA=59 and (b) SA=419. ΔV_T reduces with increases in SA.

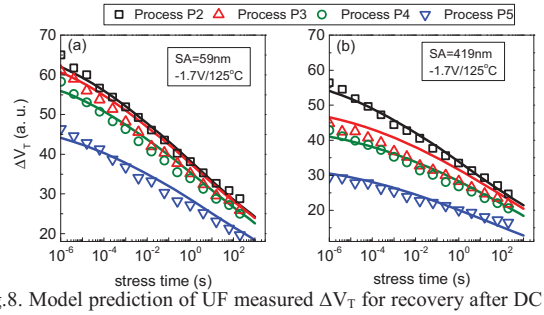


Fig.8. Model prediction of UF measured ΔV_T for recovery after DC stress for different Ge% in the channel and N% in the gate stack for (a) SA=59 and (b) SA=419.

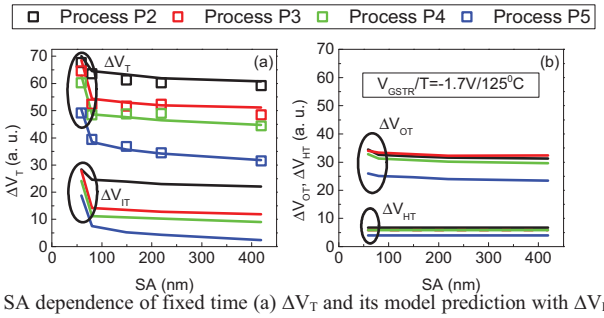


Fig.9. SA dependence of fixed time (a) ΔV_T and its model prediction with ΔV_{IT} subcomponent and (b) ΔV_{HT} and ΔV_{OT} subcomponents, for DC stress in FDSOI having different processes. SA induced variation is due to changes in ΔV_{IT}.

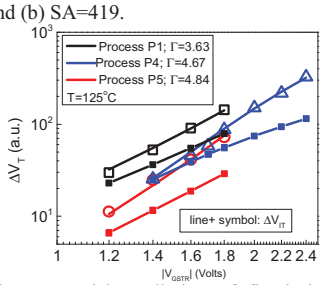


Fig.10. Model prediction of fixed time ΔV_T for different processes. ΔV_{IT} shown by line + symbols.

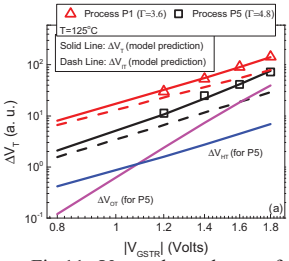


Fig.11. V_{GSTR} dependence of fixed time degradation for Si and SiGe devices. The ΔV_{IT} (dash line) at operating voltage is close to ΔV_T.

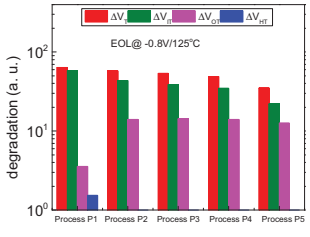


Fig.12. EOL ΔV_T at operating conditions and underlying subcomponents for Ge% and N% changes in FDSOI devices.

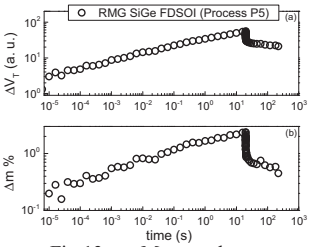


Fig.13. Measured stress-recovery time kinetics for (a) ΔV_T, and (b) body coefficient (m).

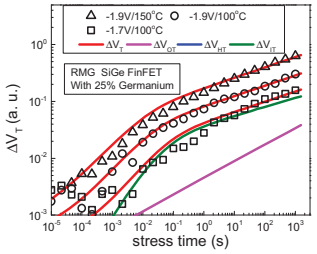


Fig.14. Prediction of stress kinetics in RMG SiGe p-FinFET during DC stress for different V_{GSTR} and T. Subcomponents for the lowest dataset are shown.

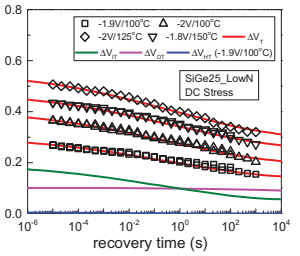


Fig.15. Prediction of recovery kinetics in RMG SiGe p-FinFET after DC stress for different V_{GSTR} and T. Subcomponents for the lowest dataset are shown.

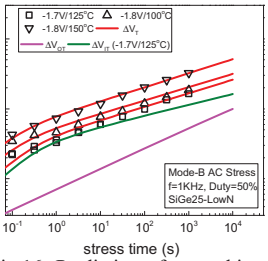


Fig.16. Prediction of stress kinetics in RMG SiGe p-FinFET during AC stress for different V_{GSTR} and T. Subcomponents for the lowest dataset are shown.

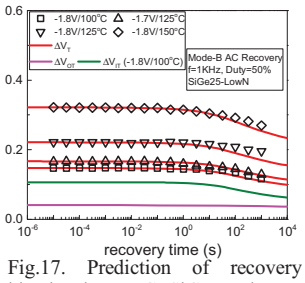
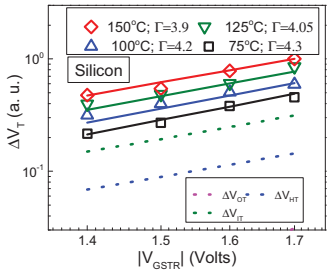
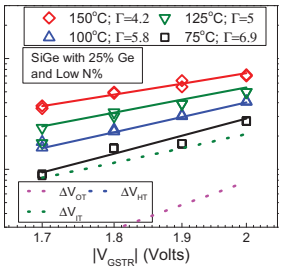


Fig.17. Prediction of recovery kinetics in RMG SiGe p-FinFET after AC stress for different V_{GSTR} and T. Subcomponents for the lowest dataset are shown.





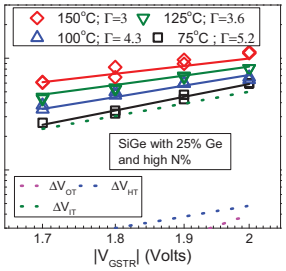


Fig.18. Model prediction of measured fixed time ΔV_T versus V_{GSTR} at different T for Si and SiGe RMG p-FinFETs with different N%. VAF decreases with T. VAF (iso-T) increases with increase in Ge% and reduces with increase in N%.

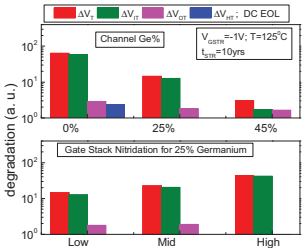
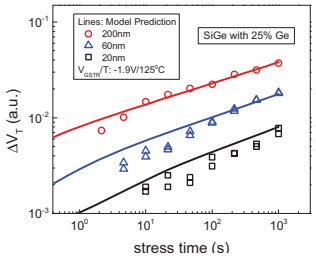


Fig.19. EOL ΔV_T under operating conditions and underlying subcomponents for different Ge% (top) and different N%.



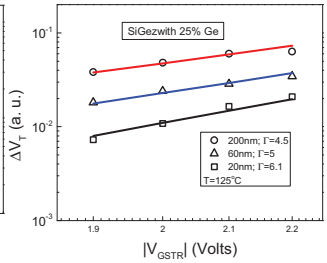


Fig.20. Prediction of ΔV_T time kinetics for different channel length at fixed V_{GSTR}/T. ΔV_T reduces with reduction in L.

Fig.21. Prediction of ΔV_T as a function of V_{GSTR} for different channel length.

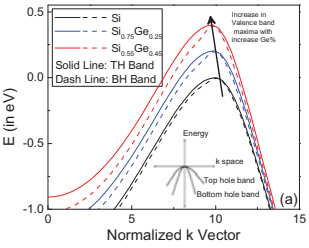


Fig.22. Simulated top and bottom hole (TH and BH) bands for Si and SiGe showing strong Ge% impact on the barrier φ_B.

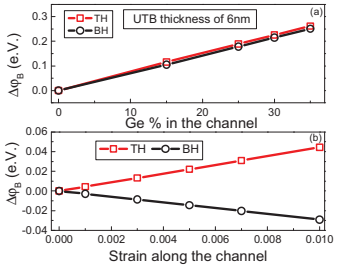


Fig.23. (a) Channel Ge% impact on TH and BH bands. (b) Uniaxial compressive strain impact on TH and BH bands.

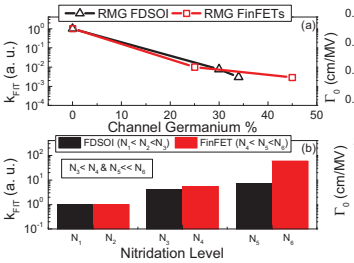


Fig.24. ΔV_{IT} pre-factor as a function of (a) channel Ge% and (b) N% in IL. It reduces with higher Ge% but increases with higher N%.

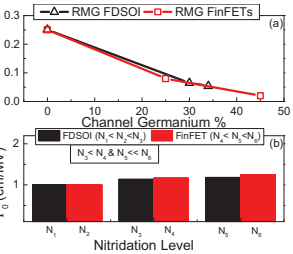


Fig.25. Tunneling parameter (Γ_0) as a function of (a) channel Ge% and (b) N% in IL. Γ_0 reduces with Ge% due to change in φ_B, but weakly depend on gate stack N%.

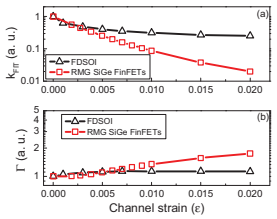


Fig.26. Mechanical strain dependence of (a) ΔV_{IT} pre-factor k_{FIT} and (b) tunneling parameter (Γ_0). FinFETs shows steeper strain dependence due to (110) sidewall.

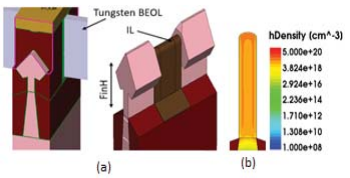
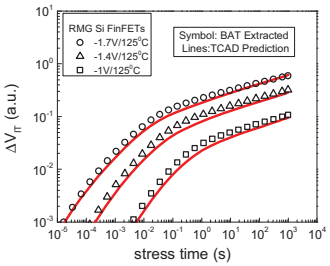


Fig.27. (a) TCAD [13] structure used for Si and SiGe FinFET simulation. (b) Hole density profile in channel Fin. Proper mechanism for Si-H bond dissociation (Fig.2) is used.



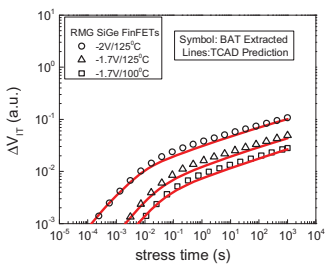
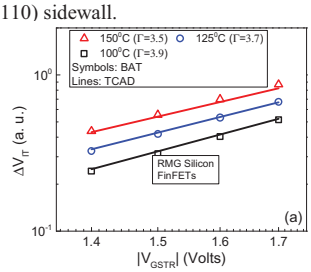


Fig.28. TCAD prediction of ΔV_{IT} stress time kinetics (extracted from analysis of p-FinFETs) at different V_{GSTR} and T for Si (left) and SiGe (right) p-FinFETs.



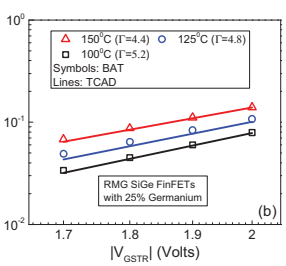


Fig.29. TCAD prediction of fixed time ΔV_{IT} (extracted from measured ΔV_T) as a function of V_{GSTR} at different T, for (a) Si channel and (b) SiGe channel with 25% Germanium RMG FinFETs. SiGe devices show higher VAF and larger T impact of VAF due to polarization (see Fig.2).

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