Consistent Modeling of Snapback Phenomenon Based on Conventional I-V Measurements

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***Abstract*— The snapback phenomenon is investigated with use of 2D-device simulations. It is found that the phenomenon is induced by three sequentially occurring mechanisms: 1. Impact ionization, 2. Potential increase, and 3. Bipolar effect. Further, it is demonstrated that this series of mechanisms can be successfully modeled with use of the compact model HiSIM_HV by introducing an internal node within the substrate, which is solved in a consistent way. The node is verified to describe the new induced electrical balance correctly. It is demonstrated that the node potential change is the origin of the three involved mechanisms. The reason for the achieved simple but accurate modeling is mainly related to the potential-based modeling approach of HiSIM_HV adopted for the basic *I-V* modeling, which is influenced by the internal node potential as well.**

Keywords—snapback, impact ionization, bipolar effects, MOSFETs, circuit simulation, compact model

I. Introduction

Device reliability is an important issue. In particular, device breakdown and degradation must be predicted accurately. In power devices, the snapback phenomenon [1] is well-known and constrains a safe-operating-area (SOA). Additionally, accurate snapback modeling becomes of increased importance for circuit-level simulation when considering electro-static discharge (ESD) events, because it is an appropriate approach for realizing consistent simulation which bridges from device to circuit level. On the device level, the SOA must be properly identified. Further, for confirming the reliability of on-chip ESD protection circuitry, circuit simulation is needed which considers the snapback phenomenon. To achieve these objectives, an accurate compact model has been needed for a long time.

II. Analysis of Snapback Phenomenon

2D device simulation [2] was utilized to investigate internal physical mechanisms in the course of the snapback phenomenon. Focused here is DC static analysis. Even in DC static analysis, the snapback phenomenon occurs, as shown in the simulation result of Fig. 1 for the current sweep characteristics, where the drain voltage sweep is shown for comparison.

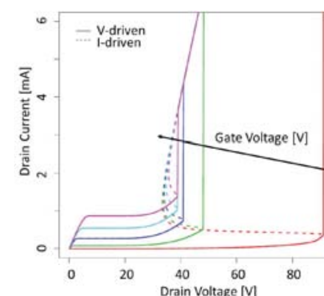

Fig. 1. Simulated drain current vs voltage characteristics using a circuit simulator together with a developed model for snapback in this work. "V-driven" (solid lines) and "I-driven" (dotted lines) simulations sweep drain voltage and drain current, respectively.

Fig. 2 shows 2D-device simulation results of a laterally diffused drain MOS (LDMOS) at V_{gs}=12V, while the drain bias is varied. The potential distributions for the three bias conditions, identified by red solid circles, are depicted together. Even at the grounded source side in the channel, the potential does not reduce to a small value but remains relatively high for high V_{ds} values. Further, the equipotential contour along the channel direction is observed to extend to the whole substrate.

Fig. 3 explains the mechanisms leading to the snapback phenomenon. Different current flows are depicted by different colors. The hole-current flow to the substrate remains rather small and the largest current flow is between source and drain, where the drain current and the source current are distinguished. Origins of the current characteristics are given. Figs.4a and b show the carrier distribution change for the studied V_{ds} values and I_{ds}=1mA (see Fig. 3) along the line A-B. The impact-ionization increases the carrier density (mechanism I), which results in the potential increase within the substrate (mechanism II, See Fig. 4c). This potential increase, namely the reduction of the p/n junction barrier at the source side, induces a junction current flow at the source side (mechanism III). This third mechanism is a bipolar carrier flow induced by the potential distribution deep in the substrate, as observed in Fig. 2.

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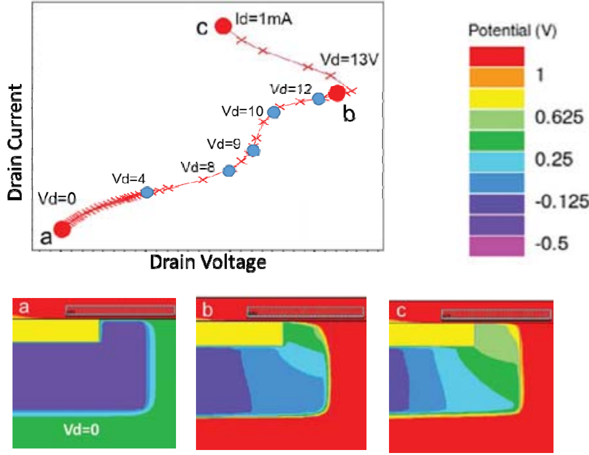

Fig. 2. 2D device simulation results for an LDMOS structure at V_{gs}=12 V. On its way of sweeping bias conditions, simulator changes over from voltage sweep to current sweep. The upper diagram is drain current vs drain voltage characteristics. Potential distributions are also shown for three selected bias points, identified by red solid circles in the graph. In due course of bias sweeping, the potential at the body region starts to raise and uphold at the source-body junction. This results in forward-biasing of the junction.

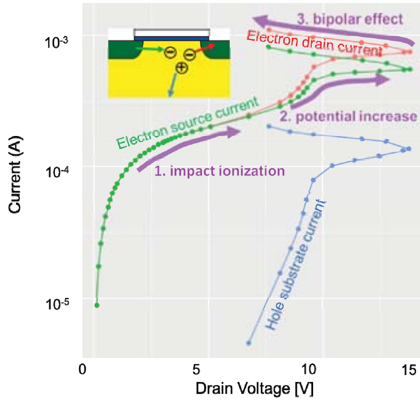

Fig. 3. 2D device simulation results for the same LDMOS structure. Green, red, ane blue lines represent electron source current, electron drain current, and hole substrate current.

III. Modeling for Three Mechanisms

Three sequentially occurred mechanisms are origins of the snapback phenomenon, and their modeling is presented here. The assembly of the developed models is depicted in Fig. 5 as an equivalent circuit.

A. Impact ionization

Impact ionization is typically modeled as A exp(-B/V) [4] in its simplest form, where A and B are model parameters, and V is the voltage drop across the high electric-field region at the drain junction. These model parameters can be determined through fitting to conventional measured substrate current-voltage characteristics.

I_{sub} (in Fig. 5) consists of two parts as in

$$I_{sub} = \alpha_1 \cdot I_{ds} + (1+\alpha_2)\cdot I_{bs} \tag{1}$$

where α_1 represents the impact ionization coefficient for the MOSFET channel current I_{ds} and α_2 represents that for the source-injected current I_{bs} (See (10) later). The formula for the first term is given in [5]. The latter is a new term introduced in this work and its impact ionization coefficient α_2 is expressed as

$$\alpha_2 = X_{sub1SNP} \cdot P_{sisubsatSNP} \cdot \exp\left(-\frac{X_{sub2SNP}}{P_{sisubsatSNP}}\right) \tag{2}$$

$$X_{sub1SNP} = \mathbf{SUB1SNP} \cdot \left(1+\frac{\mathbf{SUB1L}}{L_{gate}^{\mathbf{SUB1LP}}}\right) \cdot X_{subTmp} \tag{3}$$

$$X_{sub2SNP} = \mathbf{SUB2SNP} \cdot \left(1+\frac{\mathbf{SUB2L}}{L_{gate}}\right) \cdot \frac{1}{X_{subTmp}} \tag{4}$$

$$P_{sisubsatSNP} = \mathbf{SVDSSNP} \cdot V_{ds} + \phi_{S0} - \frac{L_{gate} \cdot P_{sislsat}}{X_{gate} + L_{gate}} \tag{5}$$

where **SUB1SNP**, **SUB2SNP**, **SVDSSNP**, **SUB1L**, and **SUB2L** are model parameters, and L_{gate} and ϕ_{S0} are gate length and source-side surface potential, respectively. These expressions take the same functional forms [5] as those for α_1 except for a flexibility of allowing different model parameter values from those for α_1. X_{subTmp} is a temperature dependent factor expressed as [5]

$$X_{subTmp} = 1 + \mathbf{SUBTMP} \cdot (T - \mathbf{TNOM}) \tag{6}$$

where **SUBTMP** is a temperature coefficient and **TNOM** is the nominal temperature and T is temperature. Psislsat in (4) is expressed as [5]

$$P_{sislsat} = V_{g2} + \frac{q \cdot \varepsilon_{Si} \cdot N_{sub}}{C_{ox}^2} \cdot \left\{1 - \sqrt{1 + \frac{2C_{ox}^2}{q \cdot \varepsilon_{Si} \cdot N_{sub}} \cdot \left(V_{g2} - \frac{1}{\beta} - X_{vbs} \cdot V_{bs}\right)}\right\} \tag{7}$$

where V_{g2} and X_{vbs} are expressed as [5]

$$V_{g2} = \mathbf{SVGS} \cdot \left(1+\frac{\mathbf{SVGSL}}{L_{gate}^{\mathbf{SVGSLP}}}\right) \cdot \frac{W_{gate}^{\mathbf{SVGSWP}}}{W_{gate}^{\mathbf{SVGSWP}} + \mathbf{SVGSW}} \cdot (V_{gs} - V_{fb}) \tag{8}$$

$$X_{vbs} = \mathbf{SVBS} \cdot \left(1+\frac{\mathbf{SVBSL}}{L_{gate}^{\mathbf{SVBSLP}}}\right) \tag{9}$$

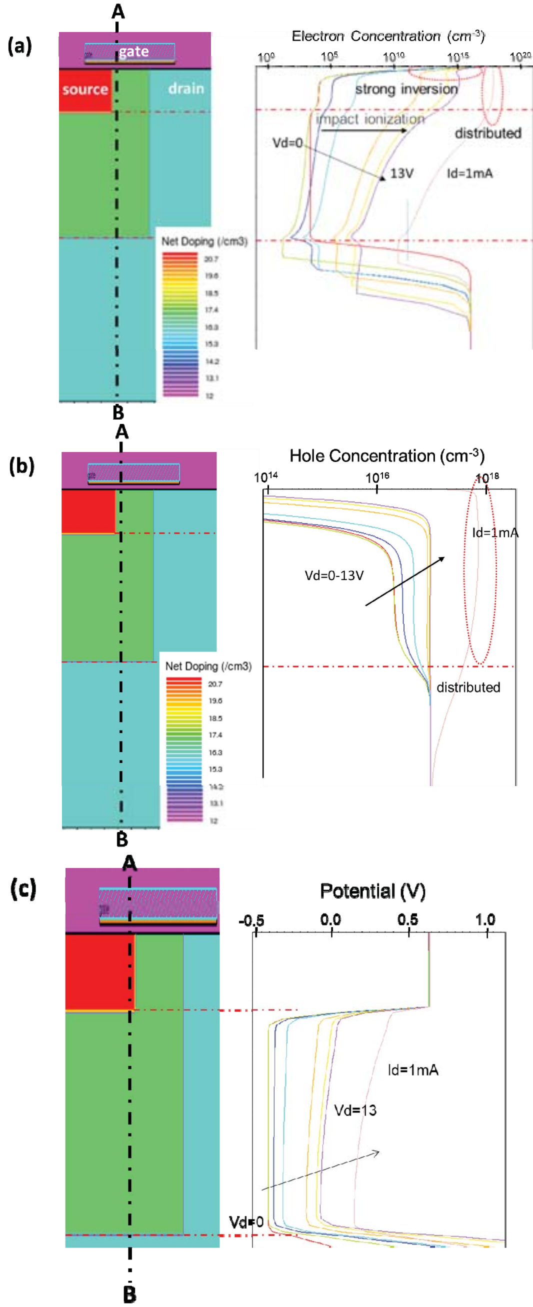

Fig. 4. Electron concentration (a) and hole concentration (b) near the source junction along line A-B for selected bias points in the snapback plot of Fig. 2. Potential distribution (c) within the substrate along line A-B. During the drain-voltage sweep leading to the snapback, the potential deep in the substrate steadily increases so that the source junction becomes forward biased.

respectively. **SVGS**, **SVGSL**, **SVGSW**, **SVGSWP**, **SVBS**, **SVBSL** and **SVBSLP** are model parameters. C_{ox} and N_{sub} are oxide capacitance per unit area and doping concentration to substrate, respectively. q, β, ϵ_{Si} are elementary charge, thermal inverse voltage, and permittivity of silicon, respectively. V_{fb} is flatband voltage.

B. Potential increase

The substrate current is not sufficient to fully account for the increase of either drain or source current. The observed current increase is due to the potential increase within the substrate [6] due to the accumulated holes, which is equivalent to a positive biasing in the substrate (see Fig. 4c).

To account for this potential increase, an internal node b' was introduced and substrate resistance was connected between this internal node b' and the bulk terminal node to describe the magnitude of the hole accumulation in the substrate. As impact-ionization-generated hole current flows through this resistor, the voltage drop across the internal node b' and the bulk node is induced. Thus, the source-body junction becomes forward biased.

C. Bipolar effects

The source-injected current I_{bs} is modeled with source junction diode model, as is provided in the HiSIM_HV code. In its simplified form, the source-junction diode current is expressed as J_s (exp(beta*$V_{b's'}$) – 1), where the equation's reference voltage is the difference between source and internal substrate node (b'). The prefactor J_s can be extracted through fitting to the conventional current-voltage measurement results for the junction leakage. More specifically in detail, the gate-side periphery component of the source-body junction diode is the dominating part where electrons are injected at the source-body junction. Using the voltage difference (V_{bsi}) between the nodes s' and b', the diode current for the gate-side periphery component is expressed as [5]

$$I_{bs,\,swg} = i_{sbs,swg} \cdot \left[\exp\left(\frac{\beta V_{bsi}}{\mathbf{NJS}} \right) - 1 \right] + \\ i_{sbs2,swg} \cdot \mathbf{CIBS} \cdot \exp\left(\frac{T}{\mathbf{TNOM}} - 1 \right) \cdot \mathbf{CTEMPS} \cdot \left(\exp\left(- \frac{\beta V_{bsi} \cdot \mathbf{CVBS}}{\mathbf{NJS}} \right) - 1 \right) + \\ \mathbf{CISBKS} \cdot \left(\exp\left(- \frac{\beta V_{bsi} \cdot \mathbf{CVBS}}{\mathbf{NJS}} \right) - 1 \right) + \mathbf{DIVXS} \cdot i_{sbs2,swg} \cdot V_{bsi} \tag{10}$$

where **NJS**, **CIBS**, **CTEMPS**, **CVBS**, **CISBKS**, and **DIVXS** are model parameters for the junction diode model implemented in HiSIM_HV. In (9), the prefactors $i_{sbs,swg}$ and $i_{sbs2,swg}$ are expressed as [5]

$$i_{sbs,swg} = W_{eff} \cdot \mathbf{JS0SWGS} \cdot \exp\left(\frac{1}{\mathbf{NJSWGS}} \cdot \left(\frac{qE_g(T = \mathbf{TNOM})}{k\mathbf{TNOM}} - \frac{qE_g(T)}{kT} + \mathbf{XTIS} \cdot \ln \frac{T}{\mathbf{TNOM}} \right) \right) \tag{11}$$

$$i_{sbs2,swg} = W_{eff} \cdot \mathbf{JS0SWGS} \cdot \exp\left(\frac{1}{\mathbf{NJSWGS}} \cdot \left(\frac{qE_g(T = \mathbf{TNOM})}{k\mathbf{TNOM}} - \frac{qE_g(T)}{kT} + \mathbf{XTIS2} \cdot \ln \frac{T}{\mathbf{TNOM}} \right) \right) \tag{12}$$

where **JS0SWGS**, **NJSWGS**, **XTIS**, **XTIS2** are model parameters. W_{eff} is the effective gate width and q/kT is the inverse thermal voltage at temperature T. $E_g(T)$ is the energy gap as a function of temperature T.

D. Implementation to HiSIM_HV

The three developed model parts are implemented into HiSIM_HV, a surface-potential-based compact model for high voltage MOSFETs, as depicted in Fig. 5. Newly defined was an internal node b', and the rest of the nodes are already provided. Between the internal bulk b' and the internal source node s', the gate-side periphery junction diode was considered. The diode current I_{bs} is expressed in (9), (10), and (11). Between the internal bulk node b' and the internal drain node d', impact-ionization generated current originating from I_{bs} was considered in addition to such current originating from the intrinsic MOSFET drain current I_{ds}. The substrate resistance introduced between b' and the bulk node determines the snapback condition. Based on these ensemble contributions defined on each branch terminating at b', the voltage at b' is solved by circuit simulator consistently. In this sense, it can be said that the node voltage at b' determines an electrical balance among those contributions.

IV. Evaluation of Developed Model

Finally, in Fig. 6, model calculation results are compared with measurements. Simulations and measurements were current-driven. Shown are drain current vs drain voltage characteristics for multiple gate voltages, for three power MOSFETs with different gate lengths. These devices clearly exhibit a snapback. The snapback bias varies with the gate-bias. The developed model captures those snapback features reasonably well.

V. Conclusion

The presented compact modeling approach for the snapback phenomenon by introducing an internal node has been proved to capture three sequentially induced mechanisms in a consistent way. Thus it is possible to reproduce the snapback features with minimal additions to an existing compact model for high-voltage MOSFETs.

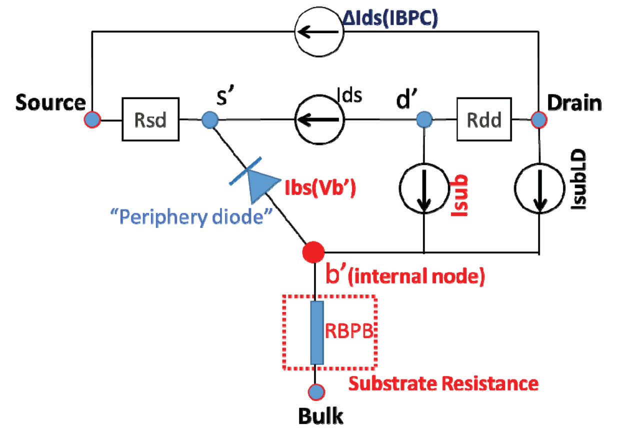

Fig. 5. A snapback model implemented into an exisiting compact model for high-voltage MOSFETs (HiSIM_HV). Impact ionization (Isub), internal node (b'), substrate resistance (RBPB), and source-injected current (Ibs as function of Vb's') are major modeling parts of the snapback model. "Rdd" and "Rsd" denote drift resistance on drain side and source side, respectively.

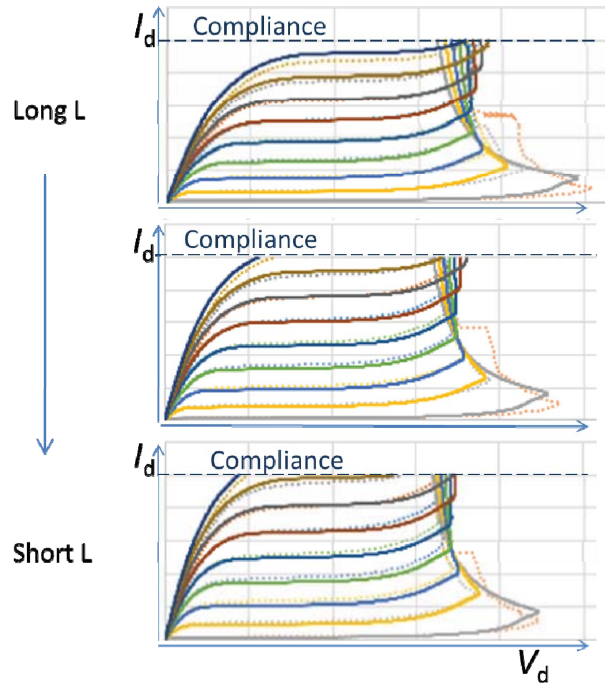

Fig. 6. Comparison to measurement data. Solid lines show simulation using HiSIM_HV 2.4.0 and dotted lines show measurements. Drain currents vs drain voltage are depicted for multiple V_{gs}. At a certain bias point, I_d-V_d curves snap back. HiSIM_HV successfully reproduces the measured snapback.

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