Simulations of Self-Heating Effects in SiGe pFinFETs Based on Self-Consistent Solution of Carrier/Phonon BTE Coupled System

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***Abstract*—Using the in-house simulation tool, self-heating (SH) effects on transport of holes in SiGe pFinFETs are simulated. The coupled system of Boltzmann Transport Equation (BTE) for holes and phonons is solved self-consistently. For transport of holes, the multi subband BTE (MSBTE) is solved for 1D hole gas system, where the subband structure is computed from the 2D $\vec{k} \cdot \vec{p}$ Schrödinger Equation (SE)/3D Poisson equation (PE) solution. For transport of phonons, the BTE for 4 phonon modes (LA, TA, LO, TO) in 3D $\vec{k}$–space is solved based on first order spherical harmonic expansion (SHE) method. This study demonstrates the strong dependence of pMOS SH on Ge content. As Ge mole fraction increases above 0.2, alloy scattering hampers the thermal conductivity by more than one order of magnitude. Combined with boundary scattering and smaller band-gap of SiGe, this effect may pose some alarms on next generation pMOS devices.**

I. Introduction

Recently, some improvements on the fabrication technology [1] make strained SiGe become a promising candidate among novel channel materials for boosting the performance of the existing strained Si pFinFET architecture. However, self heating (SH) effects in such SiGe devices are significantly pronounced due to low thermal conductivity of SiGe alloy [2]. The consequent SH effects may seriously hamper the performance and reliability of device [2]. SH studies have already been reported for Si nMOS devices [3], [4]. In this work, the heat-transport of pMOS devices is evaluated for advanced node options using the coupled BTE solver. For transport of holes, the multi subband BTE (MSBTE) is solved for 1D hole gas system, where the subband structure is computed from the 2D $\vec{k} \cdot \vec{p}$ Schrödinger Equation (SE)/3D Poisson equation (PE) solution [5], [6]. For heat-transport, the BTE for 4 phonon modes (LA, TA, LO, TO) in 3D $\vec{k}$–space is solved based on first order spherical harmonic expansion (SHE) method. The hole MSBTE (hMSBTE) coupled with phonon SHEBTE (pSHEBTE) via the temperatures and the generation rate of phonons.

II. Method

Fig. 1 shows the flow chart of simulation method. The coupled system of hMSBTE/pSHEBTE is solved self-consistently using a Gummel liked iteration approach. hMSBTE solver

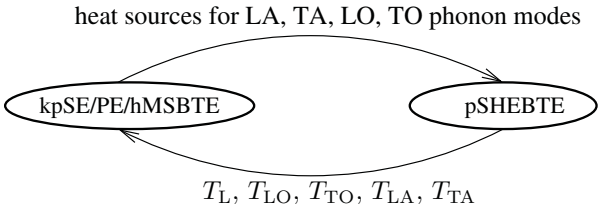

Fig. 1. Flow chart of simulation method, solving self-consistently the coupled system of kpSE/PE/hMSBTE/pSHEBTE.

computes the hole distribution function for multi subbands in a deterministic manner [5], where the valence subbands in the 2D confinement fin cross-section is obtained from the self-consistent solution of 6-band $\vec{k} \cdot \vec{p}$ SE and PE. In order to match the performance of practical devices, all relevant scattering mechanisms are included. The resulting hole distribution balances the scattering by optical and acoustic phonon, ionized impurities, alloy disorder and surface roughness. The impact of surface phonon is captured via local enhancement of deformation potential near oxide interface [7]. The scattering parameters are calibrated against the experimental data of long channel low-field mobility of Si, SiGe, and Ge pMOS structures [8]–[11]. Fig. 2 shows hardware mobility and MSBTE results. The calibration of scattering parameters has successfully reproduced the measurement data. The strain value is consistent with the lattice mismatching between channel and the relaxed buffer layer [1]. The simulation results predict 25% mobility boost for $x_{\rm Ge} = 0.4$. All low-field mobilities are calculated by linearization of hMSBTE.

The equilibrium phonon distribution is used for phonon scattering rate calculation, where the temperature for each phonon branch has been calculated individually based on the pSHEBTE solution at the previous Gummel iteration step.

Once the hMSBTE has been solved, the energy dissipation by optical phonon, $W(x)$, is locally evaluated from the corresponding scattering rates, for a position x along the transport direction. Then, hole density $p(x, \vec{r})$, is used as the weighting function to distribute $W(x)$ within the 2D

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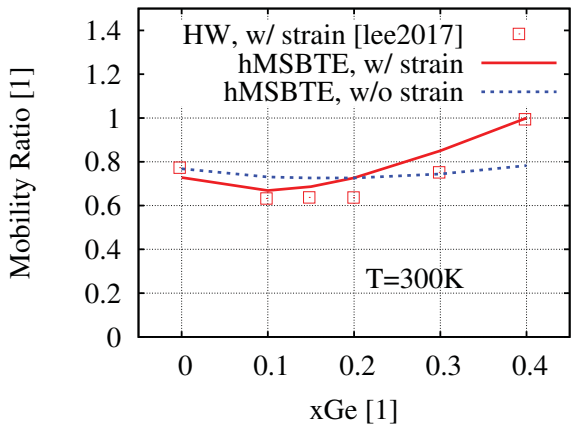

Fig. 2. Low-field effective hole mobility in strained vs unstrained SiGe DG pMOS structures based on hMSBTE. HW data are from [1]. (110) surface orientation/[110] channel direction is considered. Strain is consistent with the lattice mismatching between SiGe in the channel and the relaxed $Si_{0.8}Ge_{0.2}$ buffer layer of FinFET structures [1].

confinement coordinate ($\vec{r}$):

$$W_{3D}(x,\vec{r}) = \frac{1}{\int p(x,\vec{r})d^2\vec{r}} W(x)p(x,\vec{r}). \quad (1)$$

Finally, W_{3D} is equally distributed to pSHEBTE for LO, TO modes, while the pSHEBTE for LA, TA modes are kept isolated from W_{3D}. The Si and Ge phonon band structures are calculated using VFF method [12], then post-processed for the first order SHE framework [13], [14]. The virtual crystal approximation is used for the SiGe phonon band structure calculation. For phonon transport, the relxation time approximation (RTA) is employed [15], where the full scattering integral operator is presented in terms of a total relaxation time (τ). We take into account the scatterings due to phonon-phonon (3 phonon process), phonon impurity, phonon alloy, and phonon boundary roughness. We follow [16], [17] for modeling of τ for individual scattering processes. The scattering parameters are calibrated to reproduce the experimental data of thermal conductivity (κ) of Si, SiGe, Ge bulk system (Fig. 3) as well as thin films (Fig. 4). Compared to the Si case, κ of both SiGe bulk system and SiGe thin films is significantly dropped, due to the effect of phonon alloy scattering [17]. κ shown in Fig. 4 is strongly reduced when the film thickness is scaled down to the typical fin width ranging from 5 to 10 nm. This is mainly due to the effect of phonon boundary scattering [16], [17].

For oxide regions, the Fourier equation for lattice temperature is solved. Assuming carrier thermalization for S(ource) and D(rain) regions, we apply the Dirichlet boundary condition for temperatures at S and D contacts, while we consider a lumped thermal resistance for the G(ate) contact. Once the pSHEBTE has been solved, the temperatures of lattice and each phonon branch are calculated assuming Bose-Einstein distribution form, and fed back to the hMSBTE block for the next iteration step. The Gummel like approach is employed

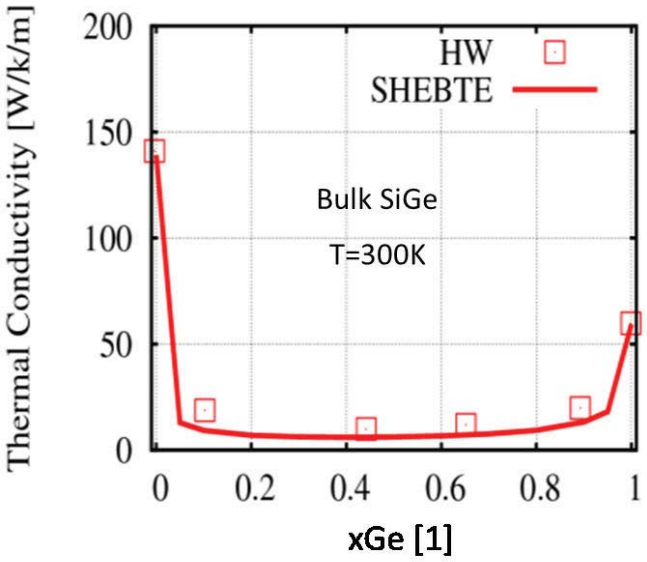

Fig. 3. Thermal conductivity of bulk SiGe vs Ge mole fraction. HW data are from [18].

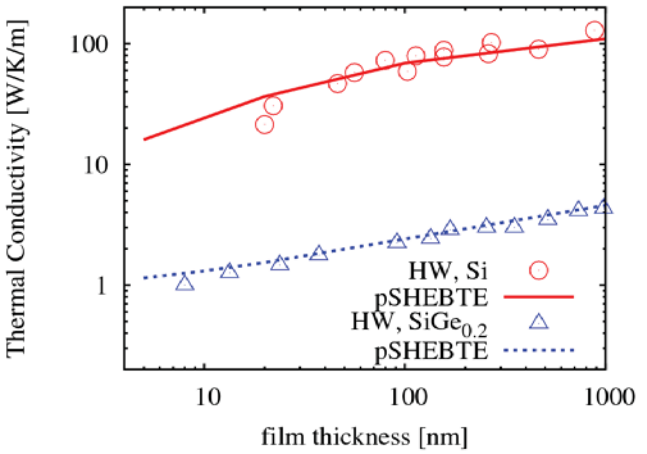

Fig. 4. Thermal conductivity of $SiGe_{0.2}$ thin film vs film thickness. HW data are from [19]–[21].

for correcting temperatures, distributions, and electrostatic potential, by iteration, until the self-consistency is established.

III. Results

Fig. 5 shows the geometry of simulated pFinFETs, where unstrained $Si_{1-\alpha}Ge_\alpha$ ($\alpha = 0, 0.1, 0.2, 0.3$) with a cross-section of 5nm×15nm is considered. The fin sidewall is (110) orientation, and the channel is along [110] direction. T_{ox} and L_g are set as 0.7nm and 20nm, respectively. We extend the length of S and D regions up to 150nm to ensure carrier thermalization [15]. For x from the S or D contacts to 75nm inside the device (Fig. 5 (left)), we keep $\alpha = 0$ and exclude the phonon boundary scattering, in order to thermally represent the high κ epi regions in the real FinFETs. By

overriding $\kappa_{\text{bottom oxide}} = \kappa_{\text{bulk Si}}$ (Fig. 5 (right)), we enable heat dissipation through the bottom oxide, as in the real bulk FinFETs, where heat is transferred from the fin to the substrate underneath. A thermal contact is added to the bottom gate. $V_{DS} = -0.7$ V is applied. V_{GS} is adjusted to fix $I_D = -10\mu$A. Moving from bulk-like S/D region to the confined channel, the average $\kappa(x)$ drops by one order of magnitude (shown in Fig. 6). This drastic drop is mainly due to the phonon boundary scattering in channel area. The other important feature is the adverse impact of phonon alloy scattering. As it is shown in Fig. 6, thermal conductivity of $Si_{0.8}Ge_{0.2}$ channel is almost 10X smaller than Si base-line. κ obtained in Fig. 6 is in good agreement with the results shown in Fig. 4.

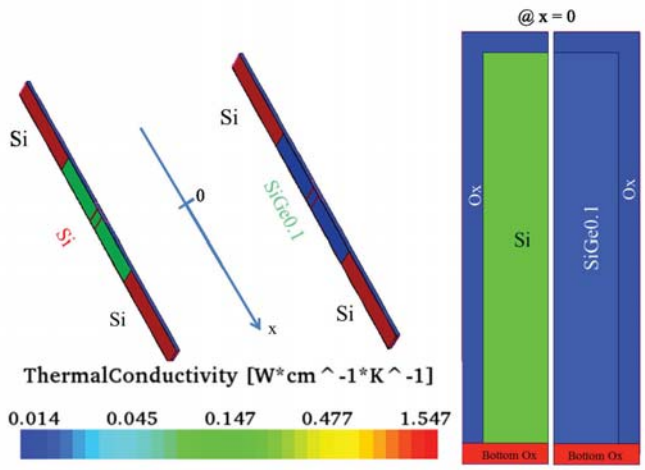

Fig. 5. Spatial thermal conductivity profile in Si and SiGe pFinFETs.

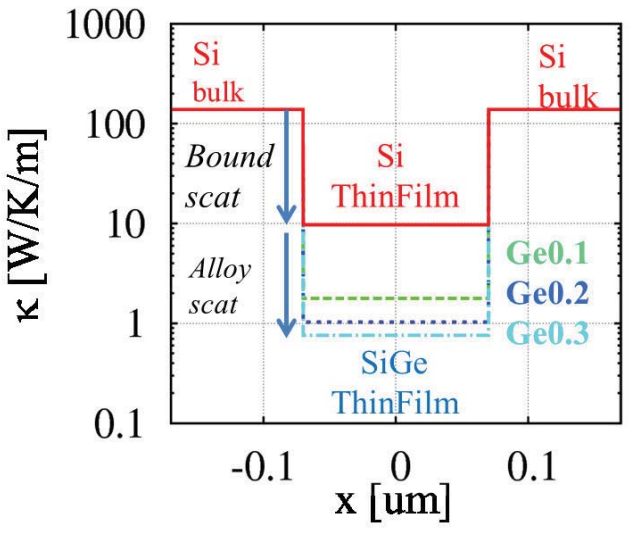

Fig. 6. Thermal conductivity profile vs position x in Si and SiGe pFinFETs.

We have found that the heat profile has small sensitivity to α, as shown in Fig. 7. It also shows a slight reduction of the $W(x)$ peak by increasing α. As it is implied in Fig. 7, full carrier thermalization is realized for $x > 100$nm deep in the drain region. For $0 \leq \alpha \leq 0.3$, the integration $\int_S^D W(x)dx$ is almost unchanged, due to energy conservation and constant I_D, V_D. However, Fig. 8 shows significant increase of peak value of T_L for $\alpha > 0$. This can be explained by sizeable drop of κ in SiGe film (Fig. 4 and 5). When α increases from 0 to 0.1, the peak value of T_L increases around 60K. However, rise in T_L saturates for $\alpha > 0.1$. Fig. 9 shows the average temperatures of lattice and phonon mode for Si and $Si_{0.9}Ge_{0.1}$ devices. The phonon temperature for each mode in Si pFinFET is lower than the one in SiGe device (highest $\Delta T = 60$K for LO mode, and lowest $\Delta T = 30$K for TA mode). Around the position of peak T_L, temperature values are in the following order: $T_{\text{LO}} > T_{\text{TO}} > T_L > T_{\text{LA}} > T_{\text{TA}}$, and this holds for both materials.

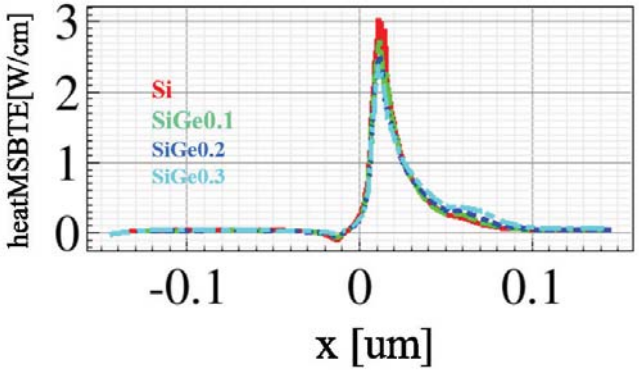

Fig. 7. Total phonon generated heat $W(x)$ in Si and SiGe pFinFETs.

IV. Conclusion

The self-consistent BTE solver for carrier and heat transport has been implemented. The scattering parameters for holes and phonons have been calibrated against measurement data. Using this setup, we have studied the SH effect for pMOS options in advanced nodes. We have found that phonon alloy scattering can trigger serious reduction in thermal conductivity. Considering the inevitable boundary and alloy scattering in fin structure, SiGe channel may face serious heat transport issues.

References

[1] C. H. Lee, S. Mochizuki, R. G. S. III, J. Li, X. Miao, R. Bao, T. Ando, R. Galatage, S. Siddiqui, C. Labelle, A. Knorr, J. H. Stathis, D. Guo, V. Narayanan, B. Haran, and H. Jagannathan, "A Comparative Study of Strain and Ge Content in Si1-xGex Channel using Planar FETs, FinFETs, and Strained Relaxed Buffer Layer FinFETs," in *IEDM Tech. Dig.*, pp. 820–823, 2017.

[2] N. Nenadovic, V. d'Alessandro, L. L. Spina, N. Rinaldi, and L. K. Nanver, "Restabilizing mechanisms after the onset of thermal instability in bipolar transistors," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 643–653, 2006.

[3] O. Badami, F. Driussi, P. Palestri, L. Selmi, and D. Esseni, "Performance comparison for FinFETs, Nanowire and Stacked Nanowires FETs: Focus on the influence of Surface Roughness and Thermal Effects," in *IEDM Tech. Dig.*, pp. 314–317, 2017.

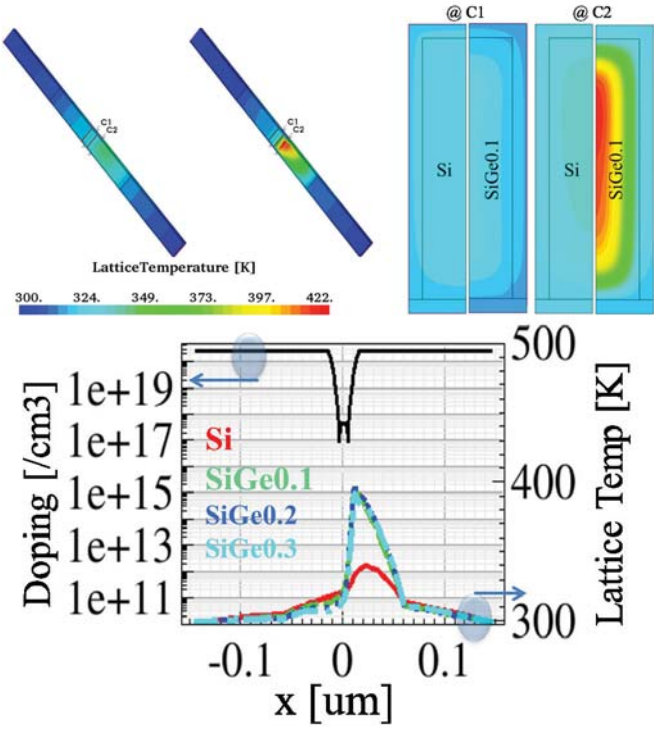

Fig. 8. Spatial lattice temperature T_L and doping profile in Si and SiGe pFinFETs.

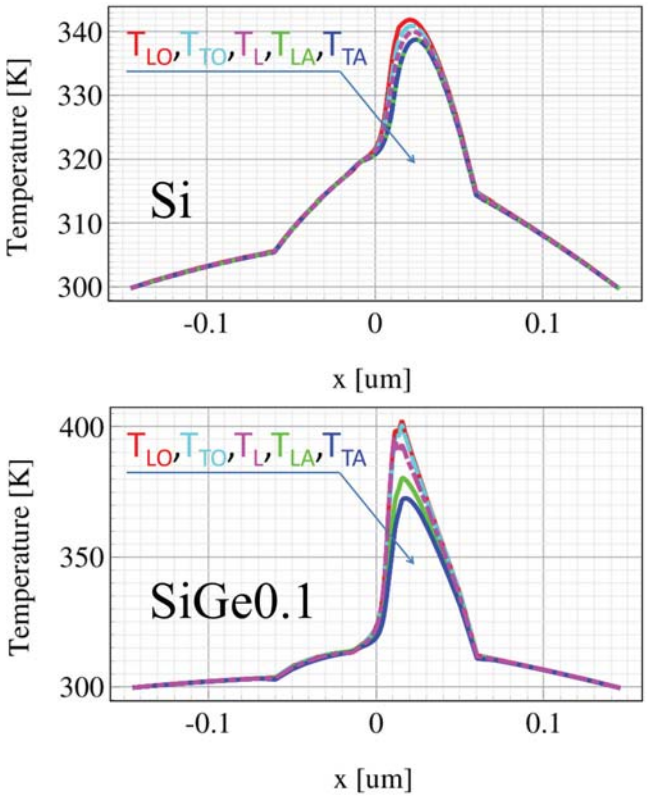

Fig. 9. Average temperatures of phonon and lattice in Si (top) and $Si_{0.9}Ge_{0.1}$ (bottom) pFinFETs.

[4] T. T. T. Nghiem, J. Saint-Martin, and P. Dollfus, "New insights into self-heating in double-gate transistors by solving Boltzmann transport equations," *J. Appl. Phys.*, vol. 116, p. 074514, 2014.

[5] A.-T. Pham, Z. Jiang, S. Jin, J. Wang, W. Choi, M. Pourghaderi, J. Kim, and K.-H. Lee, "On The Efficient Methods To Solve Multi-Subband BTE in 1D Gas Systems: Decoupling Approximations Versus The Accurate Approach," in *Proc. SISPAD*, pp. 189–192, 2016.

[6] S. Jin, A.-T. Pham, W. Choi, Y. Nishizawa, Y. T. Kim, K.-H. Lee, Y. Park, and E. S. Jung, "Performance Evaluation of InGaAs, Si, and Ge nFinFETs based on Coupled 3D Drift-Diffusion/Multisubband Boltzmann Transport Equations Solver," in *IEDM Tech. Dig.*, pp. 184–187, 2014.

[7] T. Ohashi, T. Tanaka, T. Takahasho, S. Oda, and K. Uchida, "Experimental study on deformation potential (Dac) in MOSFETs: Demonstration of increased Dac at MOS interfaces and its impact on electron mobility," *IEEE J. Electron Devices Society*, vol. 4, pp. 278 –285, 2016.

[8] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental Study on Carrier Transport Mechanism in Ultrathin-body SOI n- and p-MOSFETs with SOI Thickness less than 5 nm," *IEDM Tech. Dig.*, pp. 47–50, 2002.

[9] G. Tsutsui and T. Hiramoto, "Mobility and threshold-voltage comaprision between (110)- and (100)- oriented ultrathin-body Silicon MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2582–2588, 2006.

[10] C.-Y. Peng, F. Yuan, C.-Y. Yu, P.-S. Kuo, M. H. Lee, S. Maikap, C.-H. Hsu, and C. W. Liu, "Hole mobility enhancement of $Si_{0.2}Ge_{0.8}$ quantum well channel on Si," *Appl. Phys. Lett.*, vol. 90, p. 012114, 2007.

[11] R. Pillarisetty, B. Chu-Kung, S. Corcoran, G. Dewey, J. Kavalieros, H. Kennel, R. Kotlyar, V. Le, D. Lionberger, M. Metz, N. Mukherjee, J. Nah, W. Rachmady, M. Radosavljevic, U. Shah, S. Taft, H. Then, N. Zelick, and R. Chau, "High Mobility Strained Germanium Quantum Well Field Effect Transistor as the P-Channel Device Option for Low Power (Vcc = 0.5 V) III-V CMOS Architecture," in *IEDM Tech. Dig.*, pp. 150–153, 2010.

[12] A. Paul, M. Luisier, and G. Klimeck, "Modified valence force field approach for phonon dispersion: from zinc-blende bulk to nanowires," *J. Compu. Electr.*, vol. 9, pp. 160–172, 2010.

[13] A. Gnudi, D. Ventura, G. Baccarani, and F. Odeh, "Two-Dimensional MOSFET Simulation by Means of a Multidimensional Spherical Harmonics Expansion of the Boltzmann Transport Equation," *Solid–State Electron.*, vol. 36, pp. 575–581, 1993.

[14] S. Jin, A. Wettstein, W. Choi, F. M. Bufler, and E. Lyumkis, "Gate current calculations using spherical harmonic expansion of Boltzmann equation," in *Proc. SISPAD*, 2009.

[15] J. Rowlette, E. Pop, S. Sinha, M. Panzer, and K. Goodson, "Thermal simulation techniques for nanoscale transistors," in *Proc. ICCAD*, pp. 225–228, 2005.

[16] M. Kazan, G. Guisbiers, S. Pereira, M. R. Correia, P. Masri, A. Bruyant, S. Volz, and P. Royer, "Thermal conductivity of silicon bulk and nanowires: Effects of isotopic composition, phonon confinement, and surface roughness," *J. Appl. Phys.*, vol. 107, p. 083502, 2010.

[17] Z. Wang and N. Mingo, "Diameter dependence of SiGe nanowire thermal conductivity," *Appl. Phys. Lett.*, vol. 97, p. 101903, 2010.

[18] M. C. Steele and F. D. Rosi, "Thermal conductivity and thermoelectric power of Germanium-Silicon alloys," *J. Appl. Phys.*, vol. 29, p. 1517, 1958.

[19] X. Wang and B. Huang, "Computational study of in-plane phonon transport in Si thin films," *Sci. Rep.*, vol. 4, p. 6399, 2014.

[20] R. Cheaito, J. C. Duda, T. E. Beechem, K. Hattar, J. F. Ihlefeld, D. L. Medlin, M. A. Rodriguez, M. J. Campion, E. S. Piekos, and P. E. Hopkins, "Experimental investigation of size effects on the thermal conductivity of Silicon-Germanium alloy thin films," *Phys. Rev. Lett.*, vol. 109, p. 195901, 2012.

[21] Y. K. Koh, *Heat Transport By Phonons In Crystalline Materials and Nanostructures*. University of Illinois at Urbana-Champaign, 2010. Dissertation.