Design Guidelines and Limitations of Multilayer Two-dimensional Vertical Tunneling FETs for Ultra-Low Power Logic Applications

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***Abstract*—New designs for vertical 2D-materials-based TFETs are proposed in this paper adopting asymmetric layer numbers for the top and bottom layer with undoped source/drain using Black Phosphorus as an example. The results show that abrupt turn-on and $I_{on}/I_{off} > 10^5$ can be sustained when the channel length is down to sub-5 nm. The results are benchmarked against other TFETs based on promising 2D materials homo-/hetero-structures, meanwhile, the limitations, as well as guidelines, are presented.**

Keywords—Non-equilibrium Green's Function; DFT; tunnel FETs; black phosphorus; TMDCs; Two-dimensional Materials Heterojunctions

I. Introduction

With the imminent demise of the scaling of silicon based complementary metal-oxide-semiconductor (CMOS) field-effect transistors in sight, it is becoming increasingly important to assess energy efficient alternative electrical switching elements. Steep subthreshold switch devices—with room temperature subthreshold swing (SS) below the 60mV/dec thermal limit– are particularly attractive as they allow voltage scaling and hence enable power reduction and energy efficient computing. Tunneling Field Effect Transistor (TFET) is arguably the most mature and promising low-power steep SS post-CMOS device with numerous reports experimentally demonstrating sub-thermal SS.[1] However, previous TFET efforts with sub-thermal SS and acceptable I_{OFF} were plagued with poor on-current (I_{ON}) and high interfacial trap density (Dit). The emergence of two-dimensional (2D) materials offers promise in resolving these issues, as 2D materials provide layer-number dependent bandgap and ideal trap-free interface. One of the key advantages of Black Phosphorus (BP) is that it exhibits direct bandgap from mono-layer (1L) to bulk— most 2D materials are only direct band gap for monolayer—hence facilitating layer thickness engineering to tune the band offset and

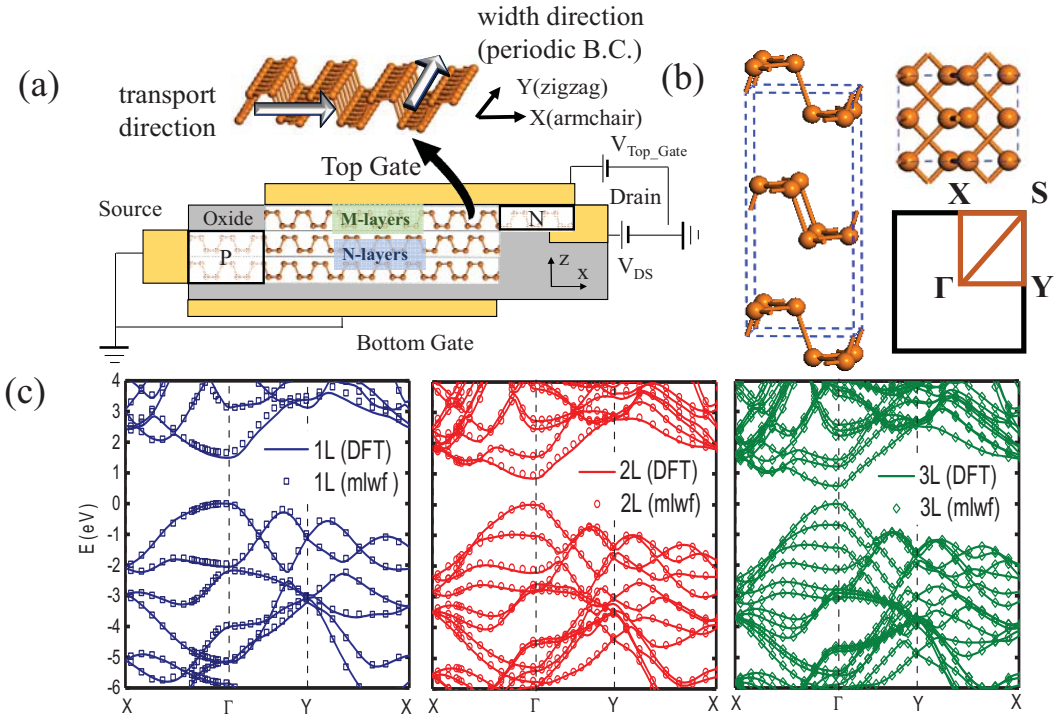

Fig. 1. (a) The schematic of the proposed device structure and the channel alignment. The channel is composed of M layers of BP at the top and N layers at the bottom. Careful selection of the number of M (top) and N (bottom) layers allows the tweaking of band offsets and SS steepness. (b) Side and top view of BP crystal and k-path in the 1st Brillouin zone. (c) BP bandstructure variation from monolayer to tri-layer obtained from DFT and mlwf calculation based on 3L BP.

optimize tunneling FET operation. In this work, we will use ab-initio quantum simulation to examine the promise and limitations of homojunction direct bandgap BP vertical TFET— with stacked channel thickness of N (bottom) plus M (top) layers (Fig.1)—down to 5nm gate length using device engineering schemes—e.g., optimizing top and bottom channel layer thickness, source/drain contact, gate layout and overlap regions—and benchmark against selected promising 2D/2D homojunctions/heterojunctions from literature using our ab-initio simulation scheme.

II. Methods

First, to quickly assess the device performance, a 10-band sp3d5s* 2nd nearest neighbor tight-binding (TB) model is used and ballistic electron transport is simulated by iteratively solving the quantum transmitting boundary method [2] and the 3D Poisson equation until self-consistency is achieved. After the preliminary evaluation, ab-initio quantum simulation framework is adopted utilizing first-principle Density Functional Theory (DFT) to extract material properties and non-equilibrium Green's function (NEGF) for electrical characterization. To achieve that, the electronic structures of monolayer and multi-layer BP are calculated by DFT with HSE06 functional [3]. The Bloch functions provided by DFT are then transformed into TB-like Hamiltonians based on Maximally Localized Wannier Functions (MLWFs) [4] with projections on 4 sp3 hybrid orbitals of Phosphorus. Finally, the acquired Hamiltonian is read in to simulate electron transport [5, 6].

III. Preliminary Results

Fig. 1(a) shows the schematic of our proposed multilayer BP vertical TFET with varying top (M) and bottom (N) layer thickness used to optimize the band offset. We show the top- and side-view of BP crystal in Fig. 1(b). Most of the preliminary transport results demonstrated here are for BP based vertical TFET with N=2 and M=1 layers. Comparisons of the MLWFs bandstructure of 1L (M=1), 2L (N=2) and 3L (overlapped channel) with DFT calculations are shown in Fig. 1(c). The results show good transferability of the parameter set used in this work. The bandgap of monolayer, bi-layer, and tri-layer BP all agree well with previous calculations and experiments. [7] Figure 2 provides a summary of transport results using 10-band sp3d5s* TB. The ON-state band diagram of the device is given in Fig. 2(a). In order to understand the tunneling paths in the device, the spatial current density

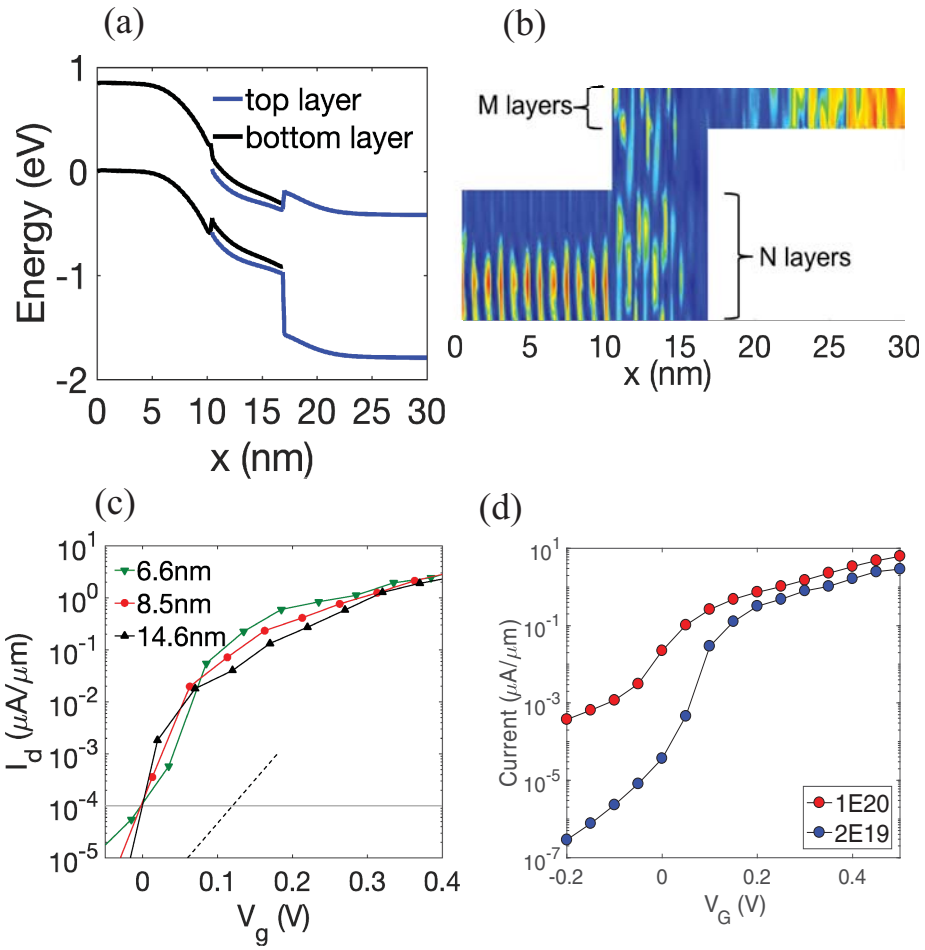

Fig. 2. (a) Conduction and valence band edges along the device transport direction. The overlapped channel region is from x=10 to x=17 nm and is composed of M (top) + N (bottom) layers. (b) Spatial current density distribution in the device. Red: high density, blue: low density. (c) Preliminary I_d-V_g characteristics and (d) Drain doping effect on 7 nm BP vertical TFET.

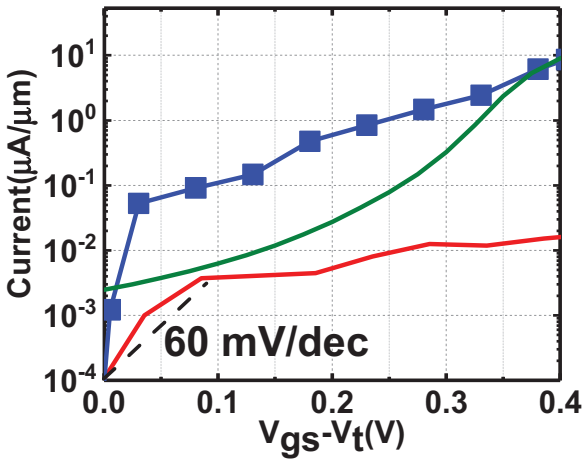

Fig. 3. Ids-Vgs curves of 3.3 nm long 1L/2L BP TFET (N=2, M=1) with S/D doping (red) and undoped D (blue). The green curve is the Ids-Vgs curve of a 5nm 1L BP lateral TFET for reference.

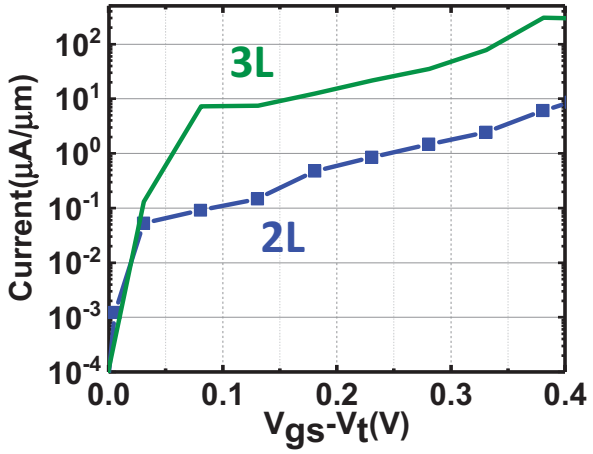

Fig. 4. Ids-Vgs of 1L/2L (N=2, M=1) and 1L/3L (N=3, M=1) BP TFETs.

distribution is plotted in Fig. 2(b). The channel region is defined from x=10 to x=17 nm and is composed of M + N layers. Fig. 2(c) shows the Id-Vg transfer characteristics and Fig. 2(d) shows the transfer curves of 7 nm BP TFET with two different drain doping densities. These results indicate improved device engineering and doping schemes are needed to achieve good scalability beyond 9 nm BP TFET. Further, we propose the idea of utilizing undoped drain and evaluate the improvement by comparing the IV characteristics of the device with undoped drain to that of conventional devices. When channel length is at least 10 nm, our simulation shows that both doped and undoped drain devices exhibit steep SS of less than 10 mV/dec (not presented here). Particularly, we benchmark our device (w/o drain doping) against a separate BP TFET device with conventional doping (opposite type of doping for source and drain) at L=3.3 nm. As the channel length decreases, Fig. 3 shows that the device with conventional S/D doping results in a significant degradation in SS and I_{on}/I_{off} due to the punch-through tunneling from the VB of source to the conduction band (CB) of drain in off state, while our proposed device maintains steep SS of <20 mV/dec at L=3.3 nm. For the purpose of testing design strategy to boost the I_{on}, we increase N to 3 and show the result in Fig. 4 where we see 3L BP TFET has a clearly enhanced I_{on} by more one order of magnitude.

IV. Conclusion

From our DFT-NEGF simulations, we find that undoped drain may be used for device operation and shows superior performance when the channel length is below 10 nm. Moreover, our simulation results show the on-current can be boosted by simply increasing the number of layers for the source without severely affecting the off-current where 3L BP TFET shows clearly improved I_{on} over 2L BP TFET using our design. It is worth noting that changing the channel orientation from zigzag to armchair direction can also effectively enhance the on-current by about 1 order of magnitude. In the presentation,, we aim to extend our preliminary results by assessing the limits of multilayer direct band gap BP vertical homojunction TFET using device engineering designs and comparing it with other promising 2D/2D homojunctions (e.g.,: MoS_2, WTe_2, etc) and heterojunctions (ex: MoS_2/WSe_2) using our multi-physics simulation framework.

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