# Physical Insights on Junction Controllability for Improved Performance of Planar Trigate Tunnel FET as Capacitorless Dynamic Memory

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***Abstract*—The work presents physical insights on the control of energy barriers at junctions of a planar trigate Tunnel FET (TFET) for dynamic memory applications. Results demonstrate the significance of electric field (*EF*) at each junction i.e. Source-Gate1 (S-G1), Drain-Gate2 (D-G2), and that between gates, evaluated through the energy barrier between G1-G2 ($\Delta E_b$) to improve Sense Margin (*SM*), Current Ratio (*CR*), speed (write time) and Retention Time (*RT*). The work highlights the impact of device parameters that aid to improve the performance metrics, and also reduce the associated trade-offs in dynamic memory.**

***Keywords*—Capacitorless, DRAM, Junction, Planar Trigate, TFET**

## I. Introduction

The demand of high speed and denser memory with low power has resulted in the use of energy efficient devices as Capacitorless Dynamic Random Access Memory (1T-DRAM) [1-6]. One such device is Tunnel FET which benefits from low off-current, weak temperature dependence and improved scalability [7,8]. TFET being a $p^+$-*i*-$n^+$ requires architecture modification [3-6] to create the physical well for dynamic memory operation. The present work demonstrates the functionality as DRAM based on the control of *pn* junctions of a planar trigate TFET. The insightful analysis showcases the significance of each junction, regulated through film thickness ($T_{si}$), workfunctions ($\varphi_{m1}$, $\varphi_{m2}$) of Gate-1 (G1) and Gate-2 (G2), and bias applied at gates ($V_{g1}$, $V_{g2}$) and drain ($V_d$). Results show an improvement over previous works [3-5] with a Sense Margin (*SM*) of ~ 200 nA, Retention Time (*RT*) of ~400 ms, Current Ratio (*CR*) of ~ $10^2$ and write time of 10 ns at 85 °C with gate length and storage region of 100 nm each.

## II. Results and Discussion

### A. Simulations and Device Description

TFET was analyzed using ATLAS simulation tool [9] through models well calibrated to the available experimental data [7] (Fig. 1). The non-local model simultaneously with Klaassen model for Band-to-Band Tunneling (BTBT) along with Shockley-Read-Hall recombination with Scharfetter relation [5,9], bandgap narrowing, and Lombardi mobility model along with Fermi statistics and temperature dependent lifetime [9] was included in the analysis. The work utilizes a planar tri-gate TFET (Fig. 2(a)) with the device functionality based on controlling the separate regions of film. The planar tri-gate TFET structure used in the analysis has $p^+$ doped source region, $n^+$ doped drain region with doping concentration of $10^{20}$ cm$^{-3}$ and an intrinsic ($10^{15}$ cm$^{-3}$) channel region between them. The silicon film thickness ($T_{si}$) is 20 nm with 3 nm of $HfO_2$ as the gate dielectric layer ($T_{ox}$).

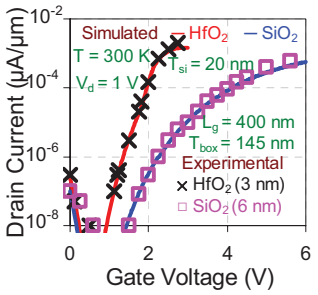


Fig. 1 Drain current ($I_{ds}$) - gate voltage ($V_{gs}$) characteristics of TFET of our simulation with experimental data [7].

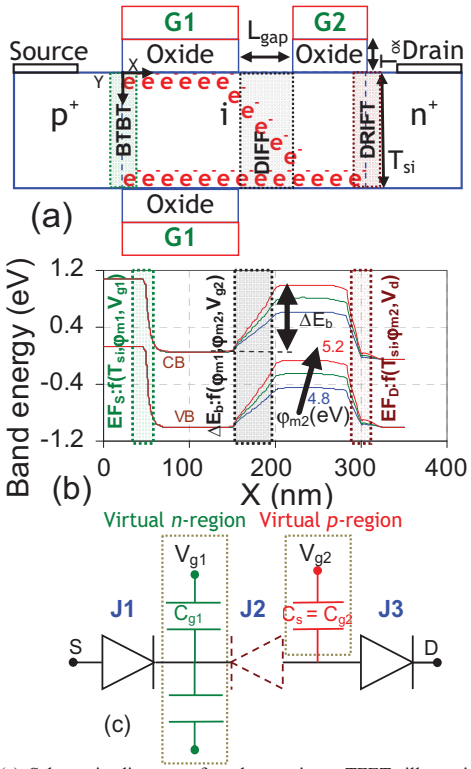


Fig. 2 (a) Schematic diagram of a planar trigate TFET, illustrating Read operation of DRAM with (b) variation in band energy along *X* as a function of $\varphi_{m2}$ and its (c) equivalent schematic representation. (a) shows different mechanisms at each junction (J1, J2, J3) represented in (c) which depends on Electric Field at source ($EF_S$) and Drain ($EF_D$), and energy barrier between G1-G2 ($\Delta E_b$), shown in (b). Parameters: $L_{g1} = L_{g2} = 100$ nm, $T_{si} = 20$ nm, $T_{ox} = 3$ nm ($HfO_2$), $L_{gap} = 50$ nm, S/D doping = $10^{20}$ cm$^{-3}$ $C_{g1}$ and $C_{g2}$ (= $C_s$) are the gate capacitances, DIFF: Diffusion.

The symmetric gates (G1) are electrically connected and are located at a partial region ($L_{g1} = 100$ nm) of the silicon film, aligned to source, while G2 ($L_{g2} = 100$ nm) is positioned adjacent to G1 at front interface with a lateral spacing ($L_{gap} =$

50 nm). The gates (G1 and G2), with appropriate workfunctions, electrically induce a virtual *n*-type and *p*-type regions as demonstrated in Fig. 2(b). This is feasible through use of $n^+$ poly (low $\varphi_{m1}$) dual G1, and $p^+$ poly (high $\varphi_{m2}$) G2. The use of dual gates (G1) enhances *SM* as outlined in [6]. Such devices can be fabricated by adopting the approach demonstrated in [10-12]. Fig. 2(b), thereby forming a $p^+$-$n$-$p$-$n^+$ architecture with an energy barrier ($\Delta E_b$) between the gates that quantifies the depth of potential well.

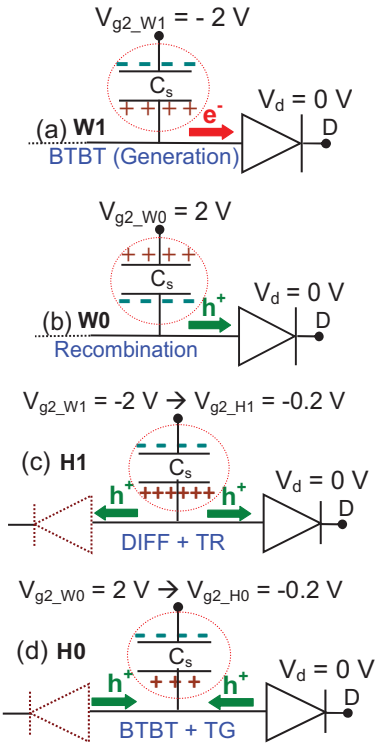


Fig. 3 Schematic illustration of Write (W) and Hold (H) operation in TFET with (a) W1 for state '1', (b) W0 for state '0', and Hold with (c) H1 for state '1', (d) H0 for state '0'. $V_{g1}$, $V_{g2}$, and $V_d$ are the voltages at G1, G2 and drain, respectively. DIFF, TR, BTBT and TG represent diffusion, thermal recombination, band-to-band tunneling, and thermal generation, respectively.

Fig. 2(c) shows the equivalent schematic of the device, where the three junctions: (a) $p^+$-$n$ (J1 at Source-G1 junction), (b) $n$-$p$ (J2 at G1-G2 junction), and $p$-$n^+$ (J3 at G2-Drain junction) are represented through diodes and the gates with their equivalent capacitances. Fig. 2(b) illustrates the dependence of each junction on various parameters. The electric field at J1 and J3 is regulated through film thickness, workfunction of G1 for J1, and that of G2 for J3, and bias applied at G1 for J1 and at drain for J3. The energy barrier at J2 is governed by film thickness, workfunction of G1 and G2, and bias applied at G2. While G1 primarily regulates the read mechanism based on BTBT, G2 controls the hole sustenance in the storage region. The significance of each junction and the associated parameters will be described in the subsequent section.

### *B. Physical Insights into Functionality as DRAM*

Fig. 3 illustrates the schematic representation and bias scheme of TFET device during Write and Hold operation, where capacitance associated with G2 serves as the storage capacitance ($C_s$). Write '1' is defined as the storage of excess holes, performed through BTBT by applying negative bias at G2 that result into electron tunneling towards drain (Fig. 3(a)). Removal of excess hole is classified as Write '0', performed through positive bias at G2 that result into hole recombination at drain (Fig. 3(b)). Sustenance of each State is evaluated through *RT*, determined by Hold operation. The difference between the read currents of the states ($I_1$, $I_0$) is evaluated as *SM*, and the time until maximum *SM* ($\Delta I$) reduces by 50% is defined as *RT*.

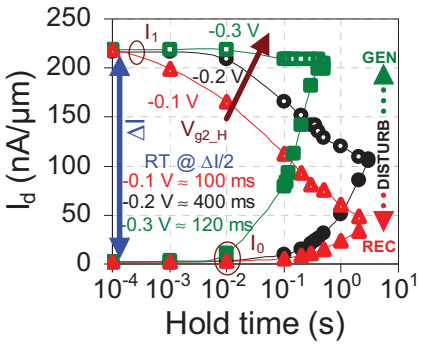


Fig. 4 Variation in read currents ($I_1$ and $I_0$) with hold voltage and time.

State '1' degrades with hole removal from the storage region due to Thermal Recombination (TR) and diffusion of holes (Fig. 3(c)). State '0' is degraded with hole accumulation in the potential well due to Thermal Generation (TG) and BTBT (Fig. 3(d)). This is regulated through the bias applied, as reflected in Fig. 4. While a more negative bias sustain State '1' for longer time and degrades State '0', a more positive bias retains State '0' for longer but recombines holes, decaying State '1' at a faster rate. Fig. 4 shows for a bias of -0.3 V at G2 during Hold, *RT* is disturbed due to hole generation, while that for a bias of -0.1 V due to hole recombination. Thus, maximum *RT* of ~ 400 ms is obtained for a bias of -0.2 V at G2.

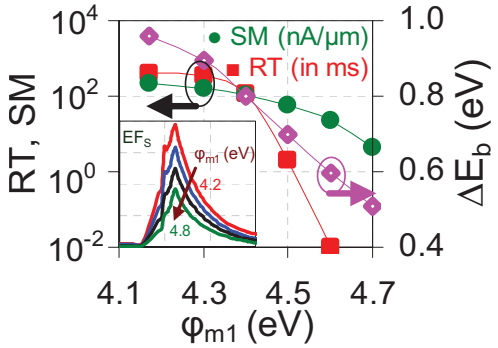


Fig. 5 Dependence of *RT*, *SM*, $\Delta E_b$ and $EF_S$ on workfunction of G1 ($\varphi_{m1}$).

The difference in a state is observed due to presence/absence of excess holes and is reflected in $\Delta E_b$ during Read [3-6]. The presence of excess holes, lowers the potential barrier ($\Delta E_b$) for electrons and thus, show a higher read current for State '1' in comparison to State '0'. Fig. 2(a) illustrates the Read operation governed by three mechanisms, each at different junctions i.e. BTBT at J1, diffusion at J2, followed by drift at J3. BTBT operation is primarily governed by the Electric Field (*EF*) at Source ($EF_S$) which is a function of $T_{si}$, $\varphi_{m1}$ and $V_{g1}$. An increase in $EF_S$ increases BTBT rate [8], and thus, the current for both the states ($I_1$, $I_0$) and hence, *SM* (= $I_1$ - $I_0$) improves. This is evident from Figs. 5 and 6, where an increase in $\varphi_{m1}$ reduces the electron concentration (region changes from *n* to $n^-$). This increases

the depletion width at S-G1 junction, and hence, reduces $EF_S$, shown in Fig. 5. This decreases the *SM*.

The impact of variation in $\Delta E_b$ with $\varphi_{m1}$ is reflected on *RT*, which is explained later. Although, both $I_1$ and $I_0$ increases with $V_{g1}$, significant change in $I_0$ compared to $I_1$ reduces *CR* (= $I_1/I_0$) as shown in Fig. 6, while the *SM* follows the trend as that of variation in $EF_S$. *CR* decreases with increase in $V_{g1}$, but can be tuned through $V_{g2}$ (Fig. 7) that regulates $\Delta E_b$. As shown in Fig. 7, the *CR* is significantly influenced by $V_{g2}$, while *SM* is almost constant for a wider range. On the contrary, the bias variation at drain during Read impacts $I_1$ and $I_0$ by similar ratio, thereby maintaining both *SM* and *CR* for a wider window. Thus, *CR* is prominently governed by $\Delta E_b$, which can also be controlled through $T_{si}$ and $\varphi_{m2}$, while *SM* through $EF_S$ and $\Delta E_b$, with dominance of $EF_S$.

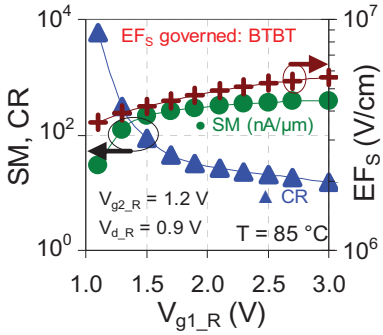


Fig. 6 Variation in *SM*, $EF_S$ and *CR* with bias at G1 during Read (R).

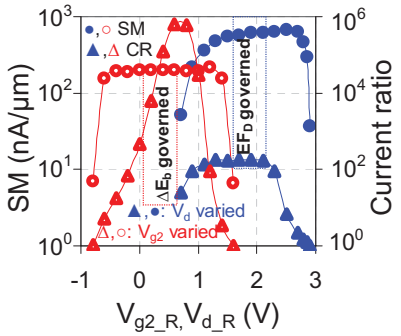


Fig. 7 Variation in *SM* and *CR* with bias at G2 ($V_{g1}$ = 1.5 V and $V_d$ = 0.9 V) and drain ($V_{g1}$ = 1.5 V and $V_{g2}$ = 1.2 V) during Read.

The impact of $\varphi_{m2}$ is shown in Fig. 2(b), where an increase in the value of $\varphi_{m2}$ enhances $\Delta E_b$. A lower $\Delta E_b$ shows higher diffusion [13], and thus, increases read currents. State '0', being depleted of carriers is influenced more by barrier modification as compared to State '1'. A prominent change in $I_0$ with lowering of $\varphi_{m2}$ as compared to $I_1$ results in decrease in *SM* (Fig. 8). A higher $\varphi_{m2}$ induces a deeper physical well (or increases $\Delta E_b$) that sustains holes, and thus, State '1' for longer duration. This retains State '1' for longer and improves *RT*. On the contrary, it also increases the hole concentration (region changes from *p* to $p^+$) that reduces the depletion width at the drain junction and thus, increases $EF_D$. Higher electric field at drain increases BTBT during Hold '0'. This result into higher hole generation in the storage region, and thus, degrades State '0'. Thus, *RT* increases with higher values of $\Delta E_b$ (Fig. 5), but reduces with increase in $EF_D$, and thus, both are crucial for *RT* but one dominates (Fig. 8).

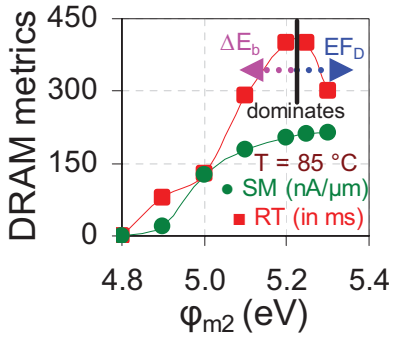


Fig. 8 Dependence of *RT* and *SM* on workfunction of G2 ($\varphi_{m2}$) for $V_{g2}$ = -0.2 V during Hold.

The same is observed in Fig. 9 where a decrease in $T_{si}$ increases both, $\Delta E_b$ and $EF_D$. Decrease in $T_{si}$ results into higher electron concentration [8] under G1 (virtually region changes from *n* to $n^+$) and higher hole concentration under G2 (virtually region changes from *p* to $p^+$). This is being verified through increase in potential in Fig. 10 for region under G1 and a decrease in potential for region under G2. The creation of a $n^+$-$p^+$ region at the channel region reduces the depletion width at S/D junction, and thereby, enhances $EF_S$ and $EF_D$.

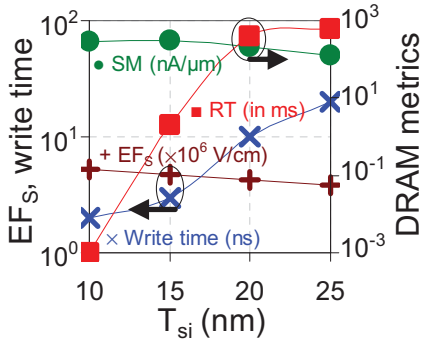


Fig. 9: Dependence of *RT*, *SM*, write time and $EF_S$ on film thickness ($T_{si}$).

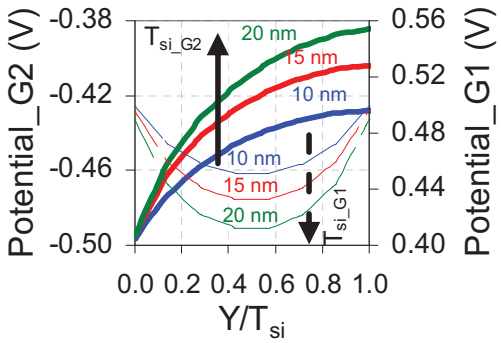


Fig. 10 Variation in potential profile under G1 and G2 along *Y* as a function of $T_{si}$ at zero bias condition.

The increase in $EF_S$ enhances BTBT at S-G1 junction which leads to improved *SM*. The increase in BTBT at G2-D junction due to higher $EF_D$ leads to hole generation during Hold '0', and thus, degrades *RT*. However, BTBT based write mechanism speeds up with higher electric field at drain. It reduces write time (Fig. 9) and thus, improves its applicability for high speed embedded memory. Thus, an increase in $EF_D$ presents a trade-off between *RT* and write time. For stand-alone applications, *RT* is more critical with value > 64 ms, for embedded memory applications it can be

relaxed and the requirement is high speed and low power [6, 14, 15].

Another metric influenced by $EF_D$ is the *SM*, that is governed by $V_d$, and affects the transport mechanism based on drift (Fig. 2(a)). The impact of increase in $EF_D$ through $V_d$ is observable for both, $\Delta E_b$ due to Drain Induced Barrier Lowering (DIBL) as well as in $EF_S$ due to Drain Induced Barrier Thinning (DIBT) [13,16], as shown in Fig. 11. However, an increase in both the read currents with same rate maintains *SM* and *CR* for a wider window (Fig. 7). Thus, the impact of each junction parameter on DRAM metric is summarized in Table I, where the *SM* is predominantly controlled through $EF_S$, *CR* through $\Delta E_b$, write time through $EF_D$ and *RT* through both, $\Delta E_b$ and $EF_D$. The influence of junction parameters is estimated through $T_{si}$, $\varphi_{m1}$, $\varphi_{m2}$, $V_{g1}$, $V_{g2}$ and $V_d$, which reflects dominance of each in various DRAM operations as well as metrics.

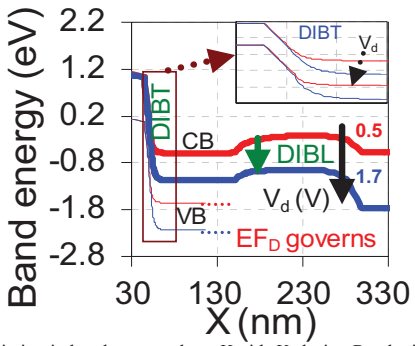


Fig. 11 Variation in band energy along *X* with $V_d$ during Read with $V_{g1}$ = 1.5 V and $V_{g2}$ = 1.2 V.

TABLE I. IMPACT OF VARIOUS PARAMETERS (↑: INCREASES, ↓: DECREASES)

| **Junction parameters** | **Physical mechanism** | **DRAM metrics** (for the range specified in this work) | | **Regulated by** (parameters) |
|---|---|---|---|---|
| $EF_S$ ↑ | BTBT ↑ at S-G1 | *SM* ↑ | *CR* ↓ | $T_{si}$, $\varphi_{m1}$, $V_{g1}$ |
| $\Delta E_b$ ↑ | Recombination ↓ | *RT* ↑ | *CR* ↑ (if $EF_S$ = constant) | $T_{si}$, $\varphi_{m1}$, $\varphi_{m2}$, $V_{g2}$ |
| $EF_D$ ↑ | BTBT ↑ at G2-D | *RT* ↓, Write time ↓ | *CR* and *SM* almost constant | $T_{si}$, $\varphi_{m2}$, $V_d$ |
| | Drift ↑ | $I_1$ and $I_0$ increases | | |

## III. CONCLUSION

Physical insights on the controllability of junctions evaluated through $T_{si}$, $\varphi_{m1}$, $\varphi_{m2}$, $V_{g1}$, $V_{g2}$ and $V_d$ in a planar Trigate TFET highlights the dependence of each on various DRAM metrics. Results showcase optimal values of each parameter is critical to regulate junction fields, and thus, results into enhanced performance with reduced trade-offs.


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