Negative-Capacitance FinFETs: Numerical Simulation, Compact Modeling and Circuit Evaluation

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***Abstract*—A complete simulation framework is presented for Negative Capacitance FinFETs including Numerical Simulation, Compact Modeling, and Circuit Evaluation. A 2D Numerical Simulation for FinFETs coupled with the Landau's Ferroelectric Model captures device characteristics. A new version of the distributed Negative-Capacitance FinFET Compact Model is also presented in this work, where influence of short-channel effects in Ferroelectric voltage amplification are newly incorporated. Finally, a detailed analysis, from an energy perspective, is presented for the gate voltage amplification of Negative Capacitance FinFETs in ring-oscillator circuits.**

***Index Terms*—component, formatting, style, styling, insert**

I. Introduction

Negative capacitance FinFETs (NC-FinFETs) [1] (Fig. 1) are quickly emerging as strong candidates for extremely scaled technologies for digital and analog applications. The recent discovery of ferroelectric (FE) materials using conventional CMOS fabrication technology [2] has led to the first demonstrations of FE based NC-FinFETs [3]. The FE material layer added over the transistor gate insulator helps in several device aspects; it suppresses short-channel effects, increases on-current due to voltage amplification, increases output resistance in short-channel devices, etc. These exciting characteristics have created an urgency for analysis and understanding of device operation and circuit performance, with numerical simulation and compact models as key players.

II. Numerical Simulation

A 2D transistor simulator coupled to 1D Landau FE models has been developed. The transistor structure is solved self-consistently with boundary conditions at source, drain, front gate, and back gate. Values of potential at boundary conditions at each point of the interfacial layer mesh is calculated with the 1D Landau Model (Figs. 2 and 3). As gate length is reduced, NC-FinFETs provide substantial improvements to baseline FinFETs, making them perfect candidates for extremely scaled technologies (Fig. 4). At small gate lengths and using Fin thickness $T_{ch} = 6nm$, and $EOT = 0.6nm$, conventional FinFET characteristics are worsened due short-channel effects. However, using a NC-FinFET structure with a FE layer (hafnium zirconium oxide in this work) of thickness $t_{FE} = 3nm$, remnant polarization $P_R = 15\mu C/cm^2$ and coercive field $E_C = 1.4MV/cm$, short-channel effects are largely suppressed (Fig. 5). For shorter channel lengths, the improvement with respect of base-line FinFET is increased due the increment of S/D to gate fringing capacitance coupling, which further improves the capacitance matching needed for NC-FinFETs [1]. These effects tighten I-V variability distribution as experimentally observed in [3]. The FE voltage (VFE) across the channel (Fig. 6) changes from source to drain, creating different voltage amplifications along the channel length (Fig. 7). These results show that a distributed approach is needed for the simulation of NC-FinFETs.

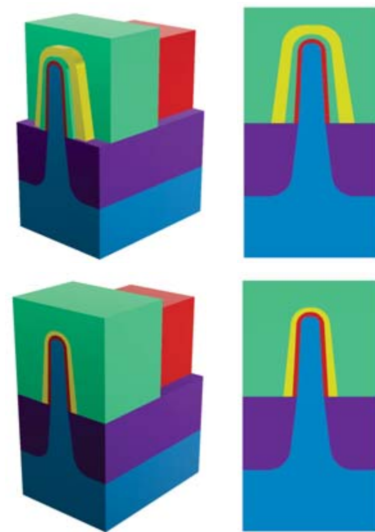

Fig. 1. Schematic of NC-FinFETs: 3D and 2D device cut. Lumped NC-FinFET (top) has a floating gate between insulator and FE. The distributed NC-FET (bottom) does not have a floating gate.

III. Compact Model

For a NC-FinFET without a floating metal (Fig. 1), the distributed charge model should be used [4], where at each point in the channel the FE layer will impact the local channel charge (Fig. 6). The Unified FinFET Compact Model [5]

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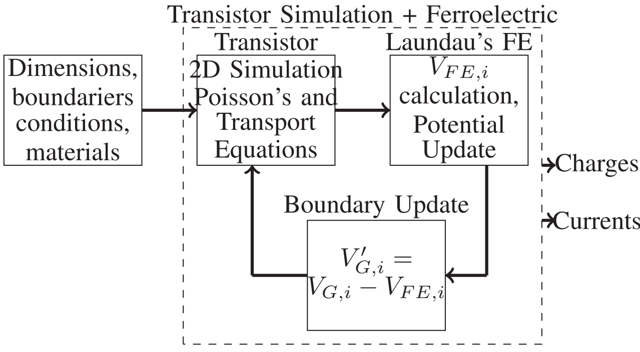

Fig. 2. Self-consistence diagram of 2D transistor simulation with FE. After first simulation is obtained, the displacement values at the interfacial layer boundary are used to obtain VFE at each point of the mesh. With them, the potential boundary conditions at the interfacial layer are updated self-consistently.

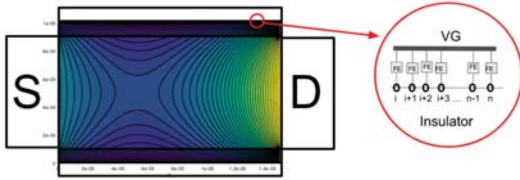

Fig. 3. Diagram of 2D transistor simulation with ferroelectric. Boundary conditions at insulator-ferroelectric interface are updated using Laundau's calculations.

is self-consistently solved with the Landau's FE model at different points of the channel (Fig. 8). The charge obtained is used in the Drain-Current model which is computed using Gauss-Quadrature integration [4]. In the case of non-hysteresis devices, a direct integration is possible and charge is being calculated only at source and drain. As shown by the proposed numerical simulation, short-channel-effects play a key role on the FE FinFET matching. These effects are newly incorporated to the distributed compact model using the extra charge from the internal S/D to gate internal fringing capacitances:

$$Q_{if,S(D)} = C_{if,S(D)}(V_{GS(D)} - V_{bi}) \tag{1}$$

where $C_{if,S(D)}$ is the internal fringing capacitance at source and drain sides, V_{bi} is the built-in voltage at the source and drain junctions. Correct effective voltages are calculated using the right build-in voltage at S/D regions, this gives the right sign of the charge at the channel and has a crucial role on determining, for given terminal voltages, on which part of the S-curve the FE is biased (Fig. 7). The presented compact model has been implemented in commercial circuit simulators, where 14nm ULP FinFETs [6] are used as base-line technology for the energy evaluation of a ring-oscillator (RO) circuit using NC-FinFETs (Fig. 9).

IV. Circuit Evaluation

Ring-Oscillators (ROs) are widely use to evaluate, validate, and monitor performance of a given technology. Indeed, the

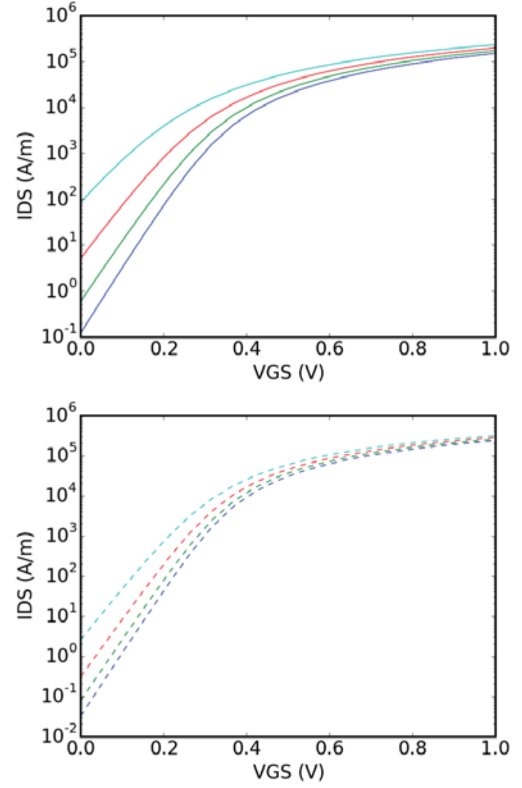

Fig. 4. Drain current characteristics of FinFETs (Top) and NC-FinFETs (bottom) for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $V_{DD} = 1.05V$. In susbthreshold region, potential barrier is increased in NC-FinFETs which decreased the I_{OFF} current w.r.t FinFETs.

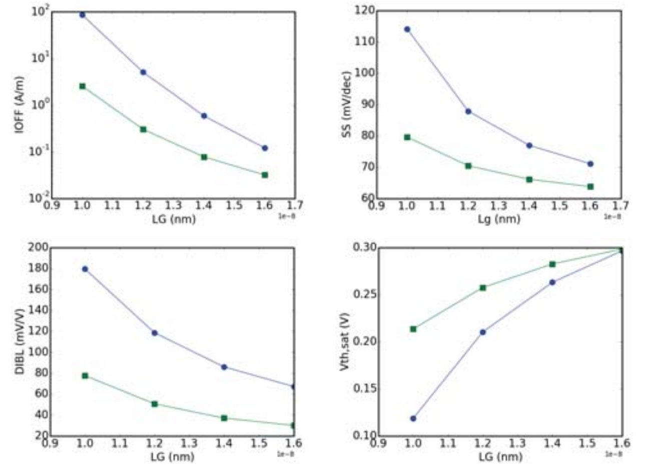

Fig. 5. Electrostatic characteristics, I_{OFF} (top left), Substhreshold Swing (top tight), DIBL (bottom left), and saturation threshold voltage Vth (bottom right), of FinFETs vs. NC-FinFETs for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $V_{DD} = 1.05V$. The I_{OFF} improvement is mainly coming from the reduction of subthreshold swing for the NC-FinFETs. NC-FinFETs present better SS than conventional FinFETs; indeed, SS of NC-FinFET at 6nm node is similar to the SS of regular FinFET at 10nm node.

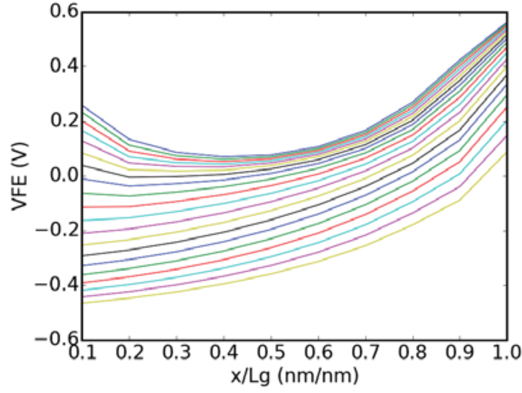

Fig. 6. Ferroelectric voltage (V_{FE}) of a NC-FinFET for different gate voltages ($V_G = 0$ to $1V$) with $L_G = 16nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 1.05V$. Top curve represents lowest V_G value.

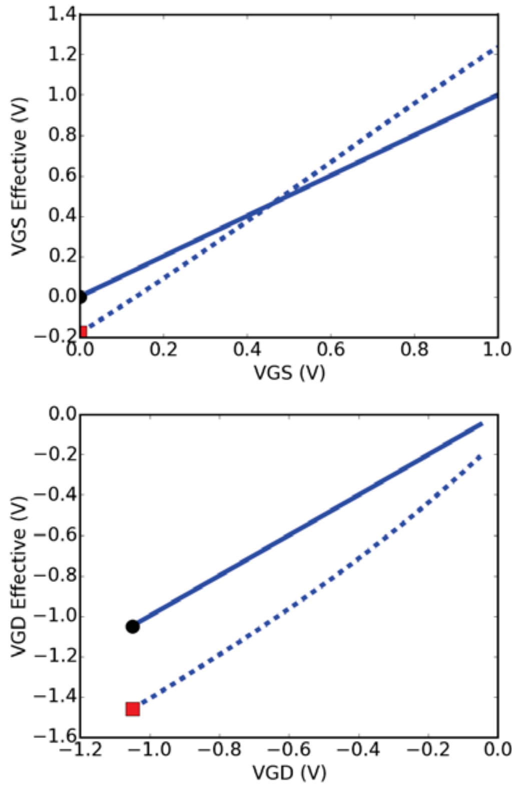

Fig. 7. Effective gate-to-source (top) and gate-to-drain (bottom) voltages of a FinFET and a NC-FinFET (same as Fig. 6). Simulation captures the complex FE polarization at source and drain regions. Inset plots show polarization vs. V_{FE} at source and drain sides. At this drain bias ($V_{DS} = 1V$) the NC-FinFET is electrostatically in the negative-capacitance region; however, source side shows both, positive and negative gate voltage amplification ($V_{FE} < 0$ and > 0), while drain side only a negative gate voltage amplification ($V_{FE} > 0$).

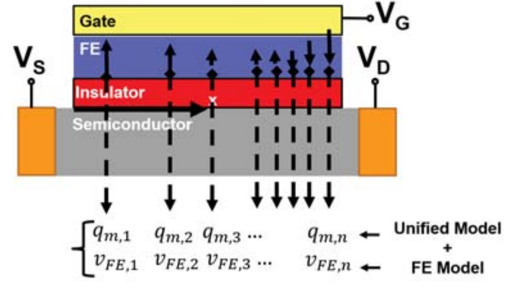

Fig. 8. The distributed compact model [4] utilizing the Unified Compact Model [5] and Landau FE model calculates the charge along the gate length direction. Short-channel-effects are incorporated by adding the charge from source/drain to gate inner fringing field coupling. At low VGS and VGD , charges are negative as in Fig. 7.

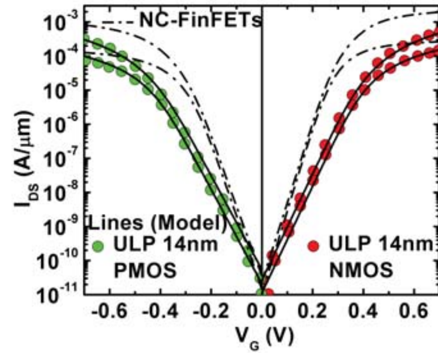

Fig. 9. Drain current versus V_{GS} for nmos and pmos base-line 14nm ULP FinFET [6], and NC-FinFETs with parasitic capacitance. $\alpha_1 = -3 \times 10^9 m/F$, $\alpha_{11} = 6 \times 10^{11} C^2 m^5/F$, and $\alpha_{111} = 0$.

frequency of ROs provides indications of technology speed and can be measured in the early stages of production. A 17-stage RO is utilized in this work (Fig. 10). First, a RO without interconnection load capacitances is considered; i.e., only intrinsic switching characteristics are analysed. Fig. 11

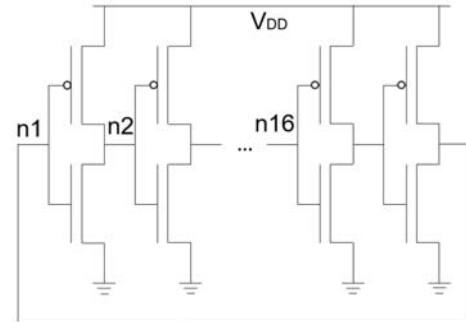

Fig. 10. 17-stage Ring-Oscillator set-up. 11 and 10 Fins are used for pmos a nmos, respectively.

shows a comparison of the voltages at the first node of the RO under study utilizing base-line ULP 14nm FinFETs versus NC-FinFETs. V_{DD} has been set to 0.7V and 0.49V,

respectively. Although both technologies use different V_{DD}, they both match the technology speed, this is the result of the voltage amplification provided from the FE films in NC-FinFETs (Fig. 12) which translates to a larger effective gate to source voltage (V_{GS}) for each transistor (Fig. 13). In order to get the same speed for both ROs, V_{GS} effective for the NC-FinFET RO has to be larger than the base-line one (0.8V vs. 0.7V), because V_{DD} is lower for the NC-RO and also because the total capacitance is increased for the NC-RO. The energy needed for the voltage amplification at each cycle is provided by the FE layers (Fig. 14). In every cycle, pmos and nmos deliver approximately 0.1fJ that are later recovered by the FE layers and re-utilized at later cycles, in a similar manner as explained in section III. This is the key mechanism that allows voltage amplification and energy reduction, making possible the implementation of quasi-adiabatic ROs where not all of the charging/discharging energy is dissipated as heat but part of it is recycled by FE layers. For each inverter, 0.2fJ (19%) per cycle is saved by using NC-FinFETs (Fig. 15), which corresponds to the energy delivered by the FE in the NC-FinFET nmos and pmos together as shown in Fig. 14. This translates to a 19% total energy reduction for NC-FinFETs compared to the base-line FinFET based RO used in this study (Fig. 16).

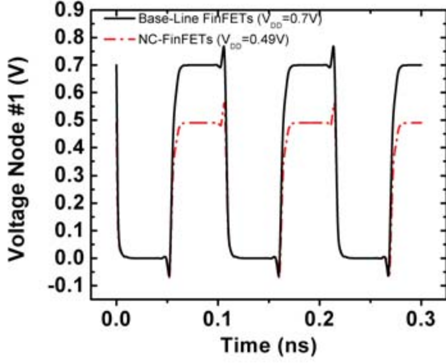

Fig. 11. Voltages at the first node of a 17-stage ring oscillator utilizing base-line ULP 14nm FinFETs versus NC-FinFETs.

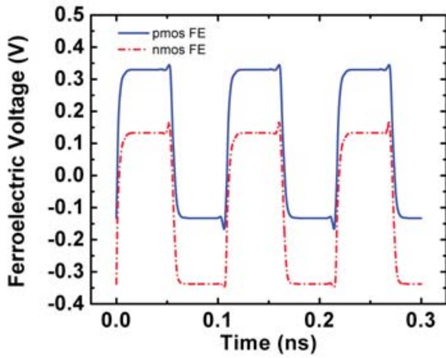

Fig. 12. FE voltage as a function of time for nmos and pmos NC-FinFETs at the first stage of the RO under study.

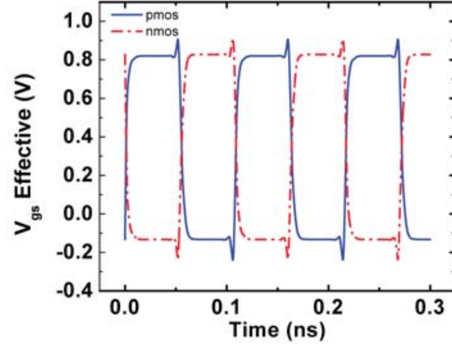

Fig. 13. Effective gate to source voltage for nmos and pmos NC-FinFETs at the first stage of the RO under study.

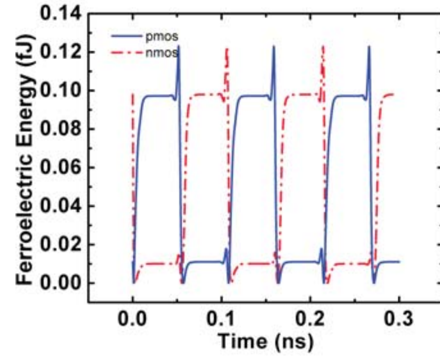

Fig. 14. Energy deliver by each FE layer as a function of time. 0.1fJ is delivered by each nmos and pmos, energy that is later recover by the FE layers.

The second RO configuration in this study is a 17-Stage RO which includes a load capacitance at each connection node between inverters. This load capacitance represent interconnection/wiring capacitances; therefore, it is a more realistic way of characterizing energy behavior for NC-FinFET based circuits. Fig. 17 shows the RO period under different load capacitances. V_{DD} is constant for the base-line FinFETs and tuned for the NC-FinFET ROs; thus, speed is matched at each load capacitance. As load capacitance become more dominant, V_{DD} can be further scaled for NC-FinFET technology. Indeed, energy reduction is increased as load capacitance become more significant (Fig. 18). These results can be understood using a simple equation for the inverter energy per cycle [7]:

$$E_{inv} = E_{dyn} + E_{dp} + E_{stat} \simeq C_L V_{DD}^2 + V_{DD} I_p t_s + V_{DD} I_l t_c \quad (2)$$

where E_{dyn}, E_{dp}, E_{stat} are the dynamic, direct-path, and leakage energy consumptions, respectively. C_L is the total

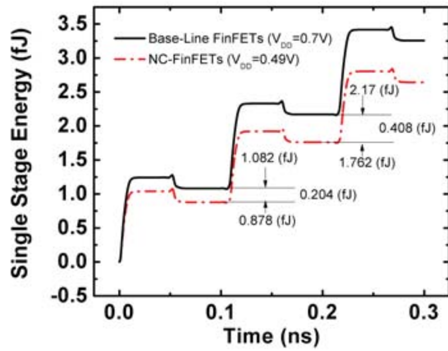

Fig. 15. Energy as a function of time used by a single stage of the RO.

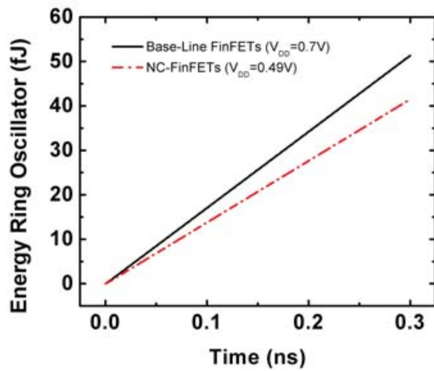

Fig. 16. Total energy as a function of time used by the 17-stage ROs using base-line FinFETs and NC-FinFETs. The later saves 19% of energy at equal RO speed.

loading capacitance for each inverter, I_p the peak current during direct path switching [7], t_s is the time during short circuit, I_l is the leakage current, and t_c is the cycle time. For NC-FinFET inverters, C_L is composed of three components: parasitic/intrinsic FinFET capacitances, interconnection capacitances, and FE capacitance. For the unloaded RO case, C_L is mainly composed by the transistor capacitances and the FE capacitance; therefore, energy reduction is not proportional to V_{DD}^2 due the extra FE capacitance (19% energy reduction). However, as C_L increases, FE capacitance becomes less significant and energy reduction is approximately proportional to V_{DD}^2, as shown in Fig. 18 (58% energy reduction for large capacitance load). Note that if FE does not recover the energy utilized in the quasi-adiabatic process, there is still a significant energy reduction as C_L increases.

V. Conclusion

This work presented insights into the device physics and behavior of FE based NC-FinFETs using numerical simulations, compact models, and circuit evaluation. As NC-FinFET become the preferred candidate for extremely scaled technologies, further device-system optimization can be obtained with the proposed simulation framework.

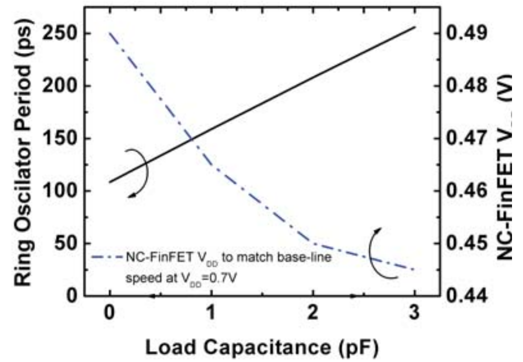

Fig. 17. Ring oscillator period (left axis) and V_{DD} (right axis) versus load capacitance per node for base-line and NC-FinFETs.

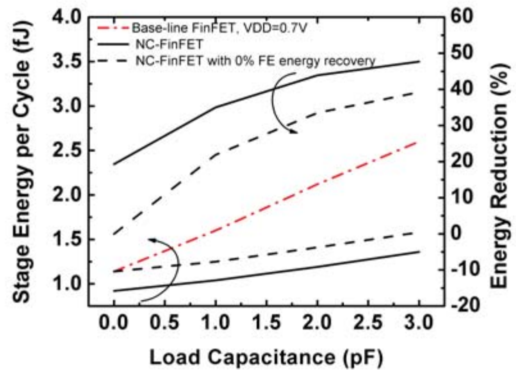

Fig. 18. Stage energy per cycle (left axis) and energy reduction (right axis) versus load capacitance per node for base-line and NC-FinFETs.

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