Modelling on Aging Induced Time Dependent Variability of Z2FET for Memory Applications

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Introduction

Z2FET is a promising integrated DRAM device to replace the traditional 1 transistor 1 capacitor DRAM [1-4]. Memory products always require minimum cell size, high density and large volume memory arrays in the limited chip real estate. However, the downscaling of Z2FET dimensions leads to severe variability issues. A novel simulation methodology has been already proposed [5] to investigate the initial Z2FET Statistical Variability (SV), but the aging induced Time Dependent Variability (TDV) has never been considered.

In this work, for the first time, the impact of the aging induced time dependent variability on the retention time of the Z2FET w/o statistical variability has been systematically studied. It is shown that the aging induced degradation of the device performance follows a Gaussian distribution after a certain stress time. After taking into account the initial SV, the aging reduces the average retention time with an increase of the deviation on a logarithmic scale. Among three corners, the best corner has the least degradation and variability, whereas the nominal devices suffer the most. Retention time before and after aging under different corners can be obtained based on the methodology and the model developed in this work. All these data can be propagated into the corresponding Spice models, and the impact of aging on the yield of Z2FET based memory matrix can be investigated through statistical circuit simulation.

Retention Time Variability

Z2FET has a novel device structure, with a p-i-n channel on SOI substrate (Fig. 1). The front gate (FG), which partially covers the channel, controls both electron and hole potential barriers together with the back gate (BG) [1]. For the memory application, the complementary potentials prevent/allow (i.e. 0/1 state) carriers flowing between the anode and the cathode, depending on the number of electrons stored under the FG.

Data retention time determines the refresh frequency, and is one of the most important memory merits. The extraction of retention time considers the following procedure [1]. First, ensure data '0' is stored by programming '0'. Second, bias to hold condition and monitor the potential (ψ) at point 'P' (Fig. 1). Finally, the time when the potential drops to a certain level is defined as the retention time (Fig. 2a & b), because the lower potential indicates the collapse of the complementary barriers. There are two variation sources contributing to the retention variation: one is from local statistical variability [6] (Fig. 2a), and the other one is from aging induced time dependent variation [7] (Fig. 2b).

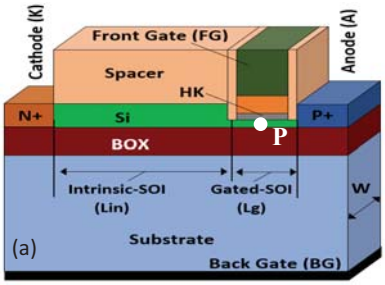

Fig. 1 3D Z2FET structure. Lg, Lin and W are 30nm, 100nm and 30nm respectively. Under ON mode, current flows from p-typed anode, through intrinsic Si, reaching n-type cathode.

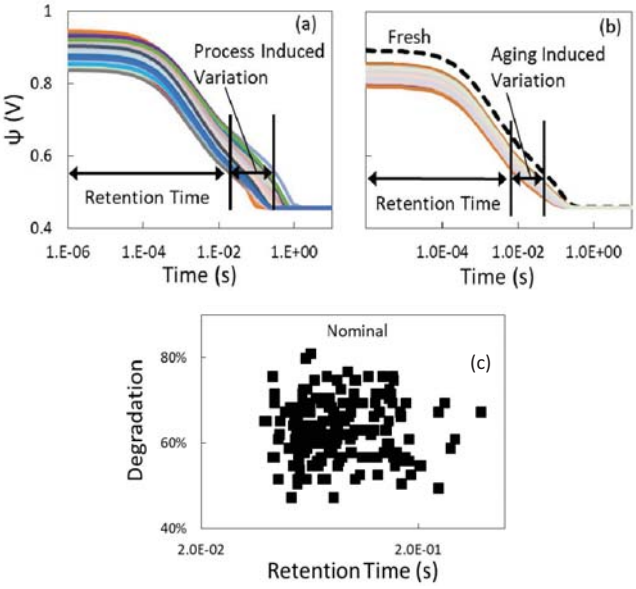

Fig. 2 Potential evolution after program '0' at point 'P' in Fig. 1. Lowered potential level leads to the barriers collapse and subsequent loss of data '0' (definition of Retention time [1]). There are two variation sources of retention time: (a) Initial statistical process induced retention variation and (b) aging induced variation due to stochastic trapping. There is no correlation between them in (c).

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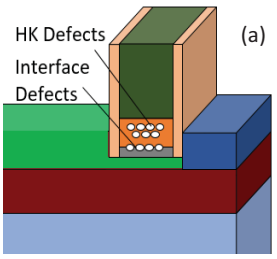
The statistical variability is mainly determined by Random Discrete Dopant (RDD), Line Edge Roughness (LER), Metal Gate Granularity (MGG), and Body-Si Roughness (BSR). The details and simulation methodology has been provided in [5] and will not be discussed here. Since there is no correlation between initial SV induced retention time variations and aging induced retention time degradation (Fig. 2c), it is of special interest to investigate and model the aging impact on Z2FET data retention.

Reliability Analysis and Modelling

As Z2FET is a device with very complicated structure (Fig. 1), there are neither experiments nor modelling studies yet of its reliability issues. The Z2FET fabrication is fully compatible with STMicroelectronics 28 nm high-k (HK) metal-gate (MG) FDSOI technology [3-4]. Degradation could happen on both FG and BG oxides. However, the BG oxide (BOX) is 25 nm thick and has large reliability margins [8] at typical operating voltage. Therefore, the performance degradation should mainly depend on the quality of the front gate HK dielectrics. Meanwhile during hold and read operation, the FG is always positively biased, placing it under Positive Bias Temperature Instability (PBTI) condition where accumulated electrons bombard the FG interface and generate defects. According to [9], unimodal defect-centric degradation approach is not applicable any more on HK/MG technology. Accordingly, the bimodal defect-centric approach must be used. Z2FET FG has the same dielectric stack as the devices in [9], which allows us to take its defects information as reference for studying the Z2FET reliability. The methodology developed in this paper can be described as follows: a) Two types of defects are considered (Fig. 3a), one is in the HK and the other one is at the interface (IT) of HK and the interfacial SiON layer. Each type has its own parameter η and Nt. b) Equivalent kinetics of degradation over 10^9s (9 decades) of aging time are simulated. c) Aging induced threshold voltage shift (ΔVth) is then converted into trap density (N_{HK} and N_{IT}) using the equation $q \bullet \Delta N = C \bullet \Delta Vth$. d) The obtained N_{HK} and N_{IT} are finally implemented for the three different process corners of Z2FET into Sentaurus Device [10] for the performance simulation.

To verify the implemented bimodal defect-centric model, the data from [9] was compared with our simulation results and a good agreement was obtained (Fig. 4a). The distribution and kinetics for 9 decades of degradation time (corresponding to aging time 10, 10^3, 10^5, 10^7, and 10^9 seconds) are obtained for defects at IT (Fig. 4b) and in HK (Fig. 4c), respectively. Fig. 4d shows the overall effects of the defects in both IT and HK regions. The same defect configurations used in Fig. 4d are applied to the front gate region of the Z2FET to enable the investigation of impact of aging on Z2FET retention time.



(b)

η_HK	0.77mV
Nt_HK	3.6
η_IT	3.6mV
Nt_IT	0.12

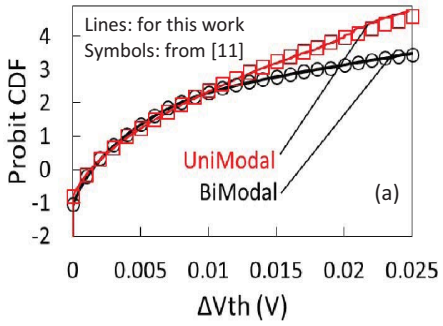
$$F_1(\Delta V_{th},\eta) = 1 - e^{-\frac{\Delta V_{th}}{\eta}} \quad (1) \qquad P_N(n) = \frac{e^{-N}N^n}{n!} \quad (2)$$

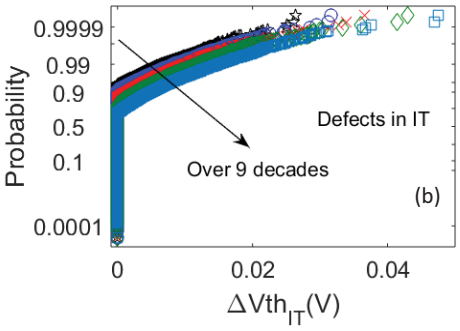
$$F_N(\Delta V_{th},\eta) = \sum_{n=1}^{\infty} P_N(n) \cdot F_n(\Delta V_{th},\eta) \quad (3)$$

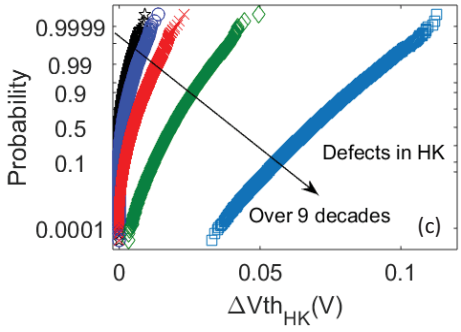
(c)

$$F_{N_1,N_2,\eta_1,\eta_2}(\Delta V_{th}) = \sum_{n_1=1}^{\infty}\sum_{n_2=1}^{\infty} P_{N1}(n_1)\, P_{N2}(n_2)\, F_{n_1,n_2,\eta_1,\eta_2}(\Delta V_{th}) \quad (4)$$

Fig. 3 According to recent published data from IMEC [9], two types of defects exists in high-k dielectric stacks. (a) shows the two types of defects: defects in HK layer and defects in the interface of HK and interfacial layer. (b) shows the parameters used to establish the bimodal for this work, and (c) are the relevant formulas in bimodal defect centric model.







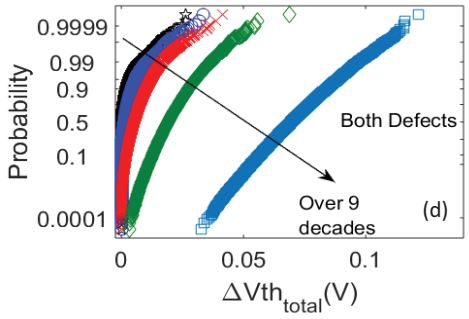
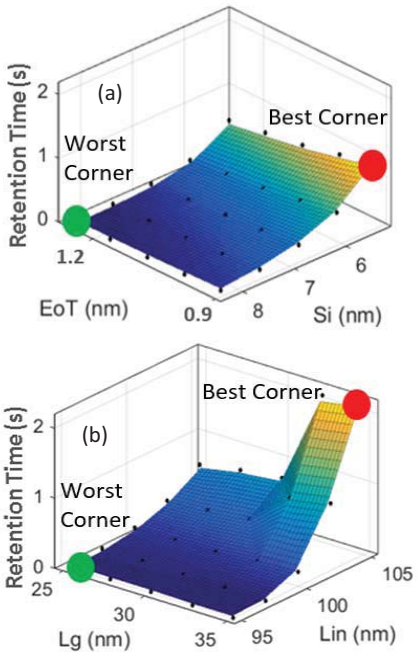


Fig. 4 Based on bimodal defect centric model, degradation over 9 decades is developed. The good agreement in (a) justifies the model we used in this work. (b) and (c) show the distribution induced by these two types of defects after aging for 1, 3, 5, 7, 9 decades respectively, and (d) is the total degradation distribution.

Process Corners

In addition to SV, systematic variation in implant dose and geometrical critical dimensions between die-to-die and wafer-to-wafer cause Global Variation (GV) [11]. GV is generally monitored by process parameter splits within a certain space. For Z2FET, we have found four critical process parameters: the EOT of front gate, the intrinsic region length (Lin), the front gate length (Lg), and the channel Si thickness (Si) contributing to GV. A design of experiment (DoE) including 150 process splits was simulated. Since the above parameters are uncorrelated, only 50 of the DoE results are shown in Fig. 5, which helps us to determine the best corner ('●') and the worst corner ('●') in terms of retention time.



(c)

Parameters	Worst Corner	Nominal	Best Corner
EoT (nm)	1.23	1.07	0.91
Si (nm)	8.28	6.78	5.28
Lg (nm)	25	30	35
Lin (nm)	95	100	105

Fig. 5 Process corners in terms of retention time. Retention time increases with thinner Si and EoT (a), and longer Lin and Lg. (b) '●' and '●' indicate the best and the worst corner respectively. (c) Key process parameters for best/nominal/worst corners.

Time Dependent Variability

The previously obtained defects information can now be implemented into Z2FET simulation (Fig. 6). The simulation result (Fig. 6a) shows that the PBTI induced degradation of retention time follows a Gaussian distribution after a relatively long aging time.

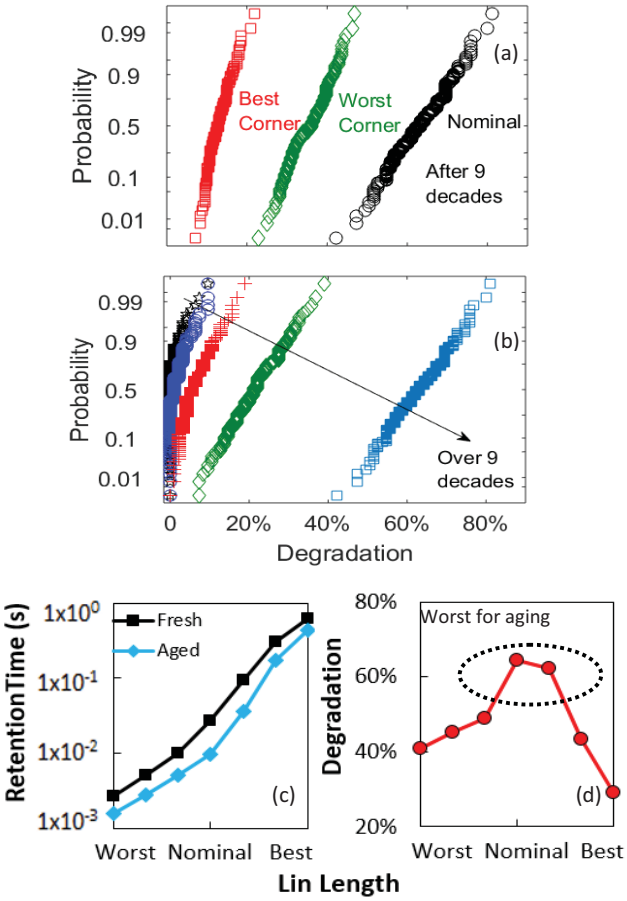


Fig. 6 Aging induced retention time degradation without considering the initial SV. (a) is on nominal devices and (b) considers the worst and best corners for 9th decade degradation. The degradation distribution gradually follows a Gaussian distribution for longer stress time, and nominal devices suffer the most. (c) and (d) simulated the retention time dependency on Lin dimension and confirms that the worst corner for retention time is not the worst corner for aging.

Fig. 6b compares the degradation for the three process corners and it is found that the nominal devices suffer the most and have the largest average degradation and spreading. It is understandable that the worst corner of retention time is not the worst corner of aging (Fig.6 c & d). Many factors affect retention time. Lin is one of the major limiting parameters when scaling down the Z2FET dimension [4]. At the worst corner of retention time, the reduced Lin enhances the leakage current coming from the Cathode and starts dominating the retention time degradation, which renders the aging induced defects to become secondary.

Moreover, we have also simulated the retention time after taking into consideration the initial SV, as shown in Fig. 7. The retention time does not follow a Gaussian distribution any more. With further degradation, the average retention time is reduced but the spreading increases on a logarithm scale. Among the three corners, the nominal devices shift the most due to their higher sensitivity to aging induced defects. All these data can be directly transferred into a circuit simulator to evaluate the production yield of Z2FET based memory matrix.

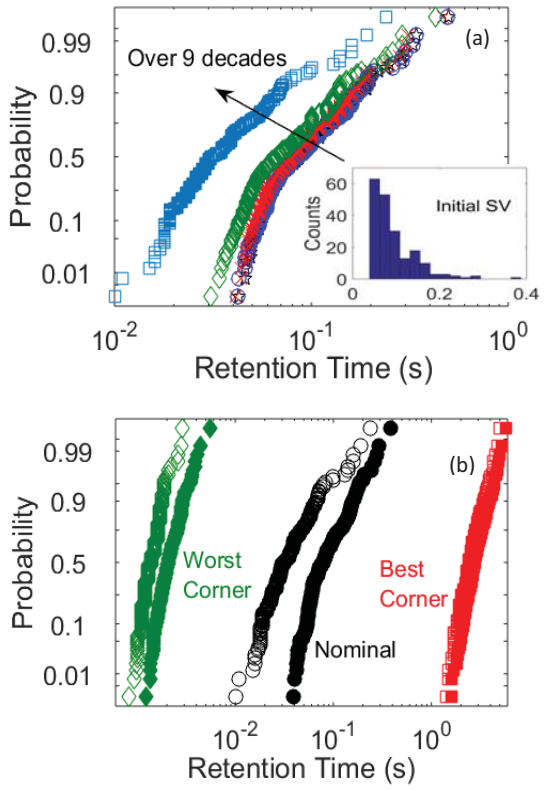


Fig. 7 Retention time distribution considering the initial SV. (a) is on nominal devices and (b) considers the worst and the best corners for 9th decade degradation. Solid symbols are before aging, and hollow symbols are after aging. As expected, nominal devices shift the most towards shorter retention times due to the larger average degradation.

Conclusion

In this work, for the first time, the bimodal defect centric aging model is implemented into Z2FET to investigate its impact on retention time. The aging induced TDV has been investigated systematically based on the model. PBTI on FG is identified as the major reliability issue in Z2FET. Retention time variability w/o initial statistical variability are simulated for three different process corners. The results presented here lay the foundation to evaluating and analysing the aging impact on Z2FET based memory product yield.

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