Evidence of fast and low-voltage A2RAM '1' state programming

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***Abstract*— For the first time, we demonstrate a new concept for programming the '1' state in A2RAM based on the impact ionization in the bridge, which can be assisted by the band-to-band tunneling effect in the top part of the silicon film. This new programming method reduces the programming voltage and writing time, making the A2RAM suitable as 1T-DRAM. Evidenced through TCAD simulation, the feasibility in matrix environment is also demonstrated.**

Keywords*— *A2RAM, TCAD simulation, 1T-DRAM, programming methodology, impact ionization, band-to-band tunneling.

I. Introduction

A2RAM is a 1T-DRAM device [1], which consists in a SOI MOS transistor with source and drain shorted by a resistive bridge (Fig. 1-a). The bridge is a doped layer (same type of doping as in source and drain) located at BOX/silicon film interface [2]. The memory operation is related to the presence of an excess or a lack of majority carriers (holes) in the body, which modulates the current flow through the bridge. A high amount of charge stored leads to '1' state and high read current (I_1). Conversely, in '0' state, the bridge tends to be fully depleted and the read current I_0 is negligible. Programming the '1' state is usually achieved by charge generation via band-to-band tunneling (B2B) at drain-body junction or by impact ionization (II) in the pinch off region of the top inversion channel [3]. Erasing is performed through capacitance coupling that evacuates the holes from the body (Fig. 1-a). The advantages of the II programming is the high writing speed and the drawbacks are the high power consumption and the reliability issues due to the hot carrier generation. For the B2B programming, the advantage is the low power consumption and the drawback is the slow writing speed.

The aim of this paper is to present a new way to program the '1' state in A2RAM which combines low writing time and low voltage operation. The method is evidenced at cell level by 2D simulations and then implemented in a 2x2 A2RAM matrix through TCAD mixed mode simulations.

II. Study of a single A2RAM cell with TCAD

A. Programming mechanism description

We highlight that, with proper programming bias applied on the gate (VgW) and on the drain (VdW), A2RAM '1' state writing can be performed more efficiently by impact ionization in the bridge. As shown on Fig. 2, charges are first generated by B2B (Fig.2-ii); they screen the vertical electric field induced by the gate and allow conduction in the bridge (Fig.2-iii), leading to the charge generation by impact ionization in the bridge (Fig.2-iv).

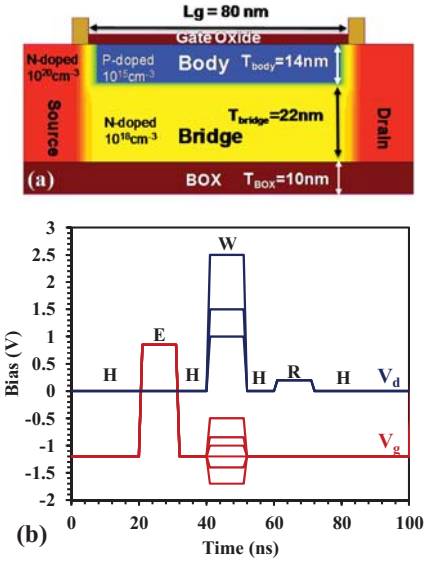

Figure 1: **(a)** TCAD A2RAM structure and main parameters, **(b)** Vd & Vg vs time for E-W-R sequence with a pulse width of 10 ns and rising/falling edge of 1 ns.

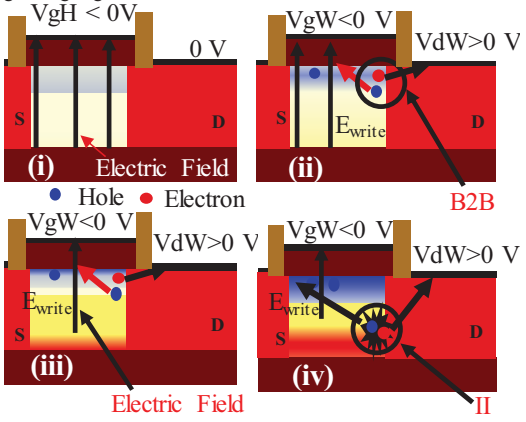

Figure 2: Description of the new A2RAM programming mechanism with the polarization applied on the gate and drain (the source is grounded), **(i)** Hold state (body and bridge are fully depleted), **(ii)** B2B generation due to VgW and VdW, **(iii)** Holes generated by B2B are stored in the body. Bridge current starts to flow. **(iv)** Activation of the II generation at bridge-to-drain junction which completes the programming and reduces the writing time at low VdW and |VgW|.

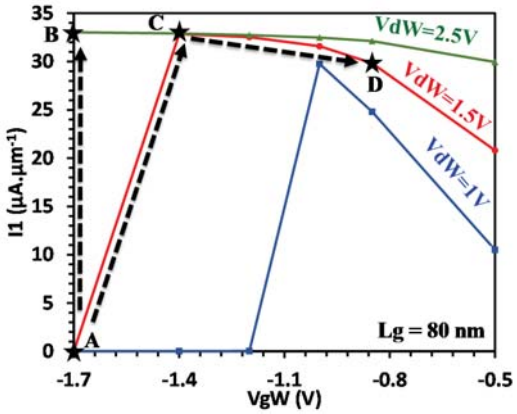

Figure 3. Read current I_1 versus the gate bias VgW applied during Write at different VdW (TCAD simulation).

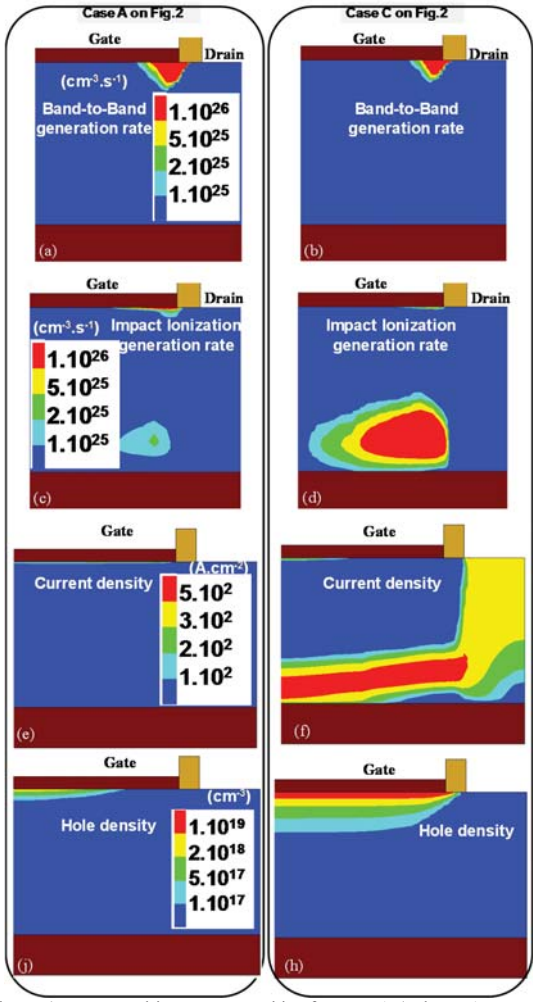

Figure 4: a, c, e and j are cartographies for case A (VdW = 1.5 V and VgW = -1.7 V) of Fig. 3 and c, d, f, and h are cartographies for case C (VdW = 1.5 V and VgW = -1.4 V). **(a,b)** B2B generation rate profile extracted at 10% of the writting time. **(c,d)** II generation rate profile extracted at 10% of the W; **(e,f)** Curent density profile extracted at 10% of the W. **(j,h)** Holes density profile extracted during the '1' state holding phase; all extracted from TCAD simulation.

B. PROGRAMMING MECHANISM EVIDENCE BY 2D TCAD SIMULATION

To evidence the programming mechanism, we have performed TCAD simulations [5]. A2RAM structure (Fig.1-a) is simulated with the technological parameters of [4]. The simulations use drift diffusion model, doping-dependent mobility, Van-Overstraeten model for II, and nonlocal path band-to-band tunneling model to account for B2B generation. Memory performance is evaluated using the operation sequence of Fig.1-b. The cell is first erased (E) to guarantee memory initial state, then '1' state is written (W) and read (R) with a hold (H) phase between each operation. The pulse width of each phase equals 10 ns and the rise and fall times are 1 ns. Since we aim to study the write 1 phase, different drain (VdW) and gate (VgW) bias are assessed.

Fig.3 shows the evolution of '1' state read current I_1 versus VgW for three different VdW. From A to B, VdW increases while keeping VgW constant: as expected, the B2B generation is enhanced leading to higher I_1. From A to C, I_1 increases if VdW is constant and |VgW| decreases. Albeit the gate-to-drain electric field is reduced as well as the B2B generation (confirmed by Fig.4-(a,b)), the II generation in the bridge becomes stronger (Fig.4-(c,d)). Indeed, the current density during W (Fig.4-(e,f)) indicates that current is flowing in the bridge only in case C. This is due to the stronger vertical electric field in case A induced by the higher |VgW| which makes the bridge fully depleted and prevents the conduction. Finally, Fig.4-(j,h) confirm that more holes are stored in the body in case C. So, with lower |VgW|, a larger amount of charge is stored in the body thanks to the II in the bridge. Still on Fig. 3, from C to D, |VgW| is further lowered at constant VdW, causing a slight I_1 decrease. Actually, reducing |VgW| leads to a source-body barrier potential decrease and consequently to a reduction of the amount of holes stored in the body (Fig.5-a). This mechanism is documented on Fig.5-b and on Fig.5-c which show the evolution of the electrostatic potential of the body during the '1' state write phase in case C and D respectively. Moving from the hold state to the beginning of the write phase (red curves on Fig.5-(b,c)), the depth of the electrostatic potential well in body is higher in case C than in case D. Thus, less holes are required in the body in case D to reach the equipotentiality between the source and body. This also explains why we need more time (*i.e.* more holes stored) in case C (Fig.5-b). Definitively, for weaker |VgW| than in case D, as the bridge is in conduction, the writing depends only on II in the bridge. To emphasize it, we represent along several cut lines at the start of the write phase (*i.e* Vg = VgW and Vd = VdW on Fig. 1-b): the B2B generation on Fig.6-(a,b), the current density on Fig.6-(c,d), and the impact ionization generation on Fig.6-(e,f). As described above, the B2B is lower for weaker VdW and VgW. For VdW = 1 V and |VgW| < 1.2 V, the B2B vanishes in the A2RAM structures (Fig.6-(a,b). However, we observe on

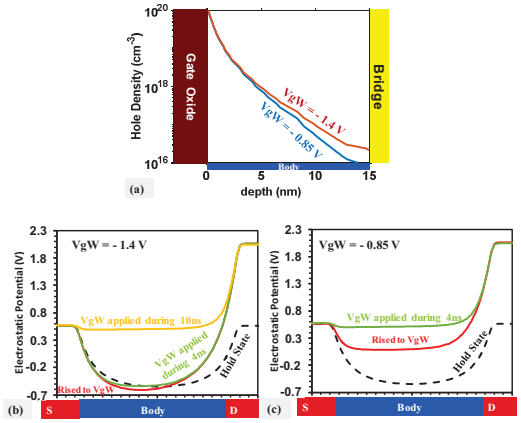

Figure 5: **(a)** Vertical holes density profile extracted during the '1' state hold phase from TCAD simulation. Evolution of the electrostatic potential from the holding state to 0, 4 and 10 ns of the writing state at the cutting line 1 nm below the gate oxide in **(b)** case C and **(c)** case D.

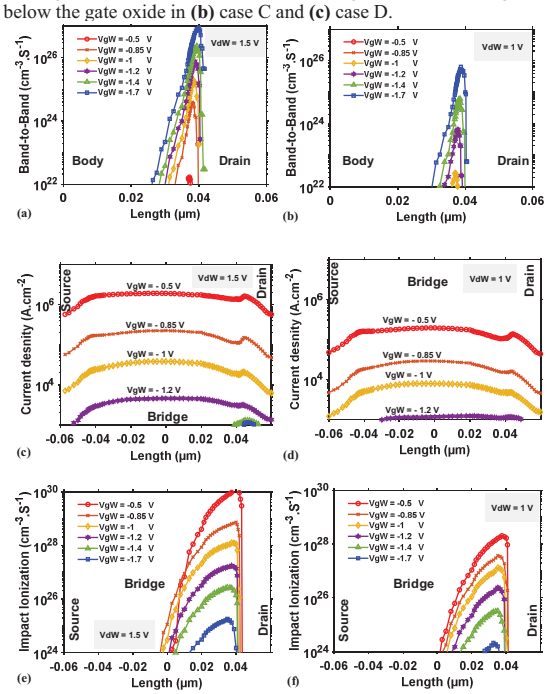

Figure 6. **(a,b)** B2B generation rate along the body-drain gate overlap region at the cutting line 1 nm below the gate oxide, **(c,d)** density of current along the source-bridge-drain at 5 nm above the BOX and **(e,f)** II rate along the source-bridge-drain at 5 nm above the BOX. All curves are extracted at the starting of the '1' state write phase.

Fig.6 (c,d) that the current density is higher for lower |VgW|, especially for |VgW|< 1.2 V, because the bridge is less depleted. The impact ionization generation at the bridge-drain junction increases (Fig.6-(e,f)) for lower |VgW| and, is the only mechanism involved in the A2RAM programming for |VgW|<1.2V. In other words, Fig.6 confirms that for |VgW| < 1.2 V the writing is achieved only by II. Therefore, the step consisting in a preliminary charge generation by B2B is not required (as illustrated on Fig.2-iii).

We now investigate the impact of the hold voltage VgHold (equal to the reading gate voltage) on the '1' state programming efficiency (W on Fig.1-(b)) and how it may affect the new mechanism. For low |VgW|, if Vg starts from

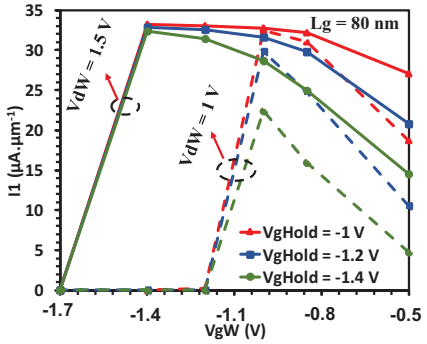

Figure 7: Read current I_1 versus the gate bias VgW applied during W at different VdW VgHold conditions.

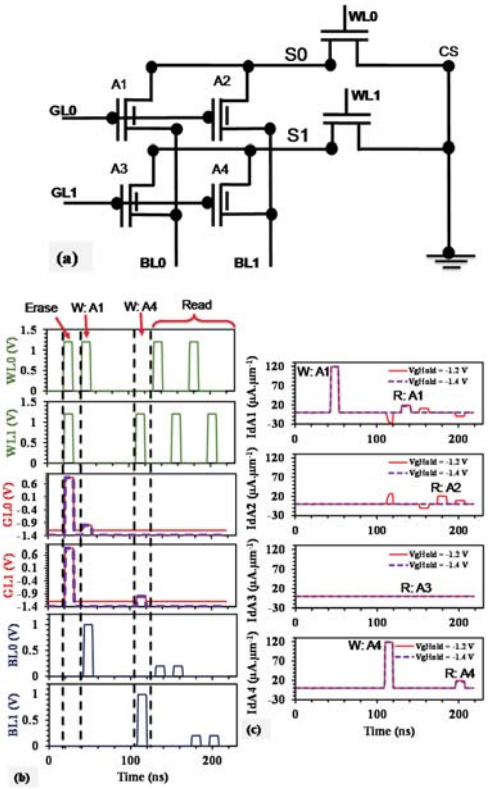

Figure 8: TCAD mixed-mode simulation of 2x2 A2RAM matrix: **(a)** schematic composed of 4 A2RAM cells (A1, A2, A3 and A4) and two selectors (MOS transistor).WL= Word Line BL: Bit Line, GL: Gate Line, and S: Source. **(b)** Pattern of bias applied on each node during the following sequence: full matrix eras-ing - A1 programming - A4 programming - full matrix reading. **(c)** Drain current vs time of each A2RAM cell during the memory sequence of 8-b for two different values of hold gate voltage V_{gHold}.

strongly negative VgHold value the impact ionization generation might not have enough time to be triggered (within the 10 ns of the pulse width) because the bridge needs first to be formed. In contrast, for higher |VgW| and lower negative VgHold, the impact ionization is rapidly triggered. We have performed similar simulations as on Fig. 3 but by varying VgHold. Note that VgHold needs to be sufficiently strong to guarantee high potential barriers between body and source-drain allowing to keep electrostatically the holes (information) in the body. I_1 versus VgW is shown on Fig. 7 for VgHold = -1 V, -1.2 V (reference case) and -1.4V: we notice that the

shape of the curves is the same. The slight variation of I_1 is related to the modulation of the bridge by the gate electric field (imposed by VgHold) during the '1' state reading phase. We conclude that VgHold does not affect significantly the programming mechanism. The optimum VgW remains around -1 V whatever VgHold is.

III. 2X2 MATRIX A2RAM: MIXED-MODE SIMULATION

The purpose here is to show a proof of concept of this A2RAM writing mechanism in a matrix environment. We consider a 2x2 matrix (schematic shown on Fig. 8-(a)) composed of four A2RAM memory points A1, A2, A3 and A4 (cell structure is described on Fig.1-a). The access of each row (Word Line WLi with i=0 or 1) is controlled by a n type 28FDSOI MOSFET [6]: if the row is selected (positive pulse applied on WLi), it connects the source electrode (Si with i=0 or 1) of each A2RAM cell to the ground. On a same row, A2RAM gate electrodes are connected to the Gate Line (GLi with i=0 or 1). On a same column, A2RAM drain electrodes are connected to the Bit Line (BLi with i=0 or 1). Erasing is performed on a full row while programming and reading are performed cell by cell in a given row. In this study, we first erase the complete matrix (Erase), then we program the '1' state on A1 (W :A1) and A4 (W :A4) and finally read the full matrix (Read). The voltage patterns are described on Fig.8-(b), the pulse width of each phase is still 10 ns and the rise and fall times are 1 ns. Note that for programming A1 and A4 cells we used VdW = 1 V and VgW = -1 V to remain in low voltage operation. From Fig.3 and Fig.7, the suitable value of gate voltage during hold operation is VgHold= -1.2 V.

To check matrix operations, we monitor the drain current (IdAi with i=1 to 4) of each A2RAM cell during the full memory sequence (Fig.8-c). On the second row, as expected, we read the '1' state current I_1 (R: A4) in A4 and the '0' state current I_0 (R: A3) in A3. On the first row, as expected we read the '1' state (R: A1) in A1, but, surprisingly, '1' state is read in A2 (R: A2) instead of the '0' state initially programmed. So, we have a parasitic writing in A2, and it has already been described as "gate disturbance" phenomena [7]. In fact, during the A4 programming, the first row is not selected so A2RAM source electrodes of this row are floating (equivalent circuit shown on Fig.9-(a)). It leads to a positive potential value on the source electrode of A1 and A2 (Vs0) (Fig.9-b), due to the BL polarization applied to program A4. Therefore, the gate-to-source voltage applied on A2 is VgHold-Vs0 ≠ VgHold (with Vs0 the source potential of A1 and A2), explaining the parasitic writing on A2. We demonstrate that the gate disturbance effect can be canceled if |VgHold| is increased. This is confirmed by mixed mode simulation on Fig. 8-c (dashed line, with VgHold=-1.4V instead of -1.2V). Still on Fig.8-(c), we can also notice that the '1' state reading current for A1 and A4 cells (dashed line) are slightly lower than the one read on Fig.3 (at VdW = 1 V and VgW= -1 V). This is because we have changed the VgHold value. In fact, as we have highlighted on Fig.7, I1 is reduced when |VgHold| increases. The key aspect is that the new A2RAM programming mechanism is compatible with matrix operation at low voltage.

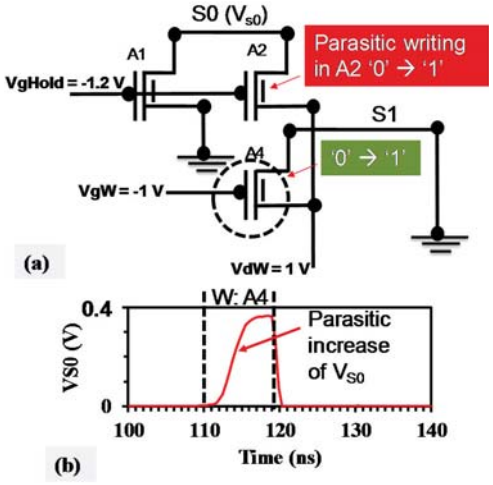

Figure 9: TCAD simulation of (a)- 2x2 matrix equivalent circuit during A4 programming with A1 holding '1' and A2 holding '0' (b)-Evolution of V_{S0} potential evidencing that A2 source potential variation is the cause of A2 parasitic programming.

IV. CONCLUSION

We have demonstrated that the '1' state writing of A2RAM can be performed with short programming time Tpt (≤ 10 ns) and low voltage (1 V ≤ VdW ≤ 1.5 V and 1.7 < VgW ≤ 0.5V) thanks to the impact ionization in the bridge. The new mechanism has then been used in 2x2 A2RAM matrix cells, which have been optimized to avoid perturbations.

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