TEM based dislocation auto analysis flow of advanced logic devices

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***Abstract*—Automatic flow of transmission electron microscopy (TEM)-based dislocation analysis on Source/Drain (S/D) and contact formation process is developed. Based on the previously developed model of dislocation stress, an automated methodology is implemented that allows fast and human-error-free extraction of dislocation core position and its impact on the device channel stress and the electrical performance. This approach enables us to analyze the impact of dislocations in S/D of advanced logic devices and to optimize structure and process conditions.**

Keywords—dislocation, Stacking fault, SiGe, epitaxy, channel stress, S/D stress, crystal defect

I. INTRODUCTION

The addition of the mechanical stress in the logic device channels has been one of the major performance boosters since 90 nm technology node [1]. At each new technology node, higher stress value was needed to meet performance boosting goals, especially for PMOS FET devices. As the dimension of semiconductor devices scales down, transistor design and fabrication encounter significant challenges to boost performance: typically increase of stress levels in the device channel is achieved by introducing high concentration of Ge in source and drain regions of the devices. However, in advanced nanoscale transistors dislocations prevent sufficient stress buildup in the channel. This is a chronic issue in advanced logic devices. Especially for FinFET technology, as dislocations are even more abundant than before, dislocation control becomes one of the most important performance knobs. Therefore, analysis of dislocations becomes critical for process technology optimization. However, dislocation engineering is hampered by the fact that accurate prediction of the effect of dislocations on the electrical performance of device needs precise information on the atomic structure of the dislocation. Extraction of the dislocation position and properties from experimental data for real devices requires analyses of multiple transmission electron microscopy (TEM) images and scanning transmission electron microscopy-geometrical phase analysis (STEM-GPA) data. This work is typically done manually for multiple process condition splits, which decrease dislocation analysis efficiency and introduces human errors in the process optimization flow to find dislocation free conditions. Therefore, the present work is focused on the development of a Automatic flow of TEM based crystal-defect analysis system for SiGe S/D regions of advanced PMOS devices.

II. SIMULATION FLOW & METHODOLOGY

The proposed analysis flow consists of three stages: 1) dislocation core position is extracted from TEM image of device S/D region; 2) dislocation type is defined by reverse engineering of local atomic configuration; 3) TCAD simulations of expected device performance in the presence of dislocation are performed. For this analysis flow this approach has been made of three parts: A) image processing; B) atomistic emulated TEM; C) channel stress calculations by TCAD stress simulation.

A. Dislocation stress analysis by image processing

For the first stage of the flow, a specially developed image processing algorithm searches for irregularities in the high-resolution TEM micrograph of device S/D area cut along the device channel. Irregularities of the crystal lattice structure are detected and marked automatically and the positions of potential dislocation cores are detected (Fig. 1). Machine learning (ML) methods are used to compare dislocation signatures extracted from real TEM image with signatures from emulated TEM database with various dislocation types and configurations. Both positions and types of eventual dislocations are extracted from TEM images and compared with emulated TEM [2].

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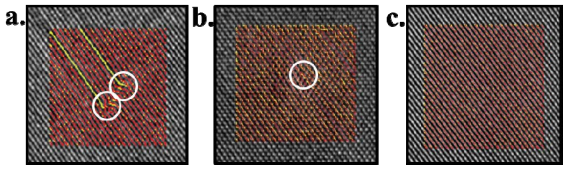


Fig. 1. The image analysis of dislocation core based on high-resolution TEM images. Structure with 2 cores (a), with 1 core (b), without defect (c).

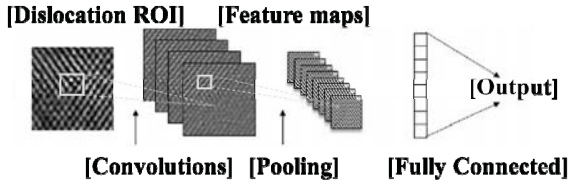


Fig. 2. The data extraction flow with region of interest (ROI) based on CNN method.

This comparison is done by Convolutional Neural Networks (CNN) [3] which is a deep learning method that has high accuracy and often used for image classification. But depended sample and condition when take a TEM, It has various quality. Therefore, to achieve high accuracy, a new algorism which can extract the more specific feature value combined with CNN has been developed (Fig. 2).

- Use small cut area image from TEM for input data and extract dislocation signature.
- Compare a signature of experimental data with the database of atomistic emulated TEM images of various configurations and types of dislocations in silicon crystal lattice
- Evaluate similarity with the ML algorithms and select up to three potential nominees to evaluate lattice defect effect.

B. *Dislication stress analysis by atomisitic emulated TEM*

A database of atomistic structures of silicon dislocations was built to identify a type of dislocation by emulated TEM signal signature. Corresponding dislocation core parameters (Burges vector) are also defined and used to calculate resulting dislocation-related stress.

1) Dislocation modeling in cubic diamond silicon : In the cubic structure, the planes of highest lattice site density are the {111} planes. These planes contain the minimum lattice translations in <110> directions; therefore they become preferred slip planes. The slip system is defined by the plane and the direction of slip, conventionally written as <110>/{111}. Basic dislocation types in this slip system are:

a) The screw dislocation with the line direction and Burgers vector parallel, e.g., $l_s = [11\bar{0}]$ and $b_s = 1/2\ [11\bar{0}]$.

b) The edge dislocation with line direction and Burgers vector perpendicular, e.g., $l_e = [1\bar{1}\bar{2}]$ and $b_e = 1/2\ [1\bar{1}0]$.

c) The 60^o mixed dislocation, where line direction and Burgers vector form an angle of 60^o, e.g., $l_{60} = [11\bar{0}]$ and $b_{60} = 1/2\ [01\bar{1}]$.

Fig. 3 and Fig. 4 show most common dislocations in silicon but to identify dislocation type properly we have to consider all possible dislocation core configurations that may exist due to lattice symmetry.

2) Dislocation core database creation : There are totally 12 slip systems due to cubic symmetry and dislocation core may have two types (glide and shuffle) according to local symmetry of a {100} plane. Furthermore, we consider edge and screw dislocations and each dislocation may dissociate to partial dislocation which are more energetically stable in silicon. Combining all possibilities we accumulated 1920 dislocation structures and the final database included 5760 emulated TEM data. To take into account inevitable variation in experimental data, the database contains emulated TEM images with slightly tilted structures to reflect non-ideal cuts of real TEM samples.

3) TEM signal emulation : Although HR-TEM can be precisely simulated by the well-known multislice method, routine calculations for the systems containing several millions of atoms for real scale device are not yet practical due to the huge computational costs. In the present work more simple equation, proposed in [4] was used to generate a database of emulated TEM images. Emulated TEMs were produced considering intensity of the Poynting vector of a monochromatic beam [5] as follows:

$$I(r,z) = \frac{|Re(E \times H^*)|}{2} = \frac{|E(r,z)|^2}{2\eta}$$

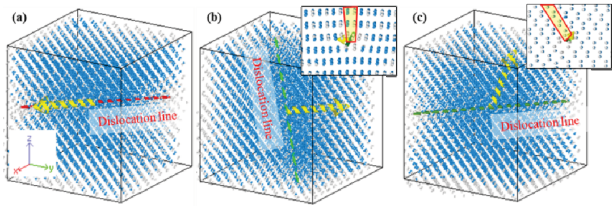


Fig. 3. A screw dislocation (a), an edge dislocation (b), a 60° mixed dislocation (c). Insets in (b) and (c) show additional half planes inserted.

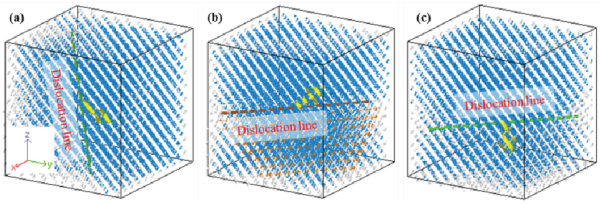


Fig. 4. A 60° Shockley partial dislocation (a), a 30° Shockley partial dislocation (b), and a 90° Shockley partial dislocation. (c).

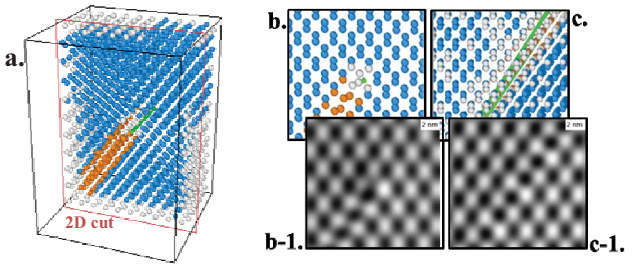


Fig. 5. The atomic structure with dislocation was built by atomic simulation (a). 2D cut plane at different coordination (b, c) and emulated TEM image from each 2D cut image (b-1, c-1).

In spite of approximations of this approach, emulated images of dislocation cores closely followed real TEM images (see Fig.5 for emulated TEM examples).

For each of dislocation core types from DB a set of emulated TEM images (including structure distortions) was generated and a dislocation core signatures were extracted by machine learning algorithm.

C. *Dislocation stress analysis on real device structure by stress simulation*

A multi-scale TCAD simulation is performed to calculate a dislocation-related stress change in the device channel and extract electrical performance. This multi-scale simulation combines conventional continuum process simulation approach similar to the one used in commercial TCAD tools [6] with atomistic stress simulation by valence force field (VFF) method [7] and a multi-scale epitaxy and contact formation simulation methodology [8,9]. All process steps before S/D formation are simulated following typical continuum-based TCAD simulation flow and then kinetic lattice Monte Carlo (KLMC) method [8] is used for the epitaxy simulation and accurate prediction of Ge and dopant distributions in S/D structure (Fig. 6).

After formation of S/D regions based on dislocation core position and type extracted from TEM image, a dislocation stress is calculated using the VFF method coupled with the finite element method (FEM) [7] and the dislocation stress model that was developed within FEM framework [10]. The resulting stress were verified by comparison with Modified Embedded Atom Method (MEAM) [11] simulation results, see Fig. 7 for details.

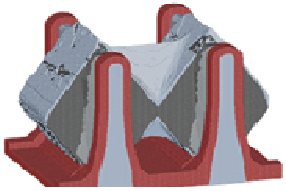


Fig. 6. A S/D shape predicted by a previously developed KLMC model [9].

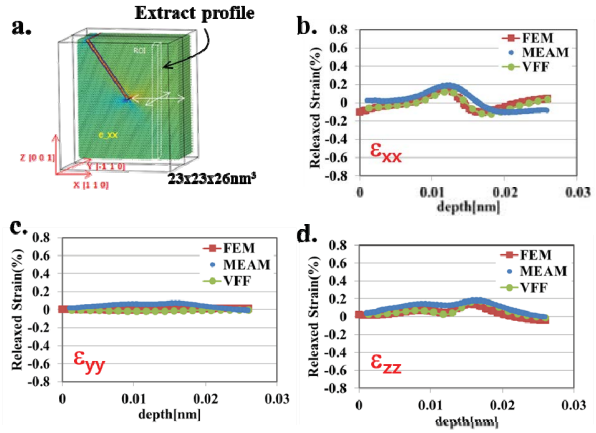


Fig. 7. A crystal-defect stress (stressXX (b), stressYY (c), stressZZ (d)) of VFF-FEM method and developed FEM-only stress model were verified for an atomic structure (a).

III. Channel Stess Simulation

Finally, after application of multi-scale contact formation simulation [9], the final value of mechanical stress in the channel is extracted along with active dopant distributions, and simulation of electrical properties of the device is performed.

The dislocation, a dislocation core is placed in the simulation structure based on the TEM image. For everyday simulations the VFF-FEM model is not always practical due to large its simulation time. So specially developed FEM-only dislocation stress model has been used. The model accurately calculates dislocation stress in confined nanoscale structure and can support automatic dislocation core positioning at interface with surrounding materials to take into account stacking fault termination at the boundary of epi-grown structure (Fig. 8) [10]. The model supports any dislocations with arbitrary Burgers vectors. The data are provided to the dislocation stress model which solves stress equilibrium considering not only dislocation core stress, but also stresses generated by lattice mismatch in the device structure, thermal expansion coefficient mismatch stress and also extrinsic stresses that may be present in real device structure (for example due to local layout effects).

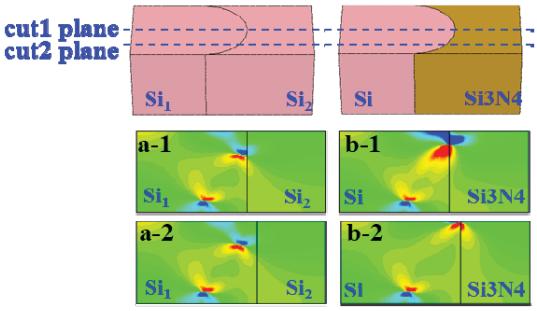
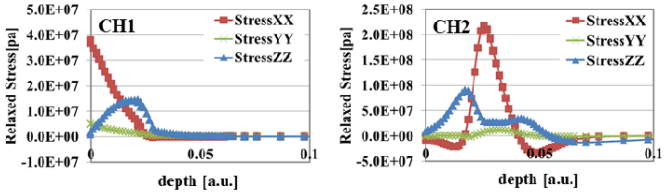


Fig. 8. The dislocation area was defined by options. The start and end point was defined in same material cut1 plane is a-1, cut2 plane is a-2 and curved dislocation was finished as Si/Si3N4 interface cut1 plane b-1, cut2 plane b-2.

Examples of application of methodology for two adjacent devices with DL core in common S/D is shown in Fig. 9 and device performance drop due to the presence of dislocation in S/D region is shown in Fig 10. Exact amount of device performance degradation strongly depends on dislocation core type, position and number of dislocations in the S/D region. The probability of dislocation formation has a deep connection with epitaxial growth process recipe. Therefore, the developed methodology allows means of TCAD-based process conditions optimization.



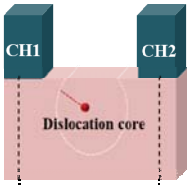


Fig. 9. The stress relaxation by only dislocation was estimated based on the structure of advanced logic device at both channels (CH1, CH2). The dislocation is a 3D defect, so effects are different at both sides.

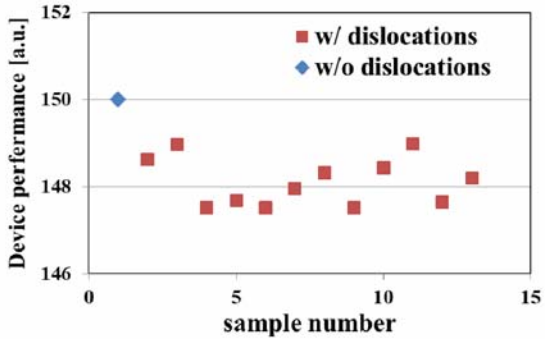


Fig. 10. Device performance depends on dislocation type and location from device simulation.

IV. CONCLUSION

A methodology for automatic analysis of S/D dislocations in advanced logic transistors and related channel stress prediction via multi-scale TCAD simulation has been developed. The analysis flow is a combination of image analysis, atomistic dislocation structure reverse engineering by emulated TEM and stress simulation with atomistic KLMC epitaxy and contact formation simulation based on multi-scale simulation flow that was developed before [9]. Combination with a FEM dislocation stress simulation model allows fast, efficient and quantitative analysis of the S/D epitaxy quality and its impact on the device electrical performance. Most importantly, thanks to the developed methodology, presented simulation flow decreases researcher's workload and reduces amount of human errors during experimental data analysis.

Additional connection between process recipe and stress level could be possible by coupling equipment level simulation and KLMC epitaxy model by introducing a local flux dependent deposition rate.

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