The efficient DTCO Compact Modeling Solutions to Improve MHC and Reduce TAT

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***Abstract*—This paper introduces the recent modeling challenges of the Process Development Kit (PDK) development due to the limitations of transistor scaling and the impact of new process technologies. And a new modeling solution, Agile PDK is presented to break though these development challenges by enabling the Design Technology Co-Optimization (DTCO) activities in the manufacturing levels. A series of advanced algorithms are newly introduced to not only reduce the PDK development time (TAT), but also improve the model accuracies and Model-to-Hardware Correlation (MHC). It is applied to the latest DRAM technology and dramatically reduces the development TAT up to 50% with improved model accuracies.**

Keywords—PDK, DTCO, SPICE Models, MHC, TCAD TEG, Full binning, Regression, Optimization, and API

I. Introduction

PDK models play a very important role in the advancement of CMOS technology and they are the key bridges between the fabrication process and IC designs. Since the CMOS technology is aggressively scaled down and the physical process limit is reached, the PDK models have emerged to meet the needs of various secondary effects and non-monotonic device trends as well as many types of variation characteristics. To accept these challenges, most industries have introduced more complex models as shown in Fig. 1.

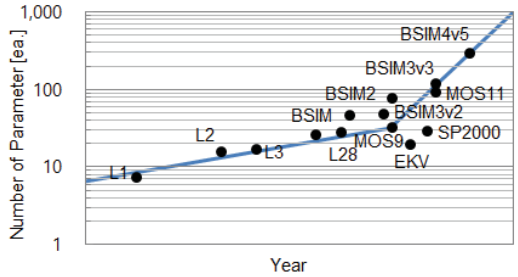


Fig. 1. The number of model parameters. It is increasing dramatically to capture the scaled transistor's characteristics. However, it is becoming more difficult and getting longer time to extract parameters with same accuracies.

However, the more complex parameters are used, the more PDK development time we need. It is one of the biggest risks in these aggressive Lg-scaling competitions, because the variable silicon data and narrower design margins cannot be compensated in a timely manner. Moreover, the various effects of new process or technology (i.e. High-K or stress effects in Memories, and the multiple channels in Logic technologies, etc.) need to be evaluated in the circuit domain as quickly as possible due to their radical effects in the performances. Therefore, the Design-Technology Co-Optimization (DTCO) activities become crucial in the early state of technology developments as shown in Fig. 2. However, the PDK modeling of these technologies so highly depends on the each modeler's expertise, that the trade-off relation between the model quality and the development cost still remains the bottleneck of these co-optimization activities.

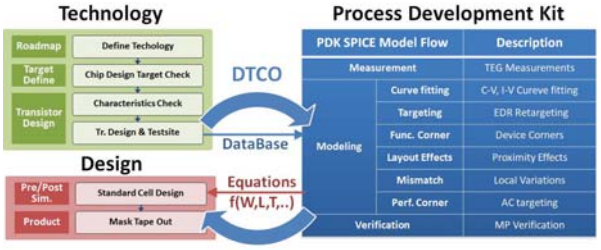


Fig. 2. The development flow of Semiconductor products and the Design Technology Co-Optimization (DTCO) activities with the agile PDK solution.

Therefore, we proposed a new generation modeling standards to change the paradigm of these time-dependent and labor-intensive PDK model developments for the early stage's technology defining. To cope with these chronic trade-off relations, we introduced a full binning algorithm to capture all geometry's device characteristics more accurately, and advanced optimization algorithms to automate the full development flow to break through the conventional limitations.

II. The Chronic Problems of General PDK Models

A. Accuracies

For several decades, only one set of model parameter called 'global model' was widely used for all devices with those scalable parameters as shown in Fig.3(a). Recently, the higher

model accuracy has been required for circuit designers. Therefore, many PDK models adopted the binning approach as shown in Fig.3(b). However, this strategy requires many model cards to be generated and increases the turnaround time (TAT)[1].

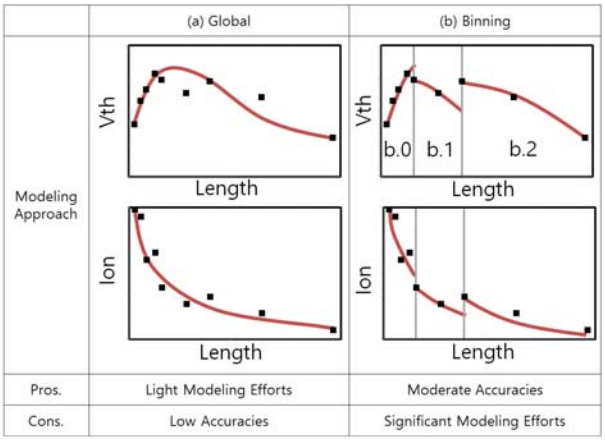


Fig. 3. The comparison of PDK modeling strategies: (a) Global modeling approach is applied to have smooth and continuous characteristics all over the geometry region using only one set of model parameters (b) Binning approach is applied to reduce total RMS error by separating the geometry region into each bin area. Accuracy is improved, but discontinuities or abrupt changes always occur.

B. *MHC (Model to Hardware Correlations)*

Fig.4 (a) shows an example of the general TEG matrix. The devices are gathered in a dog-bone shaped region due to the limitations of chip area and cost. Fig.4 (b) shows an example of the geometric device usages in a logic circuit. The devices were being operated in all geometric sizes and they all need to be modeled to improve the MHC qualities.

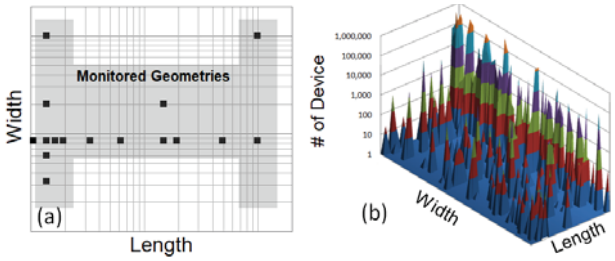


Fig. 4. (a) An example of the general TEG matrix with chip area limitations. (b) An example of the geometric device usages in a sample logic circuit.

C. *TAT bottleneck*

Table.I shows an example of the industry's average TAT for the PDK modeling. Generally, most steps are so highly rely on the human resources that the development TAT is depends on the #modelers, #DUT targets, and accuracy tolerances. Fig.5 represents the conventional development framework which has strong trade-off between cost, resources, MHC, and accuracies.

TABLE. I. A example of PDK SPICE modeling scopes and development time.

General modeling scopes		TAT	
(Meas.+) Curve fitting	C-V, I-V, Igate, Junctions	(1.5+) 2	7.5 Weeks
Retargeting	ET Centering	2	
Corners	Global Variations	0.3	
Local Layout Effects	Systematic Variations	1	
Mismatch	Random Variations	0.2	
Delay	AC targeting	0.5	

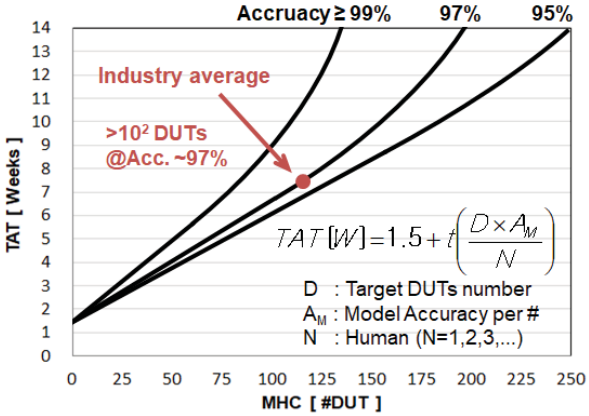


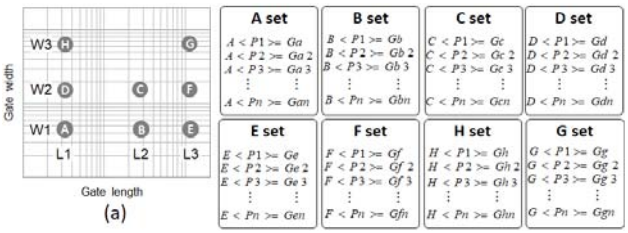
Fig. 5. The conventional PDK development framework which exhibit a strong trade-off between cost, resource, #targets, and accuracy tolerances.

III. AGILE PDK: THE NEXT GENERATION MODELING SOLUTION

A series of advanced modeling algorithms are newly introduced to break through these old and chronic limitations.

A. *The user-defined Regression Algorithm in API*

A full binning strategy is proposed as a new paradigm to achieve high modeling efficiency. To improve the model accuracies, the all targets are divided into each size as shown in Fig. 6(a). And each model parameter set is extracted automatically at each size because more fast and accurate extraction results are generally guaranteed when there is no need to consider the different sizes. This new approach also can expand the TEG coverages (MHC increases) without any TAT burdens. Especially, the devices on the corner region of the matrix are critical which have the size related secondary effects. Therefore, these corner devices are benchmarked across the previous tech nodes or evaluated using the TCAD. Once the all DUT targets including these expanded devices are evaluated, the efficient (next section's) optimization algorithms can automatically extract the individual parameter cards in the parallel processing. Finally, a user-defined regression formula can connect the fully binned targets in the application program interface (API) regardless of the SPICE model's types or versions as shown in Fig.6 (b).



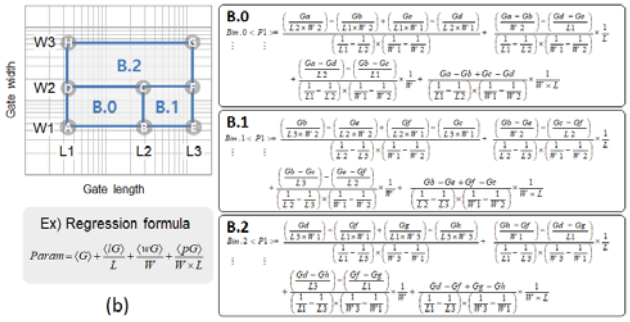


Fig. 6. The figure shows an example of the 8 different initial model cards (A,B,C,…H) and their final 3 sets of model card (Bin.0,1,2). (a) A full binning approach for the parallel processing. (b) Model parameters as the user-defined regression variables.

B. *The Advanced Optimization Algorithms*

Mathematically, MP extraction is basically a task of finding parameter vector P for which the cost-function can be minimized:

$$CF(P) = \sum_{i=1}^{m} \left\{ e_{Mi}(m) - e_{Ti} \right\}^2 \qquad (1)$$

where e_{Mi} represents a modeled electrical parameter, e_{Ti}. represents an electrical target, and CF(P) represents the cost-function to be minimized. One of the main issues in optimization is finding global minima of non-convex functions. Fig.7 shows an example of such a complex function with several local minimas and maximas. Therefore, a robust flow-based algorithm which combines both stochastic and iterative optimizers is adopted to reduce the large TAT and the risk of getting stuck in local minima as shown in Fig.8. Table. II shows the list of optimizer algorithms employed in this work.

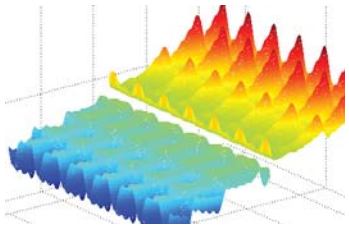


Fig. 7. The very complex function with several minimas and maximas of the SPICE models (correlated/nonlinear/constrained optimization problem)

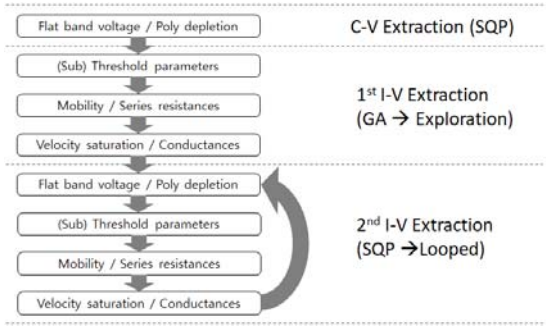


Fig. 8. Model parameter extraction flow using optimization algorithms in this work.

TABLE. II. The list of optimizer algorithms in this work.

Optimizer	Type	Search
Sequential Programming (SQP)	Iterative	Local
Newton Line-search	Iterative	Local
Genetic Algorithm (GA)	Stochastic	Global
Multi start SQP	Stochastic	Multiple

IV. Application to the Latest DRAM Technology

These new modeling solutions are verified by the latest DRAM technologies.

A. *High accuracy achievements*

Fig.9 and 10 show the results of C-V/I-V curve optimization and Fig.11 shows the results of ET target optimization. The fitting errors are around 3% for both curve-based and ET-based extractions. Fig.12 shows the SPICE results after the full binning algorithm which are completely continuous along W/L in contrast with the conventional approach in Fig.3 (b).

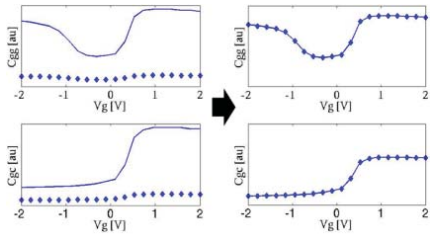


Fig. 9. C-V optimization algorithm results.

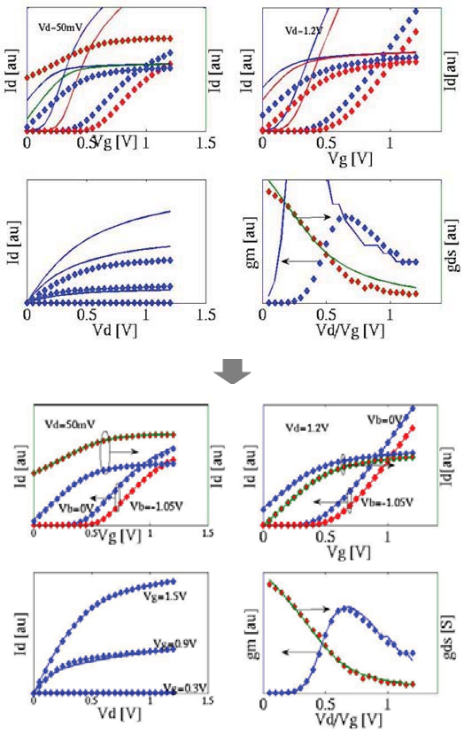


Fig. 10. I-V optimization algorithm results. Top figure shows the model before this algorithm (solid lines : Model, markers : H/W)

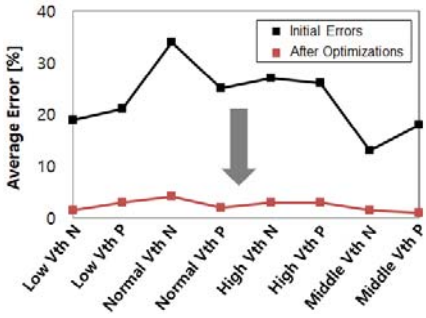


Fig. 11. ET target optimization (ET centering).

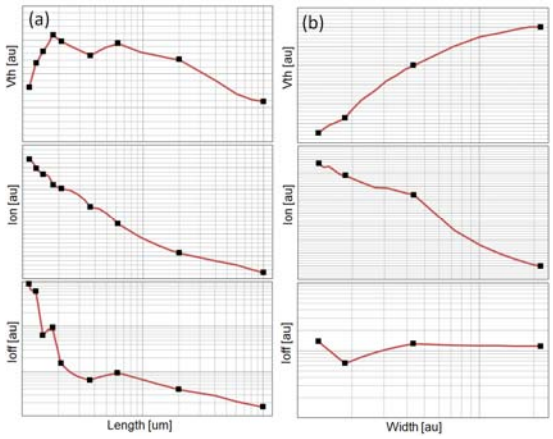


Fig. 12. Modeling results of this regression and full binning optimization. Very accurate and continuous along (a) channel length, and (b) width in contrast with conventional discontinuous model in Fig. 3(b).

B. *Remarkable MHC improvements*

The new PDK model also supports the full coverage of TEG matrix with only several corner device evaluations as shown in Fig. 13. The common models cannot cover all geometries, so the PDK generally had a recommended design rules. By contrast, this new modeling solution is able to support the 100% TEG coverages utilizing corner target evaluations regardless of any time or area limitations with the TCAD and the parallel optimization algorithm's assistances.

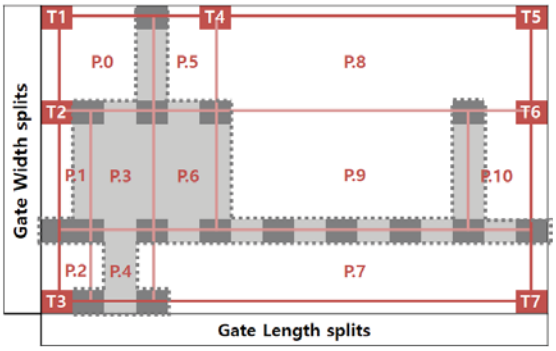


Fig. 13. The comparison of modeling coverages between a common example model (dotted line) and this work (Solid line with the TCAD evaluations of corner devices).

C. *TAT breakthrough*

The TAT could be dramatically reduced by these paralleled and automated algorithms. Fig.14 shows the comparisons of the total TAT to perform more than 7 modeling step examples, and it can be reduced up to 50% by introducing these new algorithms at the repetitive and iterative 3 steps. In addition, the TAT became the only function of the optimizer's performance which means it break through the chronic development bottlenecks: trade-offs between TAT, Resources, MHC, and Accuracies. It changed the development framework as shown in Fig.15.

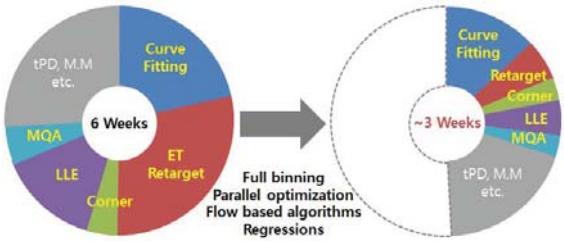


Fig. 14. PDK modeling TAT can be reduced up to 50% by introducing the regression and full binning optimization algorithms in the repetitive fitting steps, such as Curve fitting, Retargeting, and LLE modeling.

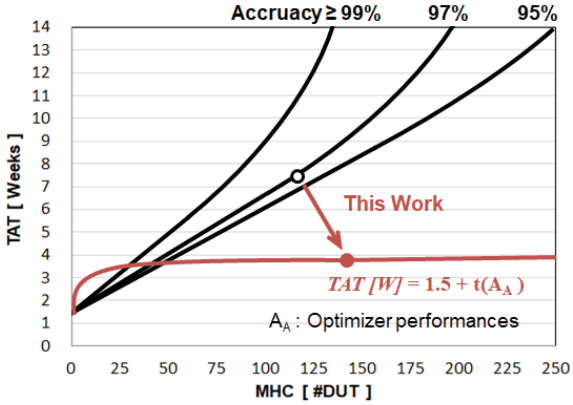


Fig. 15. The PDK modeling TAT is only depends on the algorithm's performances. This new PDK development framework can break through the chronic development bottlenecks: trade-offs between TAT, resource, #targets, and accuracy tolerances.

V. Conclusion

A series of modeling algorithms are introduced, and it solves the chronic PDK model problems of accuracy, discontinuity, MHC, and TAT as well as the TEG area limitations. It is also applied to the latest DRAM technology, and improves its model quality (Max error <3%) even in the short time. (TAT<50%) This methodology also enables the developers to co-optimize the technology and circuit-design using full TEG matrix covered PDK in the early stages. These modeling solutions are going to be the next generation modeling standards for the fast and efficient DTCO activities as well as the robust product circuit designs.

References

[1] SAMMAR K. SAHA, Compact Models for Integrated Circuit Design : Conventional Transistors & Beyond, 4-8, CRC Press (2016)