Intelligent DTCO (*i*DTCO) for next generation logic path-finding

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Abstract

Intelligent design technology co-optimization (iDTCO) methodology for next generation logic architecture path-finding and its application results are presented in this paper. There are 2 major steps in our iDTCO framework; standard cell (STC)-level iDTCO and block-level iDTCO. STC-level iDTCO, the main focus of this paper, consists of 4 major components; (1) full 3D process emulation with litho contour of standard cell (STC) layout, (2) auto-extraction of transistor compact model & parasitic RC extraction (PEX) in 3D, (3) performance-power-yield (PPY) analyzer, (4) multi-objective optimization of layout & process assumption (PA) to get best PPY. Applying our STC-level iDTCO flow to logic arch path-finding, we could speed up our PPY analysis TAT by 5~10 times with good accuracy of >95%.

1. INTRODUCTION

Typically, there are 4 phases in path-finding DTCO; (1) Setting scaling targets, (2) Architecture definition, (3) standard cell-level optimization, and (4) block-level optimization. Meeting performance-power-area-yield, so called PPAY, targets has been a continuous challenge in every logic generation, due to lack of new performance knobs and its increasing complexity of new processes introduced in the new node. In path-finding DTCO for next logic node definition, the role of TCAD has been extended from transistor-level to STC-level like Inverter (INV), 2-Input NAND (2ND), 2-Input NOR (2NR), Filp Flop (FF), and AND-OR-Invert (AOI). With delay in the advent of high mobility channel like Ge & III-V, there are few available performance boosting knobs in transistor-level. In consequence, STC-level DTCO to squeeze hidden performance out of STC design has become crucial even in path-finding stage. Therefore full 3D TCAD simulation in STC level including MOL/BEOL has become mandatory nowadays.

The main focus of conventional DTCO was to introduce numerous lithographic techniques to improve resolution [1] such as optical proximity correction (OPC) and inverse lithography technology (ILT), which are still important. However, in recent node beyond 10nm, the impact of design parameters on PPY has increased sharply by adopting many aggressive design knobs to achieve hyper scaling [2]. In consequence, PPY analysis in early stage of technology definition has become so important that many EDA/TCAD vendors have proposed their own DTCO solutions. [3,4,5] However, there are still many remaining issues hindering the active application of these solutions in the field, which will be discussed in detail later.

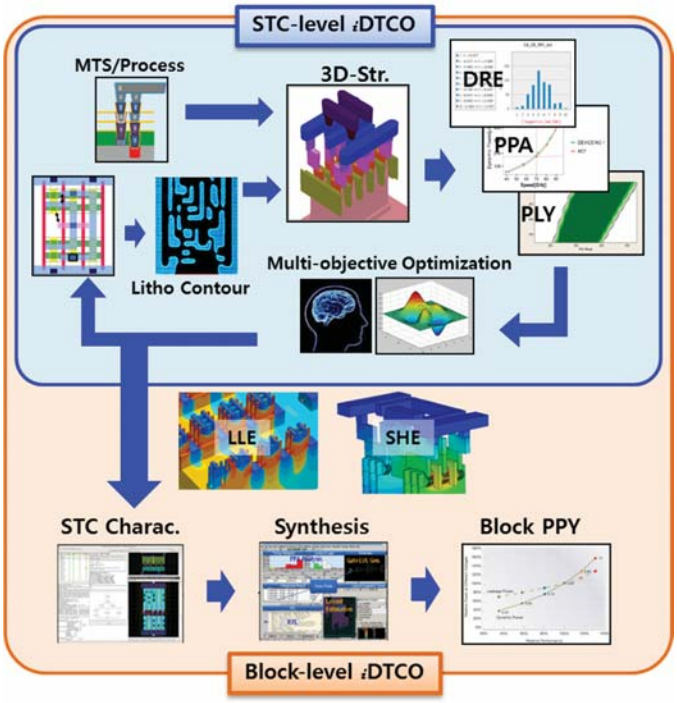

Figure 1 Schematics of STC-level and block-level *i*DTCO

Figure 1 shows the schematics diagram of overall iDTCO flow, which consists of STC-level iDTCO and block-level iDTCO. STC-level iDTCO consists of 4 major components; (i) full 3D FEOL/MOL/BEOL structure emulation with MTS & process assumption (PA) and its litho contour based on OPC model, (ii) Auto model parameter (MP) extraction & parasitic

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RC extraction (PEX) in 3D, (iii) PPAY analysis, such as performance-power for INV/2ND/2NR, area for FF/AOI, and parametric yield for SRAM, and (iv) Automatic layout handling and multi-objective optimization powered by machine learning algorithm. In sequence, block-level iDTCO consists of (i) STC characterization, (ii) synthesis with design compiler, and (iii) block-level PPA analysis along critical timing path. In between STC-level iDTCO & block-level iDTCO, it is important to assess local layout effect (LLE) & self- heating effect (SHE) considering neighboring cells & driver sizes.

2. STC-LEVEL iDTCO

In recent node beyond 10nm, many aggressive area-scaling knobs like single dummy gate and contact over active gate [2] have been introduced to achieve hyper scaling as shown in Fig.2. So that realistic 3D structure generation for parasitic RC extraction has become very crucial for better predictability in STC-level iDTCO. The key features & technical issues for each simulation step are as follow;

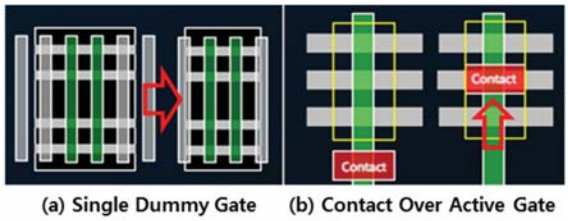

Fig. 2 Typical design knobs for hyper scaling beyond 10nm

(i) 3D structure generation with litho contour of drawn layout: Full 3D device geometry is generated using state-of-the-art process emulators like Synopsys Process Explorer™ & Coventor SEMulator3D™ to check the process margin of given process assumption (PA) for DFY & GRV. Fig.3 shows the typical examples of 3D structure generation in STC level iDTCO. The key challenges in this step are 1) getting realistic litho contour with OPC model in early tech. definition stage and 2) minimizing number of mesh with structural details like diamond-like epi shape in source/drain considering accuracy-TAT trade-off.

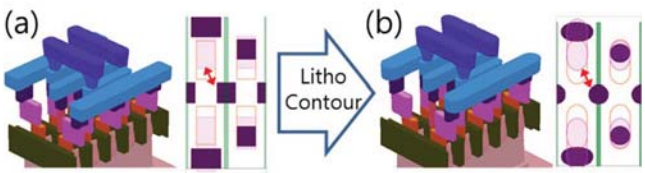

Fig. 3 3D process emulation with litho contour

(ii) Auto compact model parameter (MP) & 3D-PEX extraction: To extract transistor compact model automatically from the IV/CV curves generated by device TCAD simulation, Synopsys Mystic™ is used. It is very useful solution except lacking target-based MP extraction function. In early path-finding DTCO stage, not only IV/CV curve-based MP extraction but also target-based MP extraction is important because some performance knobs are hardly captured in DD framework without implementing new TCAD model (i.e.NC-FET).

Moreover, with drastic scaling of STC dimension, mesh optimization for 3D PEX has become crucial to avoid artificial resistance increase. Fig.4 shows the trade-off between the accuracy of via resistance and simulation time depending on mesh size. According to our result, too large mesh size can increase via R max 25% artificially. Parallel field solver and adaptive mesh refinement would be helpful to prevent this kind of artifact.

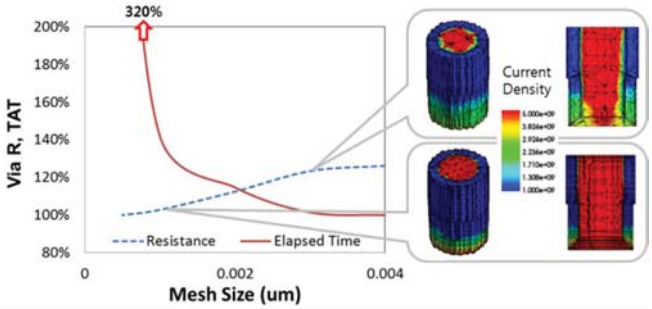

Fig.4 Trade-off between via R accuracy and 3D PEX simulation TAT depending on mesh size

Fig.5 shows the different contact size impact on RO Reff depending on PEX tools; conventional 2D PEX (StarRC™) vs. full 3D PEX (Raphael™). 3D PEX result shows steeper Reff trend than 2D PEX, which is more physical when we considers the increased portion of barrier metal layers within contact. What it means you should calibrate 2D PEX model based on 3D PEX result at all cost.

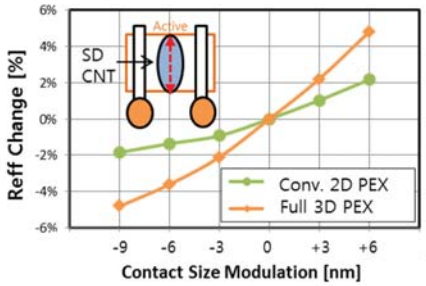

Fig.5 The impact of SD contact size on Reff in 2D & 3D PEX

(iii) PPAY analysis: Once device compact model and 3D PEX model are ready, the next step is to run SPICE simulation to assess circuit performance and to check the impact of process condition & critical dimensions on yield. However, the

type of STCs to be assessed for performance-Power (PP), area (A), and parametric yield (Y) are different. Typically INV/2ND/2NR cells for performance-power, FF/AOI cells for area, and SRAM cells for yield are evaluated at least. So it is very challenging to assess PPAY simultaneously in time!

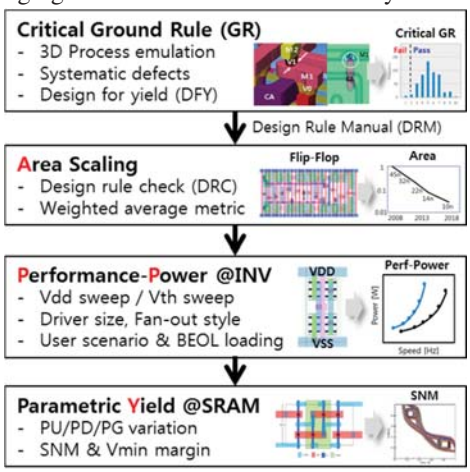

Fig.6 PPAY analysis flow in STC-level iDTCO

Fig.6 shows detailed PPAY analysis flow in STC-level iDTCO when target CPP & Mx (metal pitch) are decided. At first, critical ground rules (GR) should be check with realistic 3D process emulation. Chronic systematic defects related to critical GR should be screened out at this stage with high-sigma statistical variation, which results in the update of design rule manual (DRM). Secondly, all types of STC should be redrawn with new design rule to check area scaling in new node. Large standard cells like FF/AOI are checked at this stage to take into account metal congestion impact on area scaling. Thirdly, Performance-power trend is checked for basic STCs like INV, 2ND, and 2NR. Driver size, fan-out style, Vdd/Vth sweep, user scenario for dynamic power, and BEOL RC loading should be aligned for fair comparison. At last, parametric yield should be assessed for 6T-SRAM bit-cell with statistical variation of pull-up (PU), pull-down (PD), pass-gate (PG) transistors. Based on the read/write/disturb margin at each Vdd, Vmin margin is decided.

For fast but accurate yield assessment, state of the art yield estimation technique is applied to iDTCO platform combining neural network (NN) algorithms and advanced Monte Carlo (MC) as shown in Fig.7(a). By re-sampling on failure surface after initial pass-fail evaluation in Fig.7(b), we could get stable convergence of failure rate as shown in Fig.7(c).

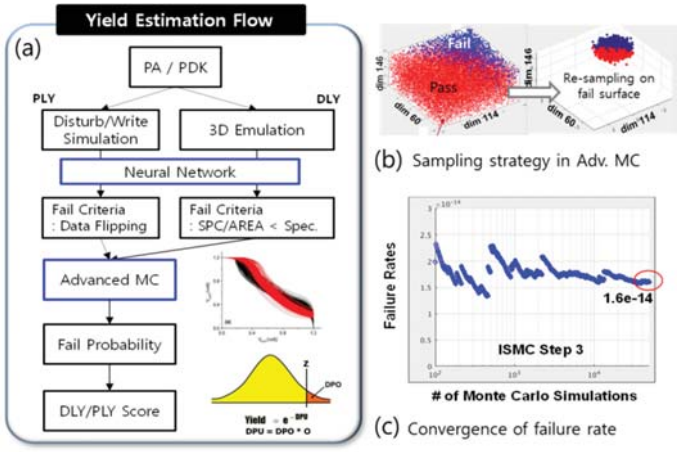

Fig. 7 Yield estimation flows combining neural network engine and advanced Monte Carlo engine for yield assessment.

Fig.8 shows Z score trend depending on sampling number in (a) conventional MC and (b) advanced MC. With conventional MC in Fig.8(a), Z score fluctuates widely even with high sampling number above 1E9. Whereas, new advanced MC algorithm combined with neural network algorithm shows very fast convergence of Z score even with small sampling of 20k as shown in Fig.8(b), which speeds up our yield estimation by ~10 times.

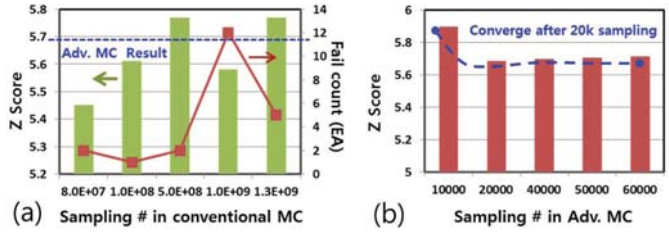

Fig.8 Z score trends depending on sampling numbers in (a) conventional MC and (b) advanced MC.

(iv) Auto layout generation and multi-objective optimization: to find optimal STC design PPAY-wise, it is important to parameterize key design knobs (i.e. contact size & position) and auto-generate the next split with this template for all STCs. There are many design knobs in 2D layout & vertical structure (X variables) and multiple optimization targets in PPAY (Y variables). Multi-objective optimization method based on machine learning algorithm is introduced to solve this problem. After initial learning with random sampling, the next split is automatically decided to get better PPY iteratively as shown in Fig.9. Our new approach could search better PP conditions, what we call Pareto front, very quickly but seamlessly without boundary. It takes only 1~2 hours (after dozens of iterations) to get an optimum design for a STC. The optimum layout de-

sign found by our iDTCO solution for 2 hours was very close to the layout optimized manually for a month. However, the quality & speed of this multi-objective optimization is strongly affected by user's domain knowledge about the process assumption & layout itself. So it is important to incorporate the expertise into our iDTCO framework.

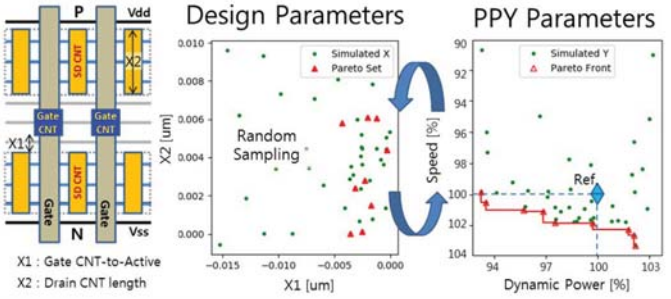

Fig.9 Schematic flow of optimizing design parameters (X) to get the optimum PPY values (Y)

3. BLOKC-LEVEL iDTCO

Block-level iDTCO consists of (i) STC characterization, (ii) synthesis with design compiler, and (iii) block-level PPA analysis, which will not be discussed in detail in this paper. The conventional focus of block-level PPA was to improve clock speed on critical timing path through holistic optimization.[6] However, with accelerated competition in dynamic power reduction on non-critical timing paths, like providing 1-fin cells in 7nm node, block-level iDTCO at path-finding stage has become super important.

Before we start block-level iDTCO, it is important to model local layout effect (LLE) [7] & self-heating effect (SHE) [8] for multiple cells of different height, driver size, and diffusion break type, which requires a large-scale stress & thermal simulation including interconnect. These LLE/SHE simulations tend to cause huge computational load. TAT issue should be solved through parallelization and domain decomposition. Scale-bridging technology connecting feature-scale TCAD to IP block-level EDA tools will be more crucial for the holistic optimization of vertical gate-all-around (GAA) devices and vertically stacked devices like monolith-3D [9] & 3D VLSI [10] in future.

4. CONCLUSION

An accurate, computationally inexpensive DTCO framework is presented. It can speeds up our daily PPY analysis by 5~10 times with good accuracy. This kind of DTCO framework powered by TCAD should keep evolving intelligently for next-generation logic path-finding. To speed up the evolution, advanced machine learning & optimization algorithms combined with domain knowledge are indispensable. The remaining challenge is how to incorporate the domain knowledge of a few experts into our iDTCO framework.

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