DTCO and TCAD for a 12 Layer-EUV Ultra-Scaled Surrounding Gate Transistor 6T-SRAM

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***Abstract*— A flow, module steps and key structural elements enabling a surrounding gate transistor (SGT) based 6T-SRAM with 50nm pillar pitch and 0.0205 um2 are presented, with emphasis on process challenges and innovations. A new DTCO/TCAD methodology is used to explore the design space, demonstrate the bit cell functionality and optimize the process. In particular, it is shown that vertical SGT are extremely sensitive to gate misalignment and that buried bottom contact makes the process immune to doping variations and misalignments.**

Keywords—Vertical nanowires, 6T-SRAM, process modules, static noise margin, DTCO, TCAD

I. Introduction

SGT [1] is a vertical Gate-All-Around (GAA) transistor architecture that carries historical significance to make a universal Si technology platform possible, including DRAM [2], NAND flash [3], and SRAM [4]. Recently, some of the authors have undertaken a comprehensive benchmark to compare 6T-SRAM designs using horizontal GAAs (hGAAs) and SGTs [5]. The study showed that SGT based bit cells can reduce the area by 20-30% with respect to hGAA based bit cells. and that SGT architecture also outperforms hGAA in term of operating voltage and standby leakage.

In this paper, we present some of the process modules necessary to successfully design and fabricate the SGT based 6T-SRAM cell. Our goal is to achieve the completion of the demonstration unit to validate a full SGT 6T-SRAM with 45nm to 50nm pitch and unit cell area of 0.018445 um2 to 0.0205 um2, respectively. This would lead to a 24% to 32% scaling factor with respect to the smallest design published to date (Fig.1). In order to maximize density, the bit cell is designed with SGT ratio of 1:1:1 for PU:PD:PG, where PU, PD, PG are the pull-up, pull-down, and pass-gate transistors, respectively.

A schematic of the bit cell is shown in Fig.2(a) along with the design guide lines Fig.2(b). The read static noise margin (RSNM) will be used as the SRAM figure of merit. RSNM is extracted from the butterfly curve (Fig.2(c)) [6].

II. Key process steps and innovations

The key fabrication steps for SGT SRAM device are shown in Fig.3. The most critical front-end-of-line (FEOL) processing of SGT SRAM cell includes, sequentially: 1) well formation, 2) nanowire [NW] pillar formation, 3) bottom S/D formation, 4) gate stack formation, 5) bottom to gate and cross couple contact formation, 6) top S/D formation, followed by middle end of line (MEOL) local interconnect and an advanced back end of line (BEOL) metallization processes exploiting super via contact process [7]. The entire process has 16 critical lithography mask layers, 12 of which are EUV layers in order to provide the designers more freedom and ease to achieve high density design. (Fig.4).

For the gate stack, single gate mid-gap workfunction (WF) has been used in order to fit in the reduced allowed space of 5nm node technology. Mid-gap WF is achieved through 5nm TiN/W gate stack. Moreover, our TCAD study demonstrates that mid-gap WF constitutes the optimal tradeoff between Read SNM (RSNM) and write SNM (WSNM) (Fig.5).

With a single mid-gap WF in mind, a complex yet widely adapted dummy gate first then last Replacement Metal Gate (RMG) process in SGT SRAM fabrication is not beneficial as almost all the high temperature thermal budget necessary to form the junctions, and detrimental to high-k/metal gate(HK/MG) performance, is applied before the gate formation. Furthermore, lower temperature top S/D epi processes were adapted not only to maintain bottom junction profile but also to maintain the HK/MG integrity intact. Therefore, we opt for a more elegant and simpler direct W gate etch with a single mid-gap work function metal TiN underneath the W gap-fill metal (Fig.6).

III. Implementation challenges

A. Design

The layout view of a high-density SRAM bitcell designed with SGTs is shown in Fig.7(a). The bitcell area is represented by the product of the cell width and cell height. The cell width is limited by the contacted gate pitch, which directly influences the metal gate dielectric and work-function (EXT_{GATE}), NW diameter (CD_{NW}), and gate spacing (SP_{GATE}). At the same time, the cell height is controlled further by the cross-couple contacts (CD_{XC}), wordline contacts (CD_{V0G}), gate extension and tip-to-tip (T2T) spacing between metal and contacts ($T2T_{GATE\text{-}XC}$,$T2T_{GATE\text{-}V0G}$) as in (1).

$$Cell\ Width = 2\ (CD_{NW} + 2\ EXT_{GATE} + SP_{GATE})$$

$$Cell\ Height = 3\ CD_{Pillar} + 6\ EXT_{GATE} + 2\ CD_{XC} + 4\ T2T_{GATE-XC} + CD_{V0G} + 2\ T2T_{GATE-V0G} \quad (1)$$

By using relaxed N7 design rules (TABLE I), we could achieve the bitcell area of the a N5 technology node.

TABLE I. DESIGN RULES

	N14	*N10*	*N7*	***This work***
Poly Pitch (nm)	*90*	*66*	*54*	*50*
Min Metal Pitch(nm)	*64*	*44*	*40*	*50*

B. Implementation into silicon

To help implement SGT SRAM design into silicon in imec's 300nm clean room, we used Coventor SEMulator™ to define process assumptions (PA) in the virtual domain and Si implementation check was done at critical steps by well-known physical characterization techniques.

In the NW module, one of the key challenges is to maintain mechanical stability when NW pillar diameters become less than 10nm in size where pillar heights are higher than 100nm. To prevent NW pattern collapse from happening where aspect ratio (AR) > 10, IPA rinse at higher than room temperature was applied [8] and control of AR over a pattern collapse threshold was maintained.

SGT architecture decoupled a photolithographic-driven gate length (LG) scaling to a process-driven LG scaling, which demands a very precise vertical process control. The vertical process control remains most challenging to implement the SGT SRAM into silicon.

Fig. 7.(a)-(d) show design to silicon implementation of NWIRE and BC module comparing against the intended SEMulator™ PA outputs.

IV. SIMULATION METHODOLOGY

3D classical TCAD on a 6-transistor structure is extremely challenging and time consuming. We have adopted a new DTCO methodology that drastically reduces the simulation time, as illustrated in Fig 8(a)&(b). Once the design space boundaries - in this case the bottom connection (BC) doping and supply voltage Vdd - have been established from the simplified DTCO structure (Fig.8(c)), a classical TCAD generated structure (Fig.8(d)) is used to determine the implant conditions and thermal steps needed for silicon implementation.

A. DTCO path finding

As shown in Fig.9, a simplified geometry based process flow, excluding implants and thermal steps, is reproduced with Synopsys Process Explorer. Afterwards, constant dopings are set with Sentaurus-Process (Fig.8(c)). From this simplified setup, the minimum doping for the P+ and NEpi regions are extracted (Fig.10). Those two areas constitute the bit cell BC, critical paths whose resistance must be kept low in order to guarantee the good functionality of the device. The optimum Vdd with respect to RSNM/Vdd is also extracted as shown on Fig.11.

In order to validate our methodology, RSNM extracted from the DTCO simulation is compared to RSNM extracted with TCAD on Fig.2(c), demonstrating that our fast DTCO produces a fairly good first order RSNM estimate.

B. TCAD optimization

To help implement SGT SRAM design into Si, TCAD must be able to answer how to achieve the doping conditions predicted by DTCO. Therefore the DTCO flow is transferred to Sentaurus-Process and augmented with implants and diffusion steps to obtain variations of the structure shown on Fig.8(d). To validate the procedure, boron and phosphorus profile comparisons between SIMS and simulation are shown on Fig. 12, with very good agreement.

At the transistor level, the most critical process step is the gate alignment since, unlike planar technology, vertical process doesn't guarantee gate to S/D self-alignment. Fig.13(a) shows that 10nm gate misalignment underlap can degrade transistor on-current (Ion) by 50%. Gate overlap also leads to 25% variation in Ion (Fig.13(b)) as well as gate capacitance fluctuations (not shown).

At the bit cell level, BC is the most critical step of the design. Proper doping of the BC n & p regions is necessary to keep series resistance low and achieve high RSNM, but is not sufficient. If the BC is connected to the SGT drain with a flat contact (Fig 14(a)), any misalignment or doping variation in the P+ and N+ areas can lead to large RSNM fluctuations. Burying the contact (Fig. 14(b)) allows to eliminate those fluctuations as illustrated in Fig 14(c) for boron dose variation in the BC P+ area.

Finally, Fig. 15 shows that projected RSNM benchmark for the SGT 6TSRAM is comparable to state-of-art MOS technologies.

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CONCLUSIONS

The key modules for the simulation of an ultra-scaled SGT 6T-SRAM were presented. A novel, time effective, DTCO method was chosen to demonstrate the bit cell functionality. Finally, TCAD was used to optimize the cell design and shows that buried bottom contacts lead to a process robust to variations.

REFERENCES

[1] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, "High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs", Technical Digest., International Electron Devices Meeting, pp. 222–225, 1988.

[2] K. Sunouchi *et al*., "A surrounding gate transistor (SGT) cell for 64/256 Mbit DRAMs", International Technical Digest on Electron Devices Meeting, pp.23–26, 1989.

[3] T. Endoh *et al*., "Novel ultrahigh-density flash memory with a stacked-surrounding gate transistor (S-SGT) structured cell", IEEE Transactions on Electron Devices , vol. 50, no 4, pp. 945–951, 2003

[4] T. Kikuchi *et al*., "A new vertically stacked poly-Si MOSFET for 533 MHz high speed 64Mbit SRAM", IEDM Tech. Dig., pp.923—926, 2004.

[5] T. H. Bao *et al*., "A Comprehensive Benchmark and Optimization of 5nm Lateral and Vertical GAA 6T-SRAMs", ESSDERC Tech. Dig. 2014, 102.

[6] FJ List, "The static noise margin of SRAM cells", Solid-State Circuits Conference, 1986. ESSCIRC'86, 1986.

[7] A. A. Gupta et. Al. Microelectronics Engineering (in press) •

[8] G. Kim et al., "Effect of Drying Liquid on Stiction of High Aspect Ratio Structures", Solid State Phenomena, Vol. 187, pp 75-78, 2012

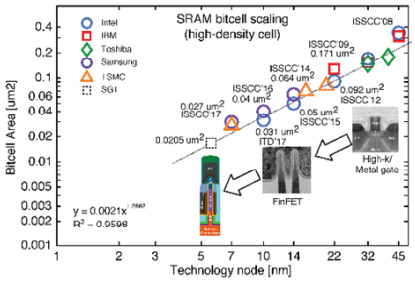
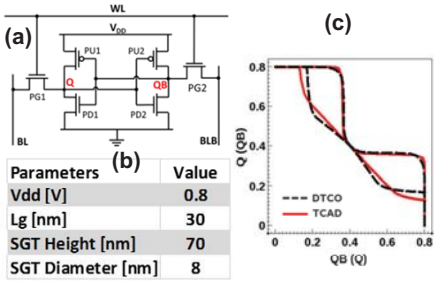


Fig. 1. SRAM area projection



Parameters	Value
Vdd [V]	0.8
Lg [nm]	30
SGT Height [nm]	70
SGT Diameter [nm]	8

Fig.2. (a) bit cell schematics;(b) Design Guide; (c) butterfly curve and SNN

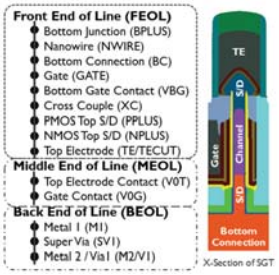


Fig. 3. SGT SRAM building blocks

FEOL Layers			
Layer	Description	Pitch(nm)	Wavelength
BPLUS	Bottom Junction	205	193i ArF
NWIRE	Nano-Wire Pillar	50	EUV
BC	Bottom Connection	50	EUV
GATE	Gate Electrode	50	EUV
VBG	Via to BC to Gate	54	EUV
XC	X-Couple	70	EUV
NPLUS	NMOS Top S/D	205	193i ArF
PPLUS	PMOS Top S/D	205	193i ArF
TE	Top Electrode	70	EUV
TECUT	Top Electrode Cut	100	193i ArF

(a)

MEOL Layers			
Layer	Description	Pitch(nm)	Wavelength
V0G	Via to Gate	60	EUV
V0T	Via to Top Electrode	60	EUV

(b)

BEOL Layers			
Layer	Description	Pitch(nm)	Wavelength
M1	Metal 1	42	EUV
V1	Via 1	60	EUV
SV1	Super Via1	56	EUV
M2	Metal 2	42	EUV

(c)

Fig. 4. Key Masks, Nominal Pitch, and Wavelength (a) FEOL (b) MEOL (c) BEOL

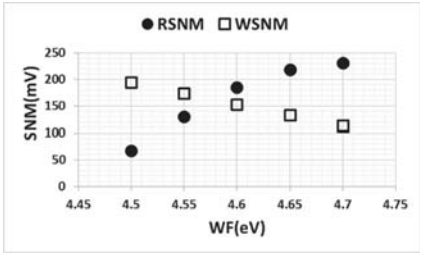


Fig. 5. RSNM & WSNM vs WF variations

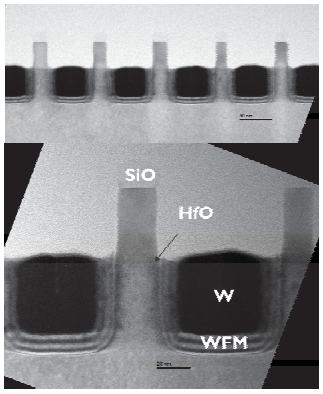


Fig. 6. Gate W / W filled metal Etch Back

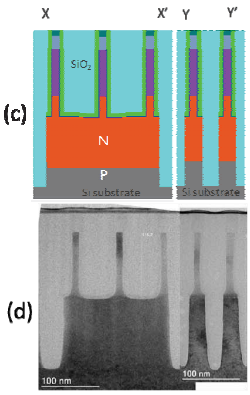


Fig. 7. Design & Implementation showing NWIRE, BC Layers; (a) SRAM unit cell layout and plain View of NWIRE (b) NIWRE dimension (c) SEMulator™ intended NIWRE/BC module PA (d) TEM confirmation of SEMulator™ PA

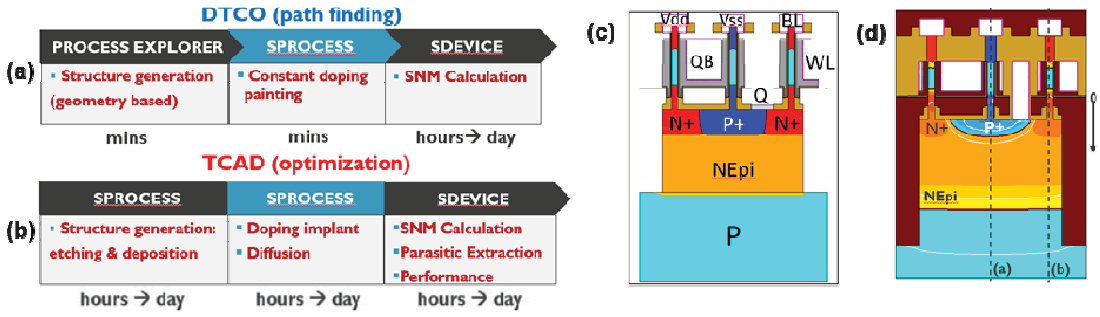


Fig.8. (a) DTCO flow; (b) TCAD flow;.(c) DTCO SRAM cross section; (d) TCAD SRAM cross section

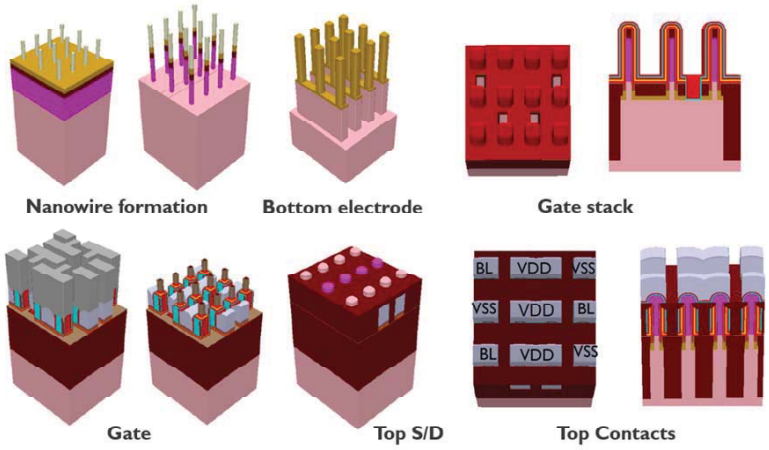


Fig.9. Sentaurus Process Explorer flow following closely the actual flow detailed in Fig.3.

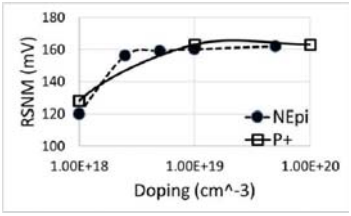


Fig.10. RSNM vs P+ & NEpi doping

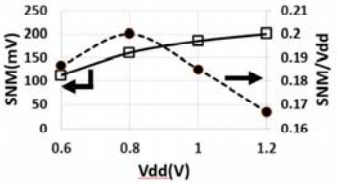


Fig.11. RSNM vs Vdd

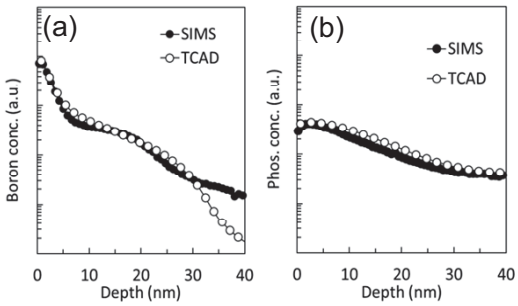


Fig.12 – Comparison between SIMS and TCAD B et P profiles along the cutlines (a) and (b) of Fig.8(d), respectively.

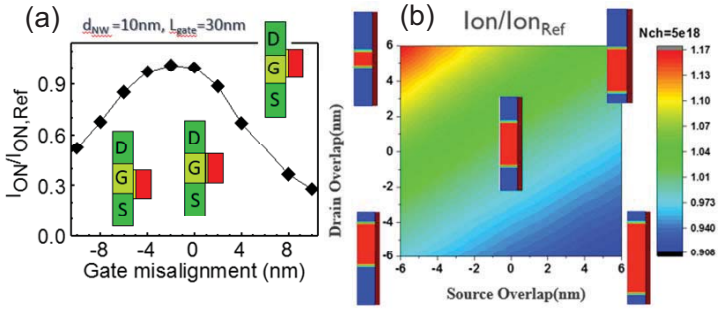


Fig.13. Impact of gate misalignment on on-current; (a) gate underlap; (b) gate overlap.

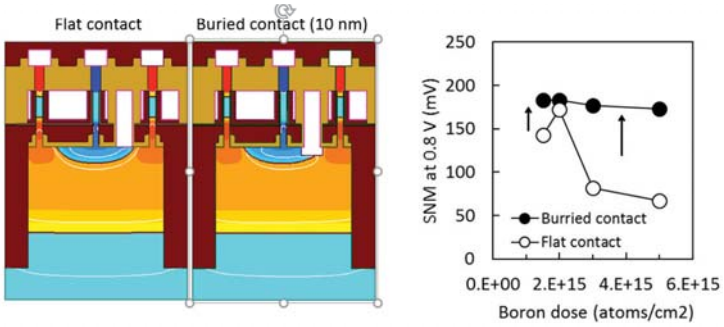


Fig.14. Flat (a) vs buried contact (b) structure. Impact of buried contact on RSNM for B dose variation in the P+ region (c). The high fluctuations occurring with the flat contact are suppressed with buried contact.

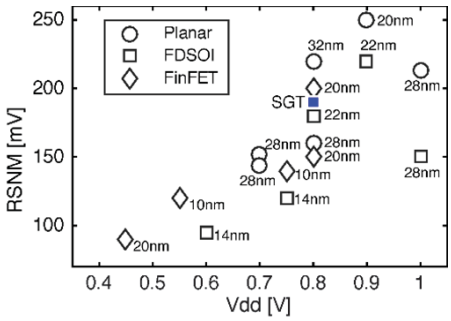


Fig.15. RSNM benchmark