Optimization of RF-22nm FDSOI Figures of Merit with 3D TCAD simulation

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***Abstract*— The aim of this study is to illustrate the efficiency of TCAD for simulating RF devices in advanced technology nodes and identify optimization paths. A strategy involving 3D simulation and a multilayered description of the resistive gate is proposed, followed by a calibration step of the TCAD setup against measurements. Then, various effects impacting the values of the *Ft*/*Fmax* RF figures of merit are assessed. At last, thanks to combination of TCAD with Design of Experiments, the sensitivity analysis of the most influent process parameters as well as their interactions is performed.**

***Keywords*— TCAD; FDSOI; RF; cutoff frequency; maximum oscillation frequency; gate resistance**

I. Introduction

This paper proposes a strategy for optimizing RF-FDSOI with 22nm design rules, an efficient solution for Mobile, IoT and RF applications thanks to its power and speed performances. The RF figures of merit (FoM) [cutoff frequency (*Ft*) and maximum frequency for power gain (*Fmax*)] are very sensitive to the parasitic capacitances and resistances in particular to the gate resistance (*Rgate*). Although *Ft* can be correctly predicted using 2D TCAD, the accurate prediction of *Fmax* requires 3D TCAD for a rigorous modelling of the parasitics [1].

II. Simulation Framework and Modelling Assumptions

A. Process simulation

This study was based on the recently published 22FDX technology from GLOBALFOUNDRIES (see [2] for process and device details). The NFET-FDSOI device was first simulated using 2D calibrated process simulation and was then extruded to 3D according to the layout taking contact-vias into account for accurate extrinsic parasitics modelling (Fig. 1). The gate is connected with one via located at each end of the finger. For the sake of sparing computation time only half a finger was simulated, assuming that the predictions of the FoMs remain identical to the case of a whole finger with the same Wf and a gate contact at both ends of the finger. The validity of this assumption was verified by simulation with finger widths in the range [0.3µm-2µm] for DC and AC FoMs, indicating that the parasitics contribution due to the overlap of the gate stack over the peripheral insulation was negligible for this device.

The global resistance of a high-K metal gate is classically described as a complex network of resistances accounting for 3D conductivity through the materials and interfaces [4]. Particular attention must be paid to the interface between the gate metal (TiN) and the doped amorphous silicon (a-Si) layer, suspected to have a major effect on *Rgate*. In this work, we propose an *Rgate* modelling framework consisting of a 2-layer n-type polysilicon with a top layer doped in the range of 10^{19}cm^{-3}, and a bottom 2 nm-thick layer accounting for the a-Si/TiN interface, whose doping acts as a tuning parameter (Fig. 2). The polysilicon layer total thickness is 18 nm. It is deposited upon a 3 nm-thick TiN layer with resistivity $2\text{x}10^{-5}$ Ω.cm and is covered with a 10 nm-thick NiSi layer with resistivity $2\text{x}10^{-6}$ Ω.cm.

B. Device simulation and extraction of the FoMs

The device simulations are performed involving the physical models usually required for FDSOI (quantum confinement and mobility model dedicated to thin layers). A 70 Ω series

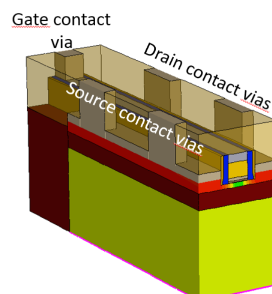

Fig. 1 3D picture of half a finger of the device. All materials are simulated up to metal-1.

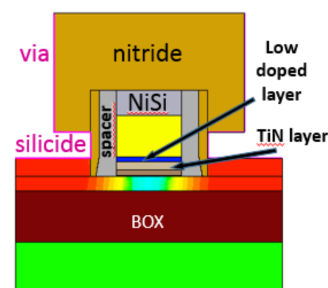

Fig. 2 Transverse cut of the device in the middle across vias, showing the interfacial poly-Si layer at the TiN interface.

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resistance is attached at each via and the silicide specific resistance at the silicon surface is 10^{-8} Ω.cm².

After small-signal device simulations in the frequency range [0.1-1000]GHz, the FoMs are extracted with the same procedures for both TCAD and experimental devices: *Ft* and *Fmax* are extracted from the extrapolation of current gain (H21) and Masons's unilateral gain, and *Rgate* is calculated from Y-parameters, at Vd=Vg=0.8V, Vs=Vb=0V at a 10GHz frequency by the expression [4]:

$$Rgate = \left|\frac{\mathrm{Re(Y12)}}{\mathrm{Im(Y11)\ .\ Im(Y12)}}\right| \qquad (1)$$

Though Vd should be 0V for a more accurate extraction, it was verified that the extraction of *Rgate* at saturation voltage gives close values and identical variations in the conditions of the present work.

Other characteristics like transconductance and capacitances useful for understanding the evolution of the RF FoMs were also extracted in saturation conditions from Y-parameters.

III. Results and Discussion

The 3D simulation of the gate stack is mandatory to take into account the series resistances within the gate and the capacitive coupling between the gate and the surrounding conductors, not only in a vertical plane across the finger. Preliminary simulations with a uniformly doped polysilicon in the gate within the appropriate range (around 10^{19} cm^{-3}) showed a gap to *Fmax/Rgate* which was impossible to bridge: Indeed, although a uniform polysilicon doping of 5×10^{16} cm^{-3} allowed fitting *Fmax*, such a low doping value was not only unrealistic but also resulted in a 3 kΩ/µm *Rgate*, much higher that experimentally measured. Thus, the experimental knowledge of the structure of the polysilicon lead to the choice of a multilayered modeling of the polysilicon. The calibration of the resistivity of the interfacial low-doped polysilicon is detailed in part A. Then, the validation of the modelling assumption is done in part B by comparison with experimental measurements made on two process splits of the 22FDX device. With the calibrated TCAD it is possible to study individual effects of process variants on the FoMs. In part C, D and E respectively, the effects of parameters having possibly an influence on the FoMs are considered: Effects of varying Contact-Poly-Pitch (CPP), polysilicon height and spacer permittivity are addressed. Finally in part F, the interest of using a Design of Experiments (DoE) strategy is presented, giving the ranking of the process parameters according to the magnitude of their effect on the FoMs and their potential interactions.

A. Effect of TiN/poly-silicon interface resistance on the FoMs

Several doping values of the polysilicon interfacial layer in the range 10^{14}-10^{19} cm^{-3} were simulated to assess the dependence of the FoMs on the gate resistance, in the case of a 1µm gate width (Wf). Fig. 3 shows that *Rgate* decreases while *Fmax* increases when the doping of the interfacial layer rises, up to the values predicted for a weakly resistive interface. On the other hand, *Ft* remains insensitive to the modification of the gate resistance. Analytical expressions of *Ft* and *Fmax* are useful to

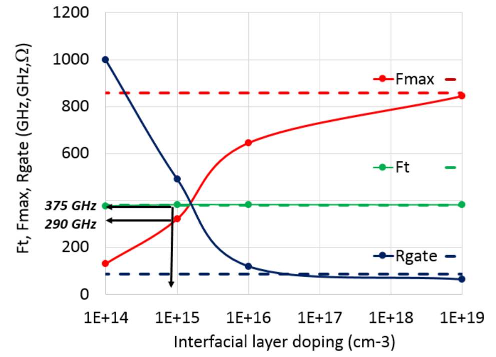

Fig. 3 Dependence of FoMs on the doping of the interfacial poly-Si. A doping ~$10^{15}$$cm^{-3}$ allows fitting the experiments. Dotted lines give the limit value of each FoM, for a weakly resistive interface.

interpret the variations of the FoMs. We chose the following expressions from [5], with *gm* the transconductance, and *Cgs* and *Cgd* the gate-to-source and gate-to-drain capacitances respectively.

$$Ft = \frac{gm}{2\pi\,(Cgs+Cgd)} \qquad (2)$$

$$Fmax = \frac{1}{4\pi}\sqrt{\frac{2\pi\,Ft}{Rgate\times Cgd}} \qquad (3)$$

In the same way as TCAD, these expressions illustrate the independence of *Ft* on interface resistance and the relative evolutions of *Fmax* and *Rgate*.

The graph in Fig. 3 allows the identification of the calibrated doping value (~10^{15} cm^{-3}) for which the simulation predicts the experimental FoM values [2] (*Ft*/*Fmax*=375/290 GHz).

B. Validation of the simulation prediction with experimental measurements

Fig. 4-6 show the fair agreement between TCAD and two sets of measurements, in predicting the evolution of FoMs vs. finger width. In order to compare TCAD with measurements made on lots with different process variants, the values are normalized to their values at Wf=1µm.The comparison shows that *Ft* remains independent of the finger width above 0.5µm. Below, one observes a decrease of *Ft* also predicted by the simulation. Such

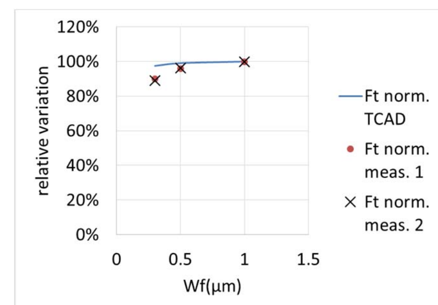

Fig. 4 *Ft* vs. finger width; comparison with measurements

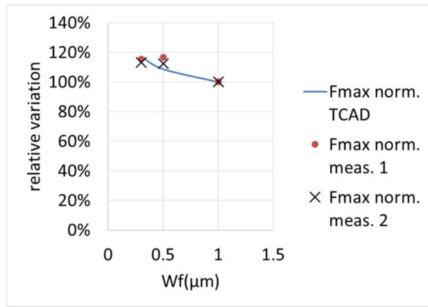

Fig. 5 *Fmax* vs. finger width comparison with measurements

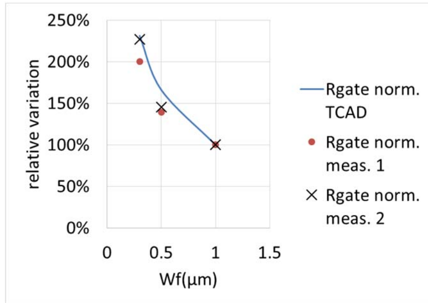

Fig. 6 *Rgate* vs. finger width comparison with measurements

a decrease is a real 3D effect which could not be obtained from 2D simulation with a lumped gate resistance. The 1/Wf decrease of *Rgate* suggests that the vertical component of *Rgate* is dominant in the range 0.3-1µm, see eq. (2) in [3]. The improvement of *Fmax* for shorter width seems contradictory with the concomitant increase of *Rgate*. However, referring to the analytical expression of *Fmax* in equation (3), it can be seen that the increase of *Rgate* could be compensated by a decrease of *Cgd*. In fact, the decrease of *Rgate* x *Cgd* for shorter finger widths was verified in the simulations.

C. *CPP effect on FoMs versus finger width*

Modifying the contact-poly-pitch (CPP) (Fig. 7-8) has an influence on *Ft* which is improved by 27 GHz thanks to a lower series resistance which increases the dynamic transconductance *gm*, see equation (2). Indeed, the source and drain series resistances are reduced because of the larger contact surface at the interface silicon/silicide. The values of capacitances *Cgs* and *Cgd* remained almost unchanged and no effect is predicted on *Rgate*. Finally, according to equation (3), the improvement of *Fmax* due to CPP at larger finger widths is explained by the *Ft*

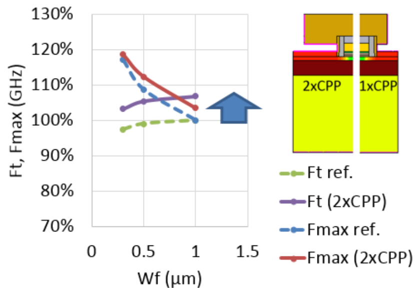

Fig. 7 Effect of CPP on *Ft*/*Fmax* vs. finger width, showing an improvement when CPP increases

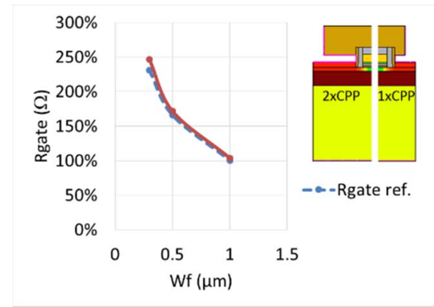

Fig. 8 No effect of CPP on *Rgate* vs. finger width

increase. It can be observed that the gain in *Fmax* is lost at shorter finger width, due to the increase of *Rgate*.

D. *Polysilicon height effect on FoMs versus finger width*

When decreasing the polysilicon-height (Fig. 9-10), *Rgate* remains unchanged because its value is essentially fixed by the resistance of the interfacial layer as mentioned before. On the other hand, the simulation predicts that *Cgd* and *Cgs* are lowered by the modification of the polysilicon height. Thus, following equation (3), the improvement of *Fmax* is explained by a higher *Ft* due to a lower gate total capacitance resulting of a smaller lateral surface of polysilicon.

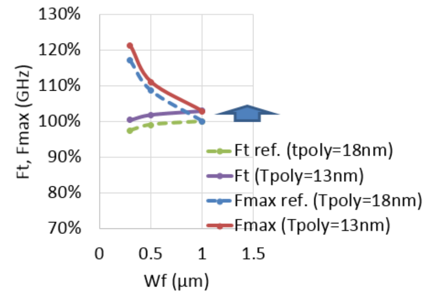

Fig. 9 Effect of polysilicon height on *Ft/Fmax* vs. finger width

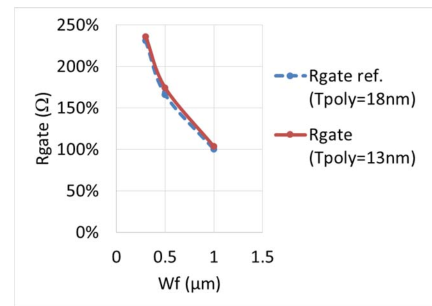

Fig. 10 No effect of polysilicon height on *Rgate* vs. finger width

E. *Spacer permittivity effect on FoMs versus finger width*

When lowering the permittivity of the spacers, simulation shows a clear lowering of the parasitic capacitances *Cgs* and *Cgd*. Accordingly, a 17 GHz gain in *Ft* and *Fmax* is predicted with no impact on *Rgate* as expected (Fig. 11-12).

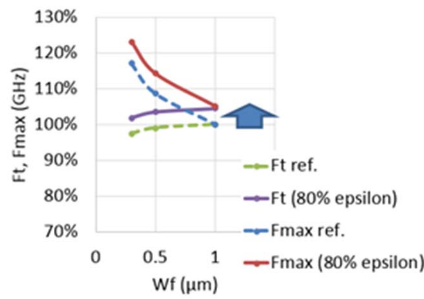

Fig. 11 Effect of spacer permittivity height on *Ft/Fmax* vs. finger width, showing an improvement at lower permittivity

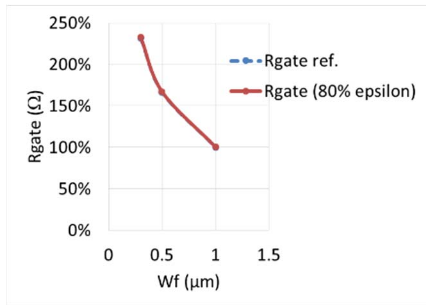

Fig. 12 No effect of spacer permittivity on *Rgate* vs. finger width

F. *Sensitivity analysis*

Designs of Experiments (DoE) coupled with TCAD allow to detect main effects but also interactions between process parameters. The Pareto graph in Fig. 13 was obtained from a DoE of 6 factors expected to have a dominant influence on the parasitics: The finger width (A), the interfacial layer doping (B), the resistivity of the silicide in the gate (C), the resistivity of the TiN (D), the spacer permittivity (E) and the series resistance (F). The Pareto graph gives the ranking of the significant effects and indicates if their increase or decrease causes the same or the reverse variation on the FoMs. The graph shows that the TiN resistivity has no significant influence on any of the FoMs, merely because the resistivity of the interfacial poly-layer is dominant. It indicates that polysilicon resistivity at TiN interface and spacer permittivity are the main limiting factors respectively for *Fmax* and *Ft*, while the effects on *Rgate* are less contrasted, with several factors and interactions being similarly influent. The dependence of *Ft* on capacitances is illustrated by the effect of parameters A (3D capacitive coupling) and E (capacitive coupling through spacers). Like for the CPP effect, the dependence of *Ft* on parameter F (series resistance) is due to a modification of *gm*. The distributed feature of the gate resistance is highlighted by the dependence on parameters A and C associated to a longitudinal resistance along the finger width, and on parameter B associated to a surface resistance as well as the significant effect of interactions AC and BC. Concerning *Fmax*, it is worth noting that the most influent parameter is B, although this parameter has a moderate impact on the other FoMs. All these observations provide objective indications for the optimization work of the FoMs.

IV. Conclusion

3D TCAD is mandatory to predict FoMs of RF-FDSOI devices because it takes into account the complexity of the gate resistance and the non-planar fringing fields at the ends of the gate finger. After calibration on an advanced FDSOI technology, the simulation proves its efficiency to identify ways of optimization.

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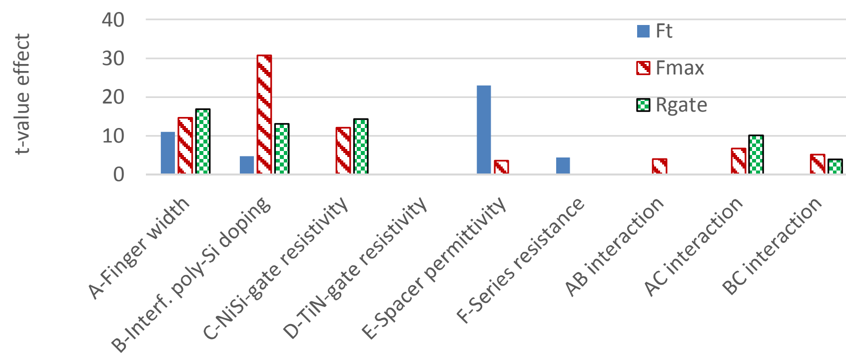

Fig.13 Pareto graphs showing the main effects impacting *Ft*, *Fmax* and *Rgate*. The higher the t-value, the more influent the parameter. These graphs give objective indications for optimizing the FoMs.