Versatile technology modeling for 22FDX platform development

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Abstract - The 22FDX platform offered by GLOBALFOUNDRIES consists of a family of differentiated products architected to enable applications across a variety of market segments such as RF & Analog, Ultra-low Power (ULP), and Ultra-low Leakage (ULL). In order to ensure the successful development of these new products, as well as to meet the time-to-market constraints, predictive Technology Computer Aided Design (TCAD) tools have been extensively used to guide development efforts, narrow the experimental conditions and reduce the number of learning cycles. The areas of impact expanded to not only predicting device outcome from process input, but also to topics traditionally not addressed by TCAD. In this paper, we present a comprehensive TCAD that has been deployed to optimize core oxide transistors, define approaches to attain ULL targets, and simultaneously investigate the AC behavior at lower operating voltages while improving RF performance. The all-encompassing co-optimization of process, device and layout has been achieved within the same platform.

I. INTRODUCTION

22FDX technology is expected to be another attractive option in the ultra-low voltage and ultra-low leakage Internet of Things (IoT) products development. It delivers 14nm FDSOI-like performance and energy-efficiency [1] at a cost comparable to 28nm planar technologies. It also provides the best path for cost-sensitive applications by offering device performance for ultra-low power consumption, software controlled transistor body-biasing for flexible trade-off between performance and power, and integrated RF. It leverages reduced system cost and back-gate feature to reduce RF power up to ~50%. It is also a suitable option for future CMOS technology because of its superior short-channel control, inherent low device variability due to undoped channel, and compatibility with the mainstream planar CMOS technology. In this work, using predictive TCAD tools, we show that a balance between spacer thickness, appropriate dopants concentration and activation anneal in combination with series resistance improvement can lead to a precise transistors overlap control and significant drive current improvement. We also present an ULL device with reduced Gate Induced Drain Leakage (GIDL) without additional process complexity and its layout dependency. Finally we discuss both AC and RF performance figures of merit (FoM) for the optimized devices.

II. 22FDX CMOS INTEGRATION

Fully Depleted Silicon-On-Insulator (FD-SOI) technology is a planar process that leverages existing manufacturing methods used in the 28nm bulk technology [2]. Besides the SOI substrates, the new Front-End process elements introduced compared to bulk include a dual SOI/SiGeOI N/P channel. The strained-SiGe channel (cSiGe) is created before STI patterning to avoid Silicon Germanium (SiGe) on insulator (SiGeOI) over-thinning linked to the Ge condensation process at active edges. A single high-k/metal gate (HK/MG) stack patterned by standard gate-first approach has been used for both NMOS and PMOS. After forming the spacers and the dual in-situ doped SiP/SiGeB N/P raised source-drain (RSD) [3], a Rapid Thermal annealing (RTA) has been performed to drive dopants from the doped-RSD towards the SOI channel to form the extension junctions. In this second generation of FD-SOI, the combination of cSiGe and SiGeB RSD provides improved pMOS drive current [4]. Device fabrication has been completed by forming silicide, contacts, and BEOL. Fig. 1 highlights the major steps of the 22FDX core transistor. A smart combination of well type (flip and conventional wells), channel (undoped/lightly doped) and back biasing enables the construction of four different transistor flavors in terms of threshold voltage (V_t) as illustrated in Fig. 2a.

III. CORE OXIDE TRANSISTOR PERFORMANCE AND TCAD DISCUSSION

TEMs of the processed and 2D-simulated NMOS and PMOS structures, with their constitutive structural elements, are respectively shown and depicted in Figs. 2b and 2c. The simulations are based on advanced TCAD work and have already been described in our previous work [5]. In particular, process simulations are based on dopant diffusion and activation models calibrated against SIMS profiles and resistivity for different RTA and dopants concentrations. Device simulations include quantum and stress effects reproducing SOI thickness and Ge content variations impact on performance similar to measurements. Such a setup accurately reproduces the measured characteristics including DC and AC results as explained in the following sections. Fig. 3 illustrates the break-up of the series resistance (R_{ON}). The importance of the contact resistance is highlighted. A major challenge [6] is the reduction of the NiSi to RSD ($R_{Silicide\ Si}$) resistance driven by the contact resistivity ρ_C. We have used Phosphorus (Ph) concentration splits ranging from 10^{20} to 10^{21} at/cm^3 to study ρ_C. Applying a recently developed

methodology [7], Fig. 4 shows that ρ_C is strongly reduced for higher Ph concentration, enabling lower R_{ON} (Fig. 5a). A similar study has been also performed for PMOS after optimization of Boron (B) concentration in the SiGeB (Fig 5b). However, for high Ph concentration ([Ph]>6x10^{20} at/cm^3), the channel resistance increases (Fig. 6a) due to a strong mobility degradation (Fig. 6b). High Ph concentration also leads to degraded overlap capacitance C_{OV} (Fig. 7). A balance between spacer thickness and RTA at optimized dopant concentration is required to enable well-overlapped devices for both NMOS and PMOS (Fig. 8). Finally, the optimized core transistors NMOS and PMOS performance are shown in Fig. 9.

IV. ULL

For mobile and IoT applications, where circuit power is dominated by static leakage, the transistor off state leakage current (I_{off}) is required to be as small as possible. The conventional method to mitigate this issue is to raise the threshold voltage of the transistor to a high value (HVT), thereby significantly reducing its subthreshold leakage current. However, when operated at high bias, such HVT transistors may show excessive GIDL due to band-to-band tunneling (BTBT) current. For NMOS, a significant GIDL reduction can be achieved using HVT transistor, length sizing and V_t re-centering (not shown here). However, in the case of PMOS transistors, GIDL still remains substantially large as the BTBT region under the spacer is unaltered. As shown in Fig. 10 and Fig. 11, PMOS GIDL reduces by increasing the spacer thickness. However, in that case the drain junction becomes underlapped degrading the transistor performance. On the other hand, a reduction of GIDL in PMOS is possible by reducing the Ge concentration in the channel. A significant I_{off} reduction in the PMOS can be then achieved by using Silicon channel (cSi) and by a combination of the back bias, gate length sizing and counter doping (Fig. 12).

V. ULP

In this section, AC performance is presented going towards ULP applications. First using the 2D DC simulation (Fig. 11) calibrated on VDD=0.8V, we ensure a good prediction of the TCAD at different VDD (Fig. 13) for NMOS and PMOS structures, which are used for Ring Oscillator (RO) simulation. Mixed-mode simulation framework has been then set up for quantitative AC performance evaluation of various technology options early in the technology development cycle. These mixed-mode simulations were run for 7-stage RO circuit in both active and quiescent modes and subsequent calculation of its delay (d) was completed. Fig. 14 shows the output voltage and the dynamic current of the simulated RO over time for different VDD. A clear change in delay and power consumption is present. In addition to the switching frequency, the current drawn from the RO power supply during its active (IDDA) and quiescent modes (IDDQ) is used to calculate the effective switching capacitances, as C_{eff} = *2d(IDDA-IDDQ)/VDD*. To extract the loading capacitances, the layout (Fig. 15) was loaded in a 3D emulation tool, where we implement the full process flow for virtual fabrication of the product (Fig. 16), and then interfaced with Parasitic Extraction (PEX) tool. The availability of the external parasitics and the intrinsic C_{OV} (C_{OV} = C_{DOV}+C_{FR}) out of the 2D simulation allows a detailed C_{eff} breakdown for further optimization of the single parasitic elements (Fig. 17). Merging the intrinsic and extrinsic parasitic components together inside a mixed-mode simulation allows direct predictions of AC performance for process changes with reasonable simulation time. Additionally, AC performance forecast has been obtained for further VDD scaling and subsequent ULP operation. Fig. 18 shows an example where AC delay for various VDD in FO3 ROs is reported for both measurements and simulations. Remarkable agreement is achieved.

VI. RF

The TCAD calibration as described in the previous section, merged with careful consideration of parasitics up to M1 allows for successful reproduction of the RF hardware (HW) data extracted from multi-finger 16x500nm test-structure (Fig. 19). Silicon data have been extracted from co-development of 22FDX RF devices, addressing IoT de-embedded S-Parameters. The C_{gd}, C_{gg}, g_m, g_{ds} and f_t are intrinsically captured by the in place TCAD methodology. In particular, accurate g_m and C_{gg} predictions have been carried out to obtain an accurate/dependable f_t simulation. *Ab-initio* simulations of the gate-stack and measurements (not shown here) were extensively used to estimate the R_{gate}, enabling a quantitative agreement to measured f_{max}. The impact of process variations on major RF parameters are hence promptly evaluated and have been summarized in Table 1. This approach helps the co-optimization along with the other flavors described above and reducing the turnaround time.

VII. CONCLUSION

The paper highlights that an advanced/versatile TACD platform and an extensive simulation support has become an essential element for advanced node technology development in order to reduce the overhead cost and learning cycle time. We showed that our extensive modeling capability has helped development of the core 22FDX with different flavors to support multiple V_ts NMOS and PMOS as well as co-development of ultra-low leakage and ultra-low power 22FDX RF devices to cater to the requirements of IoT applications.

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Fig.1. 22FDX Technology process flow at a glance.

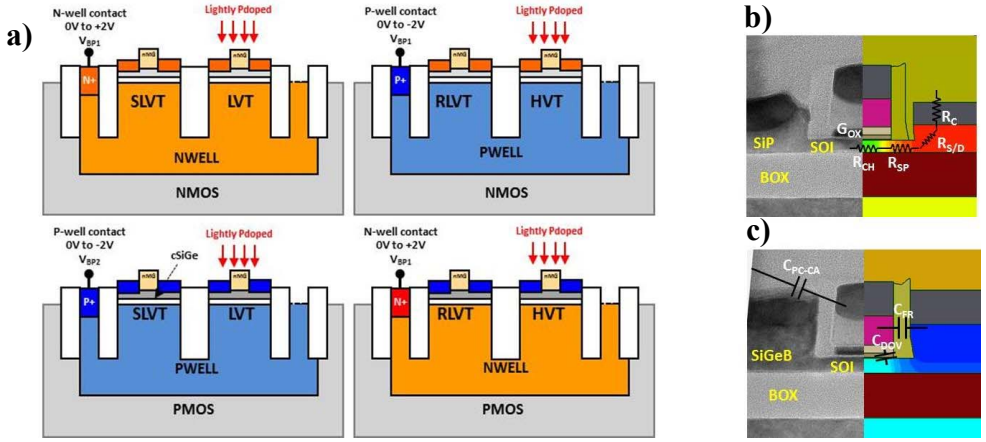


Fig. 2. (a) Schematics highlighting core oxide transistors construction for SLVT, LVT, RVT and HVT and back bias options. (b) TEM of NMOS and 2D simulated structure showing R_{ON} breakdown. $R_{ON} = R_{CH} + R_{SP} + R_{S/D} + R_C$, where the contact resistance $R_C = R_{Silicide\_Si} + R_{Contact\_Silicide}$. (c) TEM of PMOS and 2D simulated structure showing C_{DOV}, C_{FR} and C_{PC-CA}.

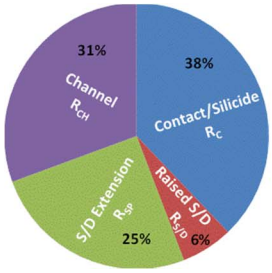


Fig. 3. R_{ON} breakdown showing the importance of R_C.

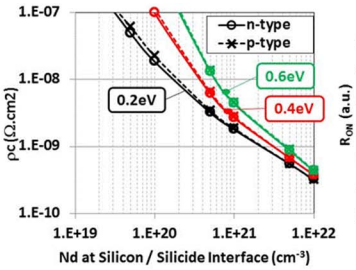


Fig. 4. Filed emission model simulating ρ_C as a function of SBH and n/p-dopant [4].

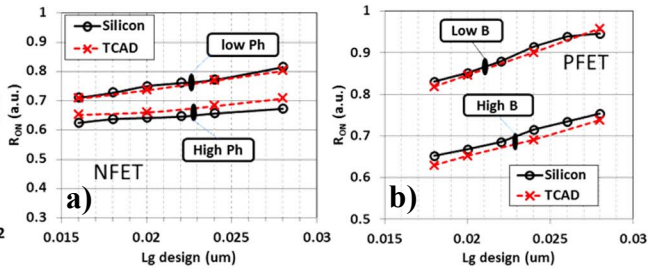
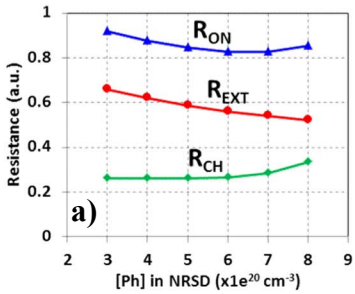


Fig. 5. Experimental data showing significant reduction in (a) NMOS and (b) PMOS series resistance by optimizing in-situ doped Ph and B concentrations.



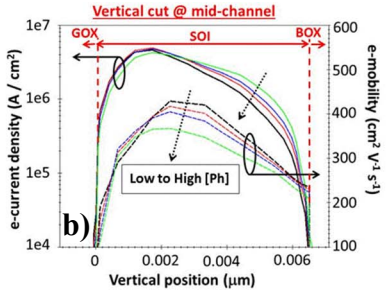


Fig. 6. Simulated R_{ON} and corresponding breakdown into $R_{ON} = R_{CH} + R_{EXT}$ (a) and electron current density and mobility (b) as a function of n-dopant concentration.

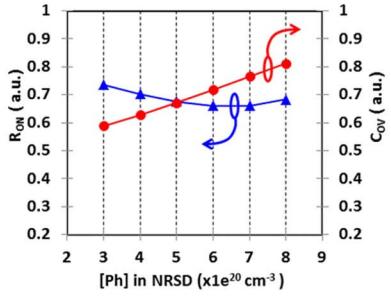
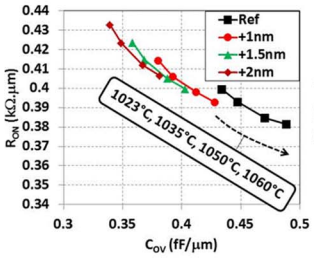


Fig. 7. Simulated R_{ON} and C_{OV} as a function of n-dopant concentration.



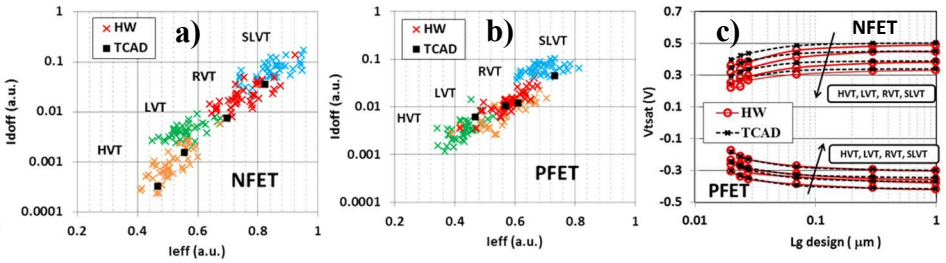


Fig. 8. Simulated R_{ON} and C_{OV} for different RTAs and spacer thicknesses (PMOS is shown for illustration).

Fig. 9. Ieff/Ioff characteristics at VDD = 0.8 V for (a) NMOS and (b) PMOS. (c) NMOS and PMOS threshold voltage under saturation conditions. TCAD reproduce fairly the measurements trend.

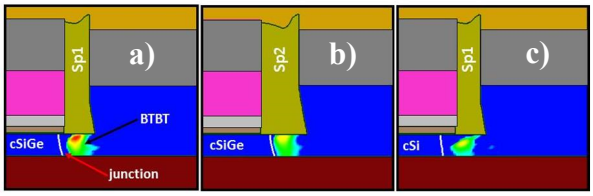


Fig. 10. BTBT profile for PMOS reference (a), thick spacer (b) and cSi (c) structures. Thick spacer and cSi show reduced BTBT.

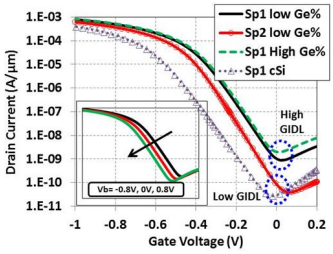


Fig. 11. Simulated PMOS (Lg=20nm design) transfer characteristics at different back biases, spacer thicknesses and channel Ge contents.

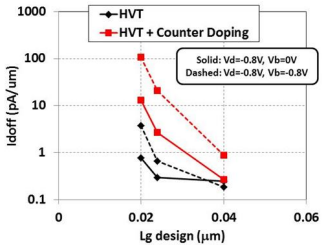


Fig. 12. PMOS Ioff optimization with Lg, Vb and channel doping. The optimized configuration is selected according to the application requirements.

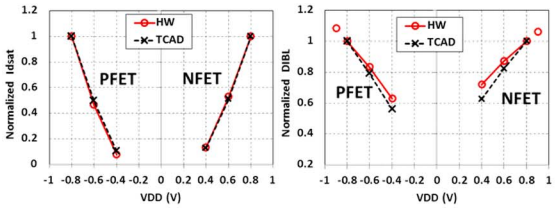


Fig. 13. NMOS and PMOS DIBL and Ion characteristics at different VDD. The TCAD projection is aligned with HW.

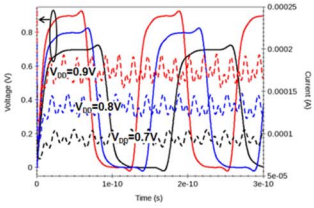


Fig 14. Transfer characteristics of the RO in active operation for different VDD.

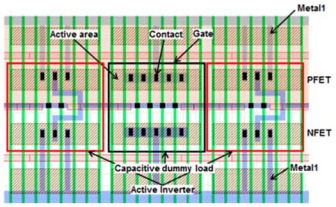


Fig. 15. Layout of the inverter stage with FO3.

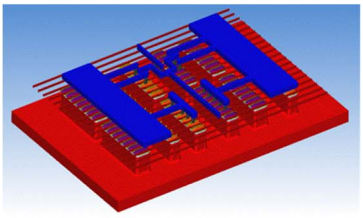


Fig 16. Process emulation of single Inverter cell and capacitive dummy load within RO.

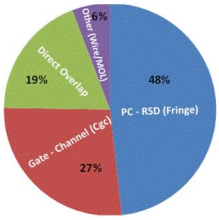


Fig. 17. RO C_{eff} breakdown where the PC-EPI fringe capacitance is the major contribution in C_{eff}..

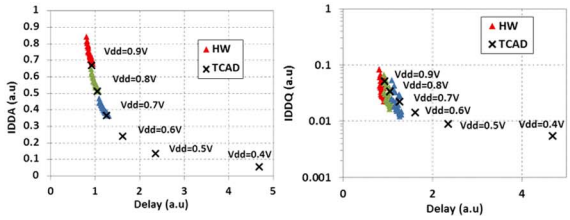


Fig. 18. IDDA and IDDQ vs. VDD. Measurements are completed for VDD 0.9V to 0.7V while TCAD covers VDD=0.9 up to 0.4V.

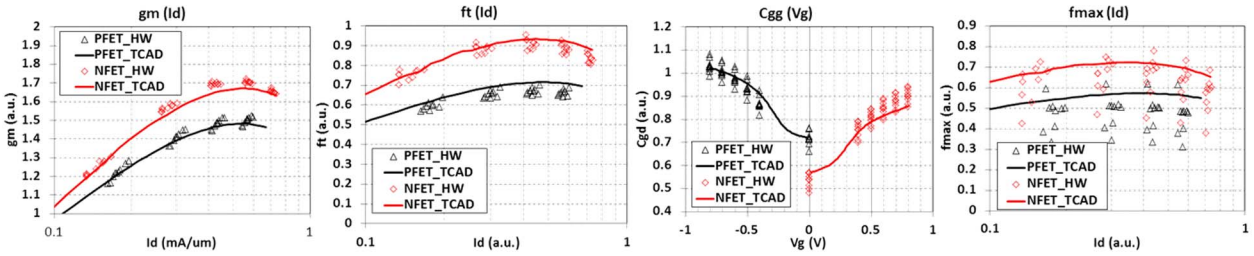


Fig. 19. Comparison between HW and TCAD of RF-relevant FoMs for N/PMOS nominal devices.

Element	Cgd	Cgg	gmsat	gds	ft	fmax*
Lg reduction	⇔	⇘⇘	⇗⇗	⇗⇗	⇗⇗	⇗
Tinv reduction	⇔	⇘	⇗	⇔	⇔	⇔
PC height	⇔	⇔	⇔	⇔	⇔	⇔
EPI Thk reduction	⇘	⇘	⇘	⇘	⇗	⇗
Spc + RTA	Adjusted at same Vt and SCE				⇔⇗	⇔⇗

Table 1. Impact of process variation on RF FoMs (Constant Rgate has been assumed).