Fast evaluation of Continuous-RX impact on performance for Strained FDSOI

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***Abstract*— UTBB-FDSOI device performance can be enhanced by stress engineering, especially thanks SiGe channel in pMOS [1]. SiGe channels induce strong local layout effects [2, 3] which are mainly due to stress relaxation during STI process [2]. In this study, we propose a TCAD simulation methodology to evaluate stress relaxation in standard active regions but also in Continuous-RX design structures. Finally, analytical model is provided to assess Continuous-RX design structure performance.**

Keywords: continuous-RX, strain engineering, TCAD, compact model, UTBB, FDSOI, SiGe.

I. INTRODUCTION

To continue the downscaling of CMOS technologies with an improvement of performance, stress engineering is used since the 90nm node [4]. For FDSOI technology, thanks to the gate electrostatic control, only pMOS channel need to be stressed to reach 20nm node required performance. It is achieved by the integration of SiGe channel and SiGe raised source and drain [1,5]. However, as already shown in [3], this integration produces strong local layout effects. To limit this loss of performance, Continuous-RX design structure has been introduced [2], but its impact on performance still need to be assessed and modeled. In this study,we developed a TCAD simulation methodology to evaluate stress relaxation in standard active regions but also in Continuous-RX design structures. Finally, analytical model is provided to assess Continuous-RX design structure performance.

II. TCAD SIMULATION METHODOLOGY FOR STRAIN RELAXATION DUE TO STI PROCESS

In CMOS technology with initially strained channel (as 14FDSOI SiGe pMOS [1]), strain relaxation in active region over 300nm from STI edge was evidenced by Nano Beam Diffraction performed just after STI process step [2]. It was mainly attributed to free boundary condition introduced during STI patterning [2, 6]. It was also demonstrated in [2] that subsequent process steps only induce a constant shift in strain meaning that strain distribution trends are preserved from STI process until the end of the front-end process [2, 6]. To reproduce such a behavior, we built a TCAD [7] deck using device layout as input, including complete process simulation [6], electrical calibration and advanced transport model for strain SiGe [7]. This study is based on 14FDSOI technology (L_g=20nm gate length, CPP=90nm and 25%SiGe channel) [1,2] but trends would be identical for comparable technologies such as 22FDX [5] or other strained MOSFET technologies such as those lying on sSOI substrates [10]. Fig.1 shows that stress distribution measured in [2] after STI process step (blue) and after raised S/D (red) are well reproduced by TCAD (dots).

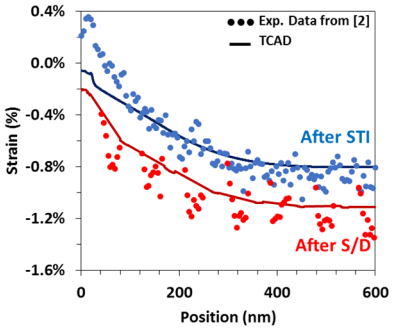


Figure 1: Strain in active region as a function of the distance with STI edge obtained by NBD measurement from [2] and simulation; blue: after STI patterning & red: after raised S/D

In real design with STI isolation (Fig.2-a), the device is not necessarily centered on the active region, then both symmetric active region (S_A=S_B=nxCPP, Fig.3-a) and dissymmetric active regions (S_A=n×CPP, S_B=m×CPP with n≠m, Fig.3-b) are considered.

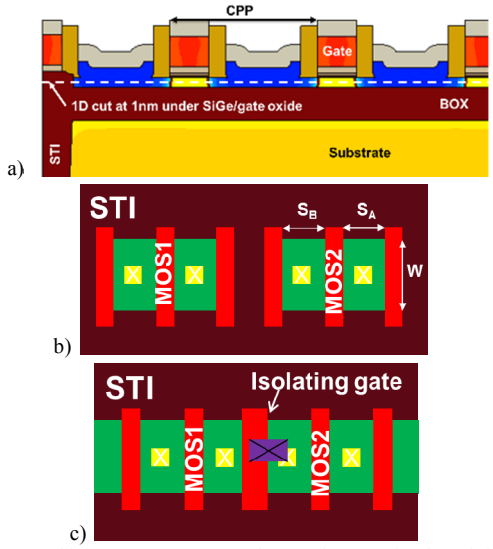
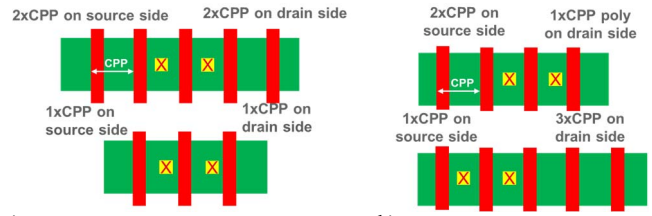


Figure 2: a) Half TCAD structure used to evaluate active length impact on performance b) classical active region c) ContinuousRX



a) b)

Figure 3: test structures schematic to evaluate impact of active length in a) Symmetric case b) dissymmetric case.

In both cases, TCAD is in a good agreement with experimental data of [2] (Fig.4). Fig.5 shows the evolution of the mean longitudinal stress under the gate obtained by TCAD after STI process simulation. It demonstrates by comparison with Fig.4 that trends of current and of mean longitudinal stress with active length are the same.

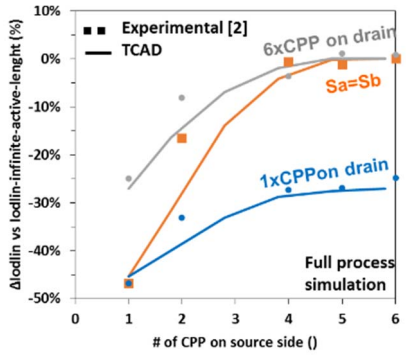


Figure 4: Variation of Iodlin (Id at Vd=50mV & Vg-Vt=500mV) normalized by infinite active length case as a function of source length in symmetric & dissymmetric cases.

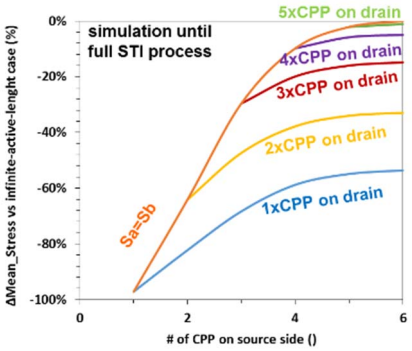


Figure 5: TCAD variation of mean longitudinal stress under the gate normalized by infinite active length case as a function of source length in symmetric & dissymmetric cases.

We plot on Fig.6 the longitudinal stress profile along a 1D cut (Fig.2-a) for several total active length $L_{act}=S_A+S_B+L_g$ just after STI process. This evidenced that, if the device is the closest to active edge, increasing L_{act} has quickly a weak impact on longitudinal stress in channel (marked by transparent red rectangle), so on performance.

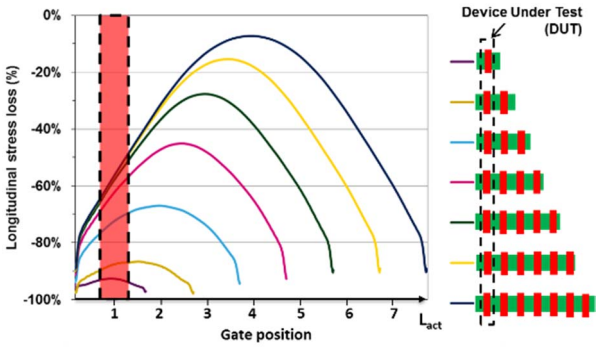


Figure 6: Longitudinal stress loss variation as a function of active length evidencing that, in dissymmetric case, the shorter side of active region is driving the performance (TCAD until full STI process).

III. CONTINUOUS-RX TCAD SIMULATIONS

To avoid the performance degradation due to stress relaxation during STI process, Continuous-RX design structure has been introduced [2]. Instead of isolating neighbor device by STI, an electrostatic isolation is performed with grounded gate enabling to each device in Continuous-RX to present large active length (Fig.2-c). However, in real design, each device doesn't present same width. So, we can expect that Continuous-RX enables to limit the loss of performance. From previous part, we know that continuous-RX structures performance can be assessed by a process simulation only until STI step. Obviously, 3D simulations are mandatory to perform such an evaluation: a 3D process simulation is built until STI and test structure layouts are defined (Fig. 7, dashed rectangle locates the DUT).

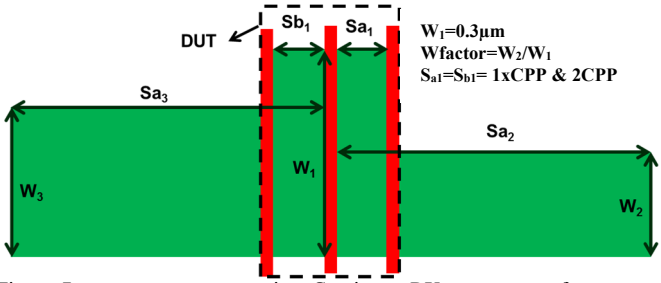
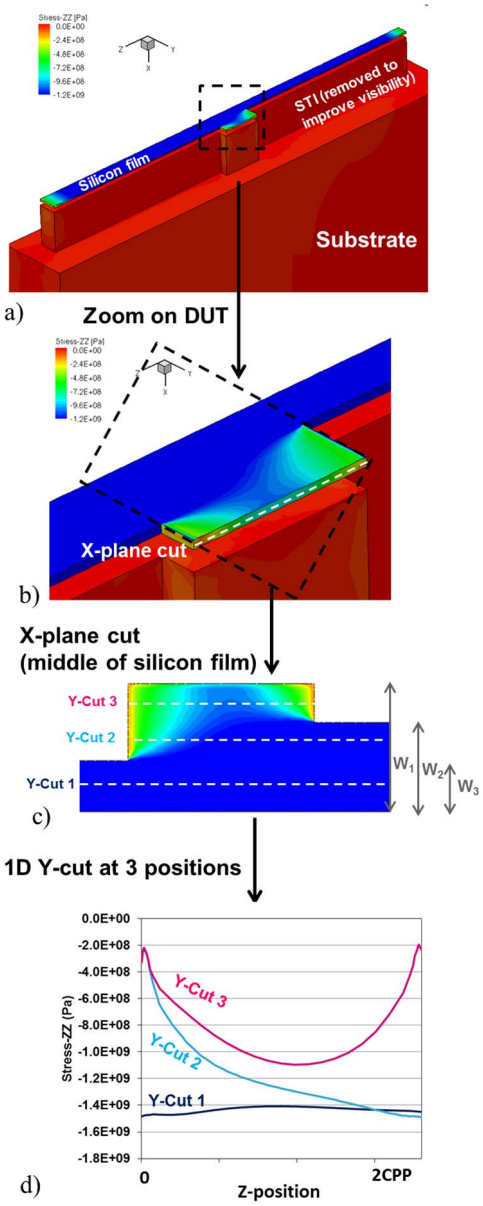


Figure 7: test structure to monitor ContinuousRX structure performance with the definition of variable parameter.

Fig. 8-a shows the mapping of longitudinal stress (stressZZ) of the full simulated structure, which have to be long enough (~2µm) to ensure "infinite" active length. Fig. 8-b shows a zoom on the DUT, Fig.8-c presents a 2D X-plane cut in the middle of silicon film and finally Fig. 8-d evidences through 1D cut on Fig.8-c 3 regions presenting identical behavior as classical active region: cut-3 is the region where active region length is "infinite" on both sides as expected, compressive longitudinal stress is not degraded by STI process. Cut-2Active length is infinite only on one side in the second region, (similar case as Fig. 6). Cut-1 represents a short active region on both sides (similar case as Fig. 4).



Note: STI removed to improve visibility

Figure 8: illustration of longitudinal stress distribution in ContinuousRX structure obtained by 3D TCAD simulation until full STI process a) full 3D structure b) zoom on DUT in 3D structure c) X-plane 2D cut in the middle of silicon film d) 1D longitdinal stress profile

To assess the impact on device performance, we evaluate the mean value of longitudinal stress in the channel (under the gate, from gate oxide to BOX) and plot on Fig.9 the loss of stress compare to infinite active region (W_2=W_3 for simplicity) for two different active length. As expected, we can see that there is still a stress relaxation with Continuous-RX design structures, but limited compare to classical active region (dashed lines). Obviously, the stress relaxation (so the loss of device performance) is higher with low Wfactor and disssymetric structures.

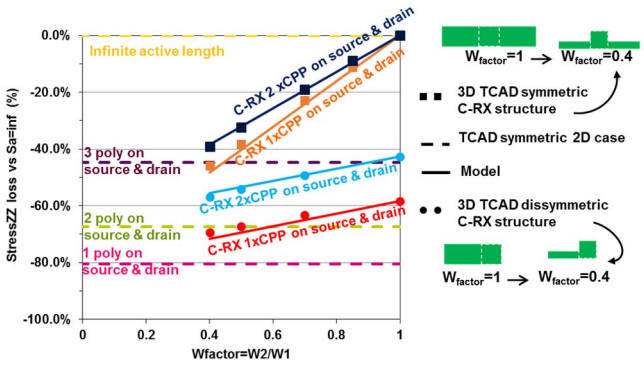


Figure 9: longitudinal stress variation vs infinite active length case (Sainf) for variation of Wfactor=W2/W1 obtained by TCAD & analytical model.

We also observe an increase of compressive longitudinal stress (so of device performance) if W2&W3>W1 thanks a corner effect (Fig.10, with symmetric structure in device width direction to enhance this effect). Finally, Fig.11 shows the stress grain brought by this structure as a function of W. Because stress improvement is due to a corner effect, stress gain is higher for shorter W.

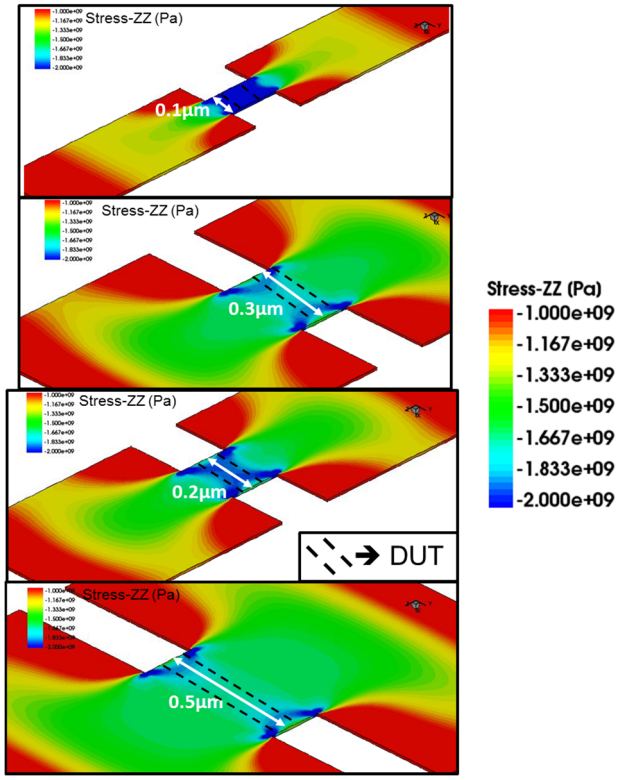


Figure 10: longitudinal stress profile obtained by 3D TCAD on Continuous-RX structure with Wfactor =2

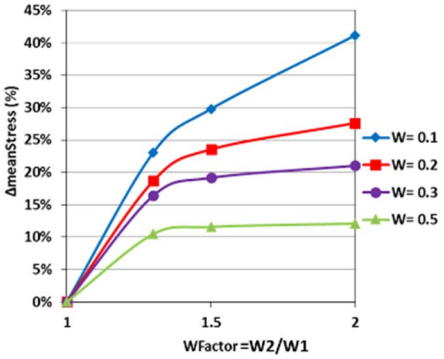


Figure 11: Longitudinal stress improvement compare to infinite active length case brought by Continuous-RX structure with Wfactor>1

IV. CONTINUOUS-RX IMPACT ON PERFORMANCE MODEL

Continuous-RX specific Local Layout Effect (LLE) need to be accounted in device model in order to be able to assess accurately the performance of every active designs. Similarly to standard active region [11, 12], stress relaxation in Continuous-RX need to be analytically evaluated, in order to be included in SPICE simulation. Previous part evidenced 3 regions in such structure which are 2D case where compressive longitudinal stress can be analytically evaluated thanks [10, 11]. Then, complete longitudinal stress in a given Continuous-RX structure, defined in Fig.8, can be evaluated as a combination of the evidenced 2D cases as:

$$\text{stress}_{CRX} = \frac{(W_1 - W_3)}{W_1}\text{stress}(Sa_1, Sb_1) + \frac{(W_3 - W_2)}{W_1}\text{stress}(Sa_1, Sa_3) + \frac{W_2}{W_1}\text{stress}(Sa_1, Sa_2) \quad \text{(Eq.1)}$$

With W_1,W_2,W_3, Sa_1, Sa_2, Sa_3, Sb_1, Sb_2 and Sa_3 defined on Fig.7 and stress(Sa,Sb) the evaluation of longitudinal compressive stress in the case of standard and rectangular active region given by [11,12]. Fig.9 shows the good agreement of our model of stress degradation for Continuous-RX design structures with TCAD simulation in the cases W_2&W_3<W_1

V. CONCLUSION

In this paper, we propose a simulation methodology to evaluate stress relaxation in SiGe channel due to STI process in classical active region and Continuous-RX structures. Note that this study was performed for longitudinal compressive stress (pMOS), but it can be also used for longitudinal tensile stress (nMOS built on sSOI substrate [10]). Longitudinal stress loss has been estimated as a function of width, length and shape of active regions. Moreover, particular Continuous-RX design structures enabling stress improvement thanks a corner effect have been evidenced. Finally, to quickly evaluate Continuous-RX design structure performance, an analytical model has been proposed.

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REFERENCES

[1] O. Weber, E. Josse, J. Mazurier, N.Degors, S. Chhun, P. Maury, S. Lagrasta, D. Barge, J.-P. Manceau and M. Haond "14nm FDSOI Upgraded Device Performance for Ultra-Low Voltage Operation," in VLSI Symp. Tech. Dig. 2015 pp 168-169.

[2] R. Berthelon, F. Andrieu, E. Josse, R. Bingert, O. Weber, E. Serret, A. Aurand, S. Delmedico, V. Farys, C. Bernicot, E. Bechet, E. Bernard, T. Poiroux, D. Rideau, P. Scheer, E. Baylac, P. Perreau, M.A. Jaud, J. Lacord, E. Petitprez, A. Pofelski, S. Ortolland, P. Sardin, D. Dutartre, A. Claverie, M. Vinet, J.C. Marin, and M. Haond. "Design / technology co-optimization of strain-induced layout effects in 14nm UTBB-FDSOI CMOS: enablement and assessment of continuous-RX designs" in VLSI Symp. Tech. Dig. 2016 pp 1-2.

[3] K. Cheng, A. Khakifirooz, N. Loubet, S. Luning, T. Nagumo, M. Vinet, Q. Liu, A. Reznicek, T. Adam, S. Naczas, P. Hashemi, J. Kuss, J. Li, H. He, L. Edge, J. Gimbert, P. Khare, Y. Zhu, Z. Zhu, A. Madan, N. Klymko, S. Holmes, T. M. Levin, A. Hubbard, R. Johnson, M. Terrizzi, S. Teehan, A. Upham, G. Pfeiffer, T. Wu, A. Inada, F. Allibert, B.-Y. Nguyen, L. Grenouillet, Y. Le Tiec, R. Wacquez, W. Kleemeier, R. Sampson, R. H. Dennard, T. H. Ning, M. Khare, G. Shahidi, and B. Doris "High Performance Extremely Thin SOI (ETSOI) Hybrid CMOS with Si Channel NFET and Strained SiGe Channel PFET" in IEDM. 2012 pp 419-422.

[4] K. Misty, M. Armstrong, C. Auth, S . Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson and M. Bohr "Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology" in VLSI 2004, pp. 50 – 51.

[5] R. Carter; J. Mazurier; L. Pirro; J-U. Sachse; P. Baars; J. Faul; C. Grass; G. Grasshoff; P. Javorka; T. Kammler; A. Preusse; S. Nielsen; T. Heller; J. Schmidt; H. Niebojewski; P-Y. Chou; E. Smith; E. Erben; C. Metze; C. Bao; Y. Andee; I. Aydin; S. Morvan; J. Bernard; E. Bourjot; T. Feudel; D. Harame; R. Nelluri; H. -J. Thees; L. M-Meskamp; J. Kluth; R. Mulfinger; M. Rashed; R. Taylor; C. Weintraub; J. Hoentschel; M. Vinet; J. Schaeffer; B. Rice "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications" in IEDM 2016 pp. 2.2.1-2.2.14.

[6] A. Idrissi-El Oudrhiri; S. Martinie; J-C. Barbé; O. Rozeau; C. Le Royer; M-A. Jaud; J. Lacord; N. Bernier; L. Grenouillet; P. Rivallin; J. Pelloux-Prayer; M. Cassé; M. Mouis, "Mechanical simulation of stress engineering solutions in highly strained p-type FDSOI MOSFETs for 14-nm node and beyond," SISPAD Tech. Dig. 2015 pp.206-209.

[7] www.synopsys.com

[8] C. Tavernier; F. G. Pereira; O. Nier; D. Rideau; F. Monsieur; G. Torrente; M. Haond; H. Jaouen; O. Noblanc; Y. M. Niquet; M-A. Jaud; F. Triozon; M. Casse; J. Lacord; J. C Barbe, "TCAD modeling challenges for 14nm FullyDepleted SOI technology performance assessment," SISPAD 2015 pp.4-7.

[9] O. Nier; D. Rideau; R. Clerc; J. C Barbé; L. Silvestri; F. Nallet; C. Tavernier; H. Jaouen "Limits and improvements of TCAD piezoresistive models in FDSOI transistors" ULIS Tech. Dig. 2013 pp.31-64.

[10] C. Fenouillet-Beranger; P. Perreau; O. Weber; I. Ben-Akkez; A. Cros; A. Bajolet; S. Haendler; P. Fonteneau; P. Gouraud; E. Richard; F. Abbate; D. Barge; D. Pellissier-Tanon; B. Dumont; F. Andrieu; J. Passieux; R. Bon; V. Barral; D. Golanski; D. Petit; N. Planes; O. Bonin; W. Schwarzenbach; T. Poiroux; O. Faynot; M. Haond; F. Boeuf "Enhancement of devices performance of hybrid FDSOI/bulk technology by using UTBOX sSOI substrates" in VLSI Tech. Dig 2012 pp. 115-116.

[11] T. Poiroux P. Scheer, O. Rozeau, B. de Salvo, A. Juge, J-C. Barbé and M. Vinet "New version of Leti-UTSOI2 featuring further improved predictability and a new stress model for FDSOI technology" MOS-AK2015, MOS-AK workshop.

[12] B. DeSalvo; P. Morin; M. Pala; G. Ghibaudo; O. Rozeau; Q. Liu; A. Pofelski; S. Martini; M. Cassé; S. Pilorget; F. Allibert; F. Chafik; T. Poiroux; P. Scheer; R. G. Southwick; D. Chanemougame; L. Grenouillet; K. Cheng; F. Andrieu; S. Barraud; S. Maitrejean; E. Augendre; H. Kothari; N. Loubet; W. Kleemeier; M. Celik; O. Faynot; M. Vinet; R. Sampson; B. Doris "A mobility enhancement strategy for sub-14nm power-efficient FDSOI technologies" IEDM 2014 pp. 7.2.1-7.2.4.