TCAD Analysis of SiGe Channel FinFET Devices

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***Abstract*— SiGe FinFET devices have many unique device elements which differ from conventional Si FinFET devices. Here we discuss their threshold voltage sensitivity, stress profiles, long channel mobility behavior, and the presence of traps at the gate oxide interface. In order to achieve a well-performing SiGe FinFET device it is important to understand the physical nature of these elements and incorporate them in a well-calibrated TCAD deck. In this paper, we examine each element with experimental data and calibrate the TCAD deck by introducing new boundary conditions, implementing a new Dit extraction method, and adjusting the material parameters. Special consideration is given to the treatment of interface traps since the readout of the trap density with the conductance method used in experiments does not represent the actual trap distribution. Finally, we review the short channel transistor performance and provide guidelines on how to achieve a high-performing device.**

I. Introduction

SiGe channel or cSiGe devices have been advocated as a promising contender for next-generation transistors due to their higher hole mobility and less disruptive process implementation [1-3]. On the other hand it is known that they have a large number of interface traps at the SiGe/oxide interface. In order to capture these characteristic physical effects it is important to create a well-calibrated TCAD deck. Our simulations include a realistic fin shape, Vth sensitivity, mechanical stress effects, and interface trap behavior. First we describe how these features are calibrated against experimental data of long-channel devices. Finally, we review the short-channel device performance.

II. Process/Stress Simulation

There are several fabrication challenges unique to the cSiGe FinFET process. It requires low temperature annealing to prevent Ge out-diffusion and it needs a special etch process to define the fin height. In addition, SiGe tends to erode more than Si during the wet cleaning/etch process. These two conditions often result in a nonconventional fin profile. In order to reproduce complex fin shapes we implemented in our TCAD deck a sophisticated numerical algorithm based on Bezier curves. Fig. 1 shows fin profiles generated from TCAD and matching TEM images.

Special consideration was given to simulating the cSiGe stress. The initial channel stress at the bottom of the fin is

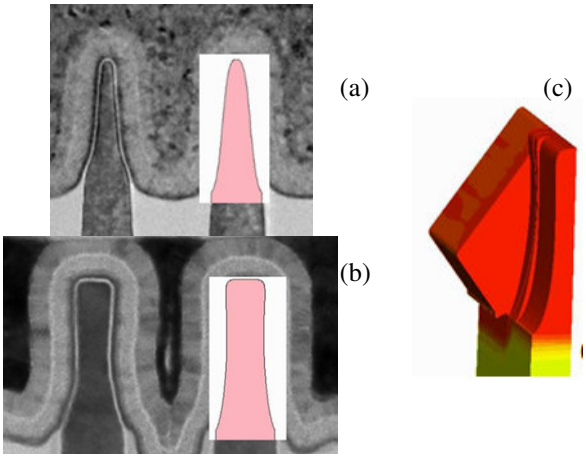

Fig. 1: Comparison between XTEM and TCAD fin profiles of (a) Si channel fin, (b) SiGe fin. In the process simulation a Bezier curve algorithm was used to describe the fin cross section. (c) TCAD 3D image of FinFET with S/D epi.

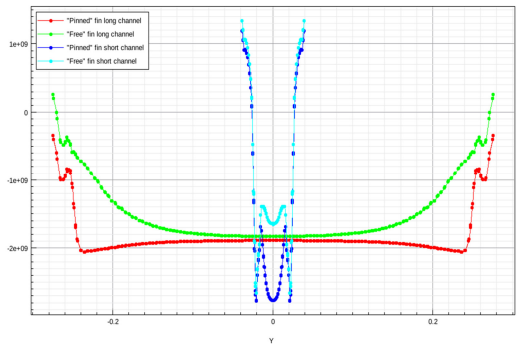

Fig. 2: LC and SC stress profiles in the middle of the fin from source to drain. Two different stress boundary conditions are compared. Note that the maximum stress is smaller in the SC device than the LC device.

generated by the lattice mismatch between the SiGe and Si materials. The fin is assumed to be infinitely long and sustain no process damage until the embedded S/D etch module. In this step, we compared two different mechanical boundary conditions (BC): a "pinned channel" case where the SiGe stress relaxation during the S/D recess etch is inhibited by the material cladding the fin; and a "free channel" case where no such pinning occurs. Fig.2 shows the stress simulation results for long-channel (LC) and short-channel (SC) devices with

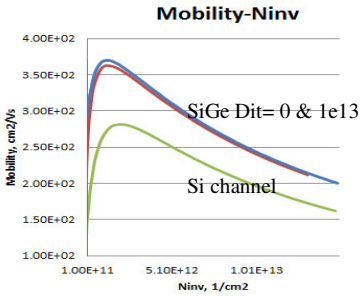

Fig. 3: LC mobility characteristics showing a 20% mobility boost of the SiGe device over the Si device. The impact of traps on mobility is small.

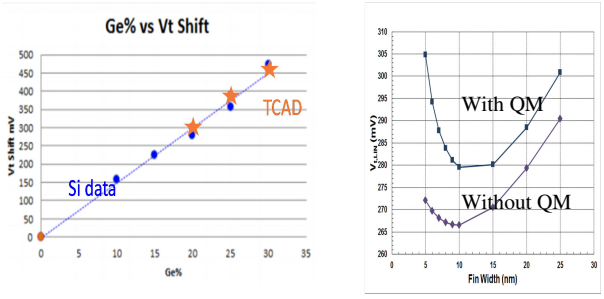

Fig. 4: (a) LC threshold voltage as a function of xGe. TCAD data (red) matches well with HW data (blue). (b) Threshold voltage vs. fin width including quantum mechanical effects. Note that QM has a significant effect on Vth for narrow-width devices.

either boundary condition. For the LC device, the maximum stress is similar for both cases because the channel center is far removed from the SD cavity. For the SC device, however, the maximum stress is significantly lower for the "free channel" case because a portion of the original SiGe fin stress relaxes during the cavity etch process.

Nano Beam Diffraction (NBD) data [1] suggests that a "free channel" is more realistic than a "pinned channel" so this boundary condition was used in all subsequent simulations shown here. In Fig. 3 we plot the LC mobility versus the inversion charge. It shows a boost of about 20% of the long channel mobility gain for the cSiGe device due to the higher stress arising from the lattice mismatch at the bottom of the fin. However, it should be noted that such a mobility boost due to the channel stress may be reduced in the short channel device because of the stress relaxation during the cavity etch mentioned earlier.

III. Device Simulation

A. *Calibration of threshold voltage*

For the device simulation we first used a 2D Schrodinger solver to calculate quantum confinement effects and then imported them into a 3D drift-diffusion device simulation. The results show that the threshold voltage level dramatically increases with decreasing fin width due to stronger confinement effects (Fig. 4(a)). Next we calibrated the dependence of the long-channel Vth with respect to the Ge concentration by modifying the bandgap narrowing model

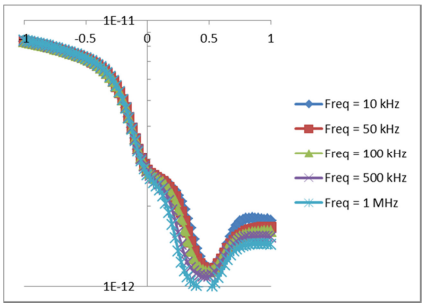

Fig. 5: CV curve from SiGe FinFET hardware showing frequency dispersion.

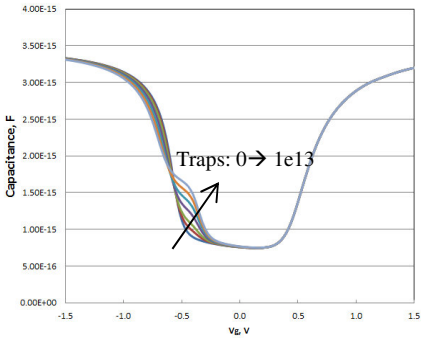

Fig. 6: TCAD results of the full CV curve for various trap densities showing an increased hump with higher trap density.

parameters. Fig. 4 (b) shows an excellent match between TCAD and hardware data.

B. *Calibration of interface traps*

Interface traps were included in the device simulation. The evidence of traps due to the SiGe channel in the real device is well observed from the frequency dispersion phenomena in the CV curve shown in Fig. 5. Note that the bias condition for this measurement, as described in Table 1, is designed to only probe the regime between depletion and inversion. For our TCAD simulation we applied a bias configuration covering all regimes.

Table. 1 Bias condition for CV measurement

	Gate	Drain	Source	Body
Inversion CV	High	Low	Low	GND
Full CV	High	Low	Low	Low

Fig. 6 shows the CV curves from TCAD simulations with various trap densities. In our simulations traps are assumed to be of donor type, i.e., positively charged when occupied and neutral when not occupied. It is apparent that the size of the hump in the CV curve becomes stronger as the trap density increases at a fixed frequency. It is also observed that the threshold voltage increases with increasing trap density, which agrees with the assumption that the traps acts as donors. There are other parameters affecting the CV behaviors such as the

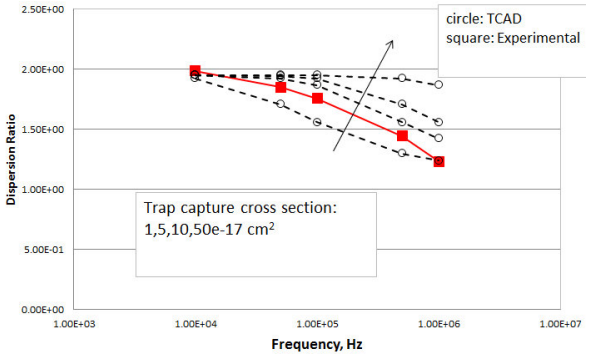

Fig. 7: Dispersion ratio for various capture cross sections. At a fixed capture area, the ratio decreases with increasing frequency indicating frequency dispersion phenomena.

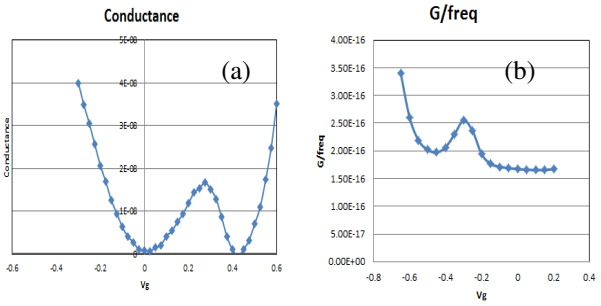

Fig. 8: Conductance plot measured at 10kHz (a). The hump in the depletion regime indicates that traps add extra charges which respond dynamically to the AC signal. (b) TCAD results.

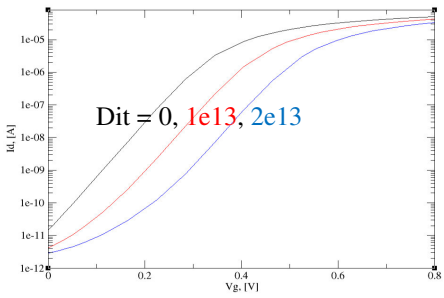

Fig. 9: Id-Vg curves for a long-channel (Lg=200nm) device with various trap densities. As the trap density is increased Vth is increased and the subthreshold slope is degraded. Note that in the simulation the trap is located in the midgap region so that the trap charge impact is noticeable at lower Vg regime.

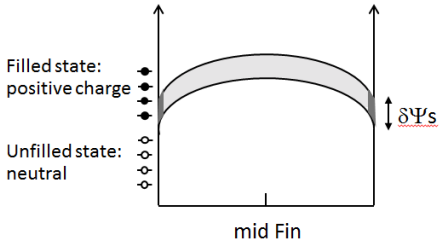

Fig. 10: Potential distribution inside the fin when surface traps are included. As the device potential increases neutral traps are filled with holes which change the charge of the device. (dark shaded area at the surface)

trap density distribution with respect to energy and capture cross section area (σ_h). In order to calibrate σ_h, we investigated the hump region of the CV curve. Fig. 7 shows the frequency dependency of the ratio of the capacitance at Vg = -0.4 V and C_{min}. This "dispersion ratio" was introduced in order to compare the dispersion behavior between experimental and simulation data in a simplified manner. As shown in Fig. 7 the frequency response of the CV curve from real hardware matches our TCAD data if σ_h is set between 1e-18 and 5e-18 cm^{-2}.

Although TCAD can extract the Dit level from the CV curve we want to compare the result with the extraction method used in experiment, viz., the conductance method [4]. In this method the DC bias forces the transistor to operate in the depletion mode while an AC signal with frequency *f* applied to the gate results in periodical changing of the Fermi level at the interface. In steady state the traps in the proximity of the Fermi level alter their occupancy. These extra trap/de-trap or charge storage/release processes act like an inductor with impedance inversely proportional to the frequency: a higher frequency gives rise to a smaller number of trap/de-trap processes which results in a reduced impedance. The total impedance measured at a specific DC bias point is comprised of the parallel connection of the MOSFET capacitance (Zc) and the trap impedance trap (Zr). The conductance method allows extracting the Dit level by assuming that the minimum of the total impedance occurs when Zc is equal to Zr. Fig. 8(a) shows the experimental peak conductance in depletion mode from which a trap density of 1e12 $cm^{-2}eV^{-1}$ can be determined.

In our TCAD simulation we apply the same bias configuration as in the experiment. A DC bias and a sinusoidal voltage is applied to the gate node and the current is monitored at the S/D/substrate node to calculate the impedance. Fig. 8(b) depicts the simulation results showing a peak conductance in depletion mode. Following the conductance method described above the TCAD simulation yields Dit = 1.8e12 $cm^{-2}eV^{-1}$ which is relatively close to the Dit level used in the actual TCAD simulation. Note that the conductance method is a convenient way of extracting Dit with over simplified assumption such as neglecting surface potential fluctuation due to depletion. However, it is good enough to guide the experimental direction in the real hardware.

C. *Long channel device characteristics*

The long-channel mobility was extracted with a D_{it} of 1e13 $cm^{-2}eV^{-1}$ and compared to a device without traps. As shown in Fig. 3 less than 5% of the mobility was degraded due to traps, which is a considerably small amount. It should be noted that our simulations do not factor in the surface roughness degradation from a poor Ge/oxide interface. Therefore it is possible that the TCAD results may underestimate the impact of traps on the mobility. Fig. 9 shows the Id-Vg curve of the long-channel device with various Dit levels. Not only is the threshold voltage level increased as in the CV curve but the

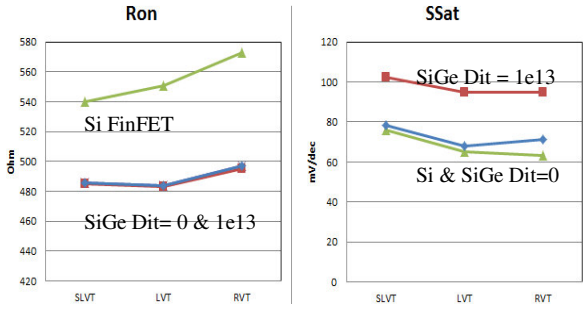

Fig. 11: (a) SC device simulations show a 10% improvement of the SiGe channel Ron due to the higher hole mobility. (b) Subthreshold behavior including traps. Traps lead to a significant degradation of the SC control.

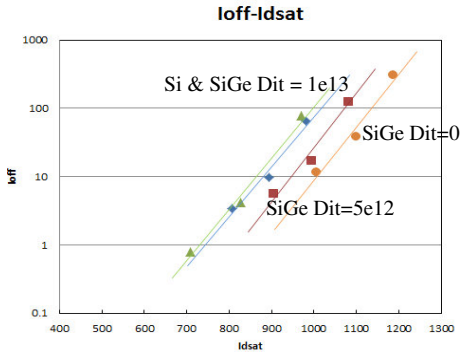

Fig. 12: Idsat vs. Ioff for Si and SiGe channels with various Dit levels. The 14% performance improvement of the SiGe channel without traps is gradually degraded as the Dit level increases.

subthreshold slope is increased in the lower gate bias regime when traps are included. We believe this to be due to the extra charges coming from occupied traps.

The subthreshold slope can be expressed by the derivative of the oxide potential with respect to the surface potential and is given by

$$S \approx 2.3\frac{kT}{q}\left(1+\frac{dV_{ox}}{d\psi_s}\right)=2.3\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right)$$

where $\delta V_{ox}/\delta\Psi_s$ is represented by the relative capacitance between the depletion layer C_d and the oxide layer C_{ox}. Note that the width of the fin is less than 15nm which is thin enough to assume that the device is fully depleted except at the very bottom of the fin. In this case the potential distribution inside the fin can be expressed by a parabolic curve as shown in Fig. 10. When there are no traps the potential distribution shifts up and down with respect to the gate bias without changing the charge state, i.e., $\delta Q/\delta\Psi = C_d = 0$ resulting in $S \approx 60$ mV/dec. When there are traps $\delta Q/\delta\Psi$ has a non-zero value associated with the Fermi level and trap density at the surface resulting in higher subthreshold slope. This trap charge is illustrated in the Fig. 10 as a dark gray area at the surface.

D. Short channel device characteristics

The short-channel device performance was studied including all the factors discussed above, i.e., fin shape, stress relaxation, quantum confinement effects, and interface traps. Fig. 11 (a) depicts Ron (0.05V/Idrain(@Vth+0.5V) for three Vth devices and shows a 10% improvement due to the SiGe channel; the impact of traps, however, is small. In contrast, the subthreshold behavior deteriorates significantly as the trap concentration is increased (Fig. 11(b)), which is in line with long channel behavior in Fig. 9 and [5]. The transistor performance was further investigated by comparing Ioff vs. Idsat for various cases (Fig. 12). The SiGe channel device performs 14% better than the reference device when traps are absent; however, this performance gain gradually diminishes as the Dit level increases. We project that the Dit concentration must be controlled to below 5e12 $cm^{-2}eV^{-1}$ in order to achieve the full benefit of the SiGe channel.

IV. Conclusion

We calibrated a TCAD deck with experimental data focusing on the device elements unique to SiGe FinFETs. These elements include: 1) adoption of a numerical algorithm based on Bezier curves to match complex fin shapes; 2) calibration of device parameters to fit the threshold voltage sensitivity with respect to the fin thickness and Ge concentration; 3) new "free channel" boundary conditions for the stress calculation to achieve the observed stress profile; 4) implementation of the conductance method by TCAD for the extraction of Dit; 5) calibration of the trap capture cross section using frequency dispersion phenomena. Finally, we analyzed the short-channel device performance with our calibrated deck. We project that SiGe FinFET devices can achieve a 14% performance boost over conventional Si FinFET devices if the Dit concentration is controlled to below 5e12 $cm^{-2}eV^{-1}$.

References

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