Modeling of Black Phosphorus vertical TFETs without chemical doping for drain

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***Abstract*—A new vertical tunnel FET design based on black phosphorus is presented in this paper adopting asymmetric layer numbers for top and bottom layer with undoped drain. The results show that the SS and I_{on}/I_{off} can be maintained below 10 mV/dec and beyond 10^5, respectively, when channel length is down to 3 nm.**

Keywords—Non-equilibrium Green's Function;DFT;tunnel FET; black phosphorus

I. INTRODUCTION

Low power operation of electronic devices is increasingly important for future consumer products in view of better user experience as well the energy crisis we are facing. In addition, further scaling in modern integrated circuit faces a major challenge due to the excessive operation power density. Tunneling FET (TFET) [1-3] is among the prime candidates for low power post-CMOS computing. The idea behind TFETs (and other steep subthreshold slope (SS) devices) is to create an ideal abrupt switch—SS ~ $[V_T - V_{G,\,OFF}]$/log $[I_{ON}/I_{OFF}]$) much less than thermal limit (60 mV/dec)—therefore enabling the reduction of the operating voltage and overall power consumption. The use of 2D materials is particularly appealing for TFET design due to their sharp density of states (DOS), narrow thickness (which leads to excellent electro-static control), and absence of dangling bonds at the surface. In the past, researchers have explored various TFET device architectures and design using group IV (e.g., [4, 5]), III–V semiconductor (e.g., [6, 7]), graphene/carbon based materials (e.g., [8]), and, most recently, 2D bilayer hetero-junction vertical TFET/tunnel diode based on vertical stack of monolayer transition metal dichalcogenides (TMDC) [9-13]. However, most of the literature work shows only mediocre device performance with either high off-state leakage or unsatisfactory low on-current due to interface states and indirect nature of band gap. In this work, we explore an advanced tunneling FET device design purely based on 2D materials with the advantage of dangling-bond-free interface for the realization of ultra-scaled and low-power steep subthreshold logic devices.

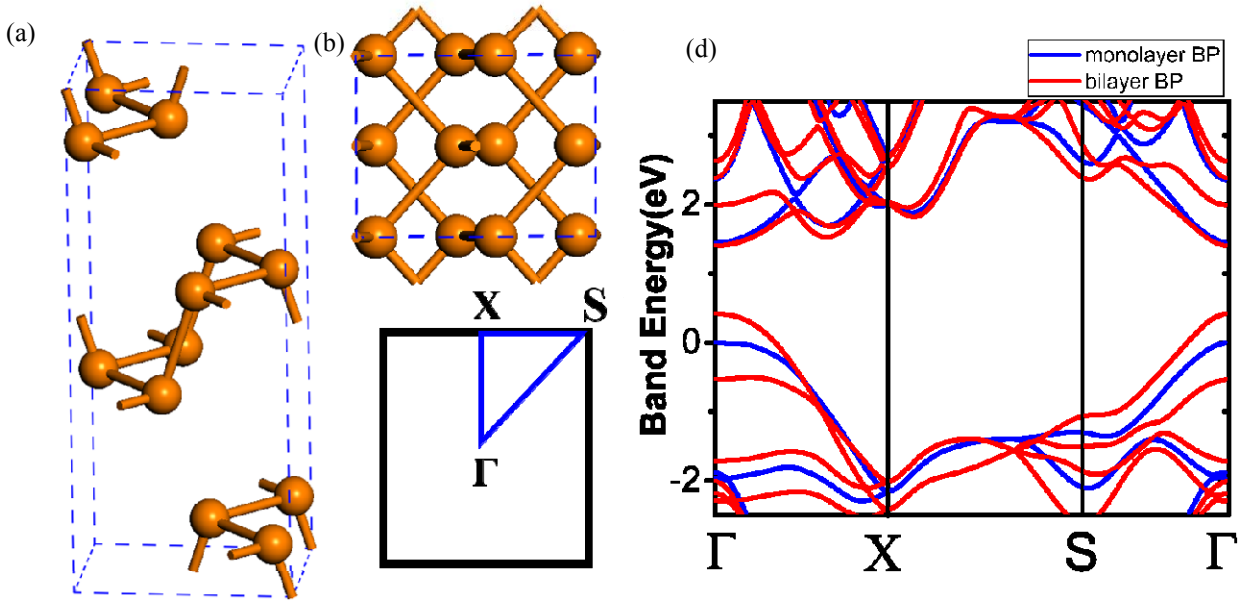

Fig. 1. (a) Side view (b) top view of the crystal structure of BP (c) 2D Brillouin Zone of BP (d) DFT bandstructure of monolayer and bilayer BP generated with MLWF using s- and p-orbitals.

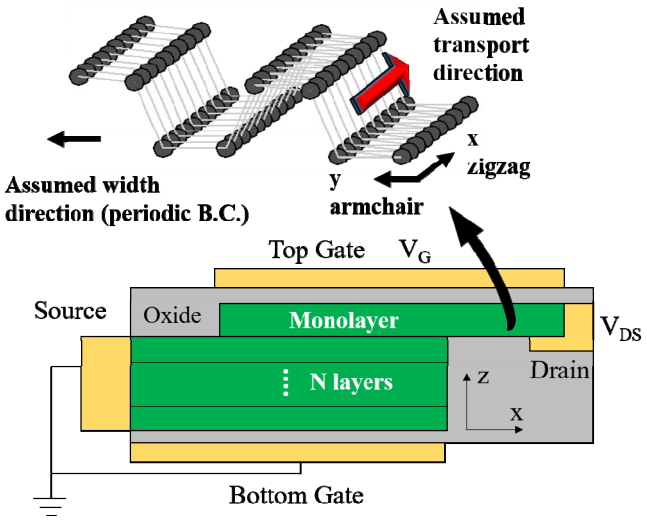

Fig. 2. Schematics of the crystal structure of BP and the TFET device.

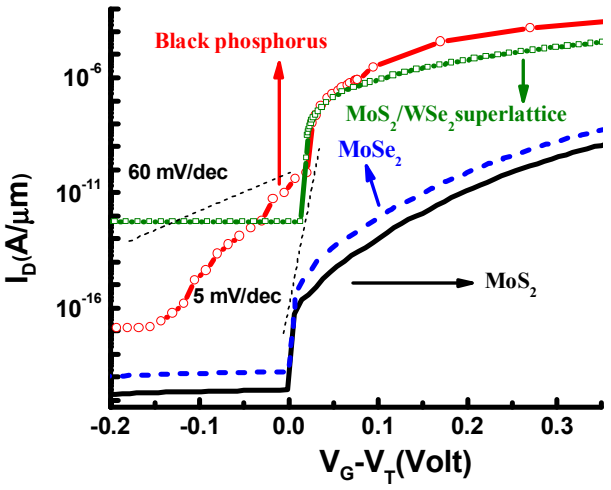

Fig. 3. Simulated ID–(VG−VT) curves for 5 nm np homo-junction TFETs based on MoS_2 (solid black), $MoSe_2$ (dashed blue), MoS2/WSe_2 superlattice (squared solid green) and black phosphorus(circled solid red).

On the hand, conventional TFET structures where the source and drain regions have opposite doping types suffer from significant leakage in the short channel limit [14], although heavily doped source and drain regions with opposite polarity are desirable to ensure large on-current. Overall, one of the major challenges toward ultra-short TFET is to minimize off current. To tackle this problem, we exploit the layer-dependent nature of 2D materials that can offer superior electrical controllability even in off state, using multiphysics simulation framework coupling Density Functional Theory (DFT) and Non-equilibrium Green's Function (NEGF).

II. Methods

Prior to the NEGF simulation, we use the Synopsys Sentaurus TCAD tool [15] to perform self-consistent simulations of 2D vertical TFET in order to provide some insights on materials selection for the subsequent NEGF simulation. The band-to-band tunneling (BTBT) underlying the TFET operation is modeled using the dynamic non-local path band-to-band model, implemented in Sentaurus. This model takes into account the nonlocal generation of electrons and holes caused by direct and phonon-assisted BTBT processes. All relevant tunneling parameters of the simulated 2D multilayer materials are obtained from either experimental data or ab initio theoretical calculations in the literature.

In order to construct Hamiltonians for our NEGF device simulation, the bandstructure of monolayer and multi-layer Black Phosphorus (BP) was obtained by using DFT method with HSE06 functional within the DFT package VASP [16]. A 12 × 1 × 10 Monkhorst-Pack k-point grid and a 500 eV plane-wave cutoff energy are used in the electronic-structure calculations. The convergence criterion is set to less than 10^{-5} eV total energy difference between two subsequent iterations. As shown in Fig. 1, the calculated bandgap of monolayer (1.44 eV) and bi-layer BP (0.93eV) is in good agreement with experimental data. After obtaining the DFT bandstructure, we transform the Bloch functions into tight-binding like Hamiltonians based on maximally localized Wannier functions (MLWF)[17], taking account of the s-, px-, py-, and pz-orbitals of Phosphorus. Finally, the acquired Hamiltonian will then be loaded into the NanoTCAD ViDES simulation environment [18], a self-consistent Poisson-NEGF solver and we obtain the I-V curves.

III. Results

Fig. 2 shows the schematics of the vertical TFET device comprised of top and bottom BP layers, where electrons tunnel from bottom to top vertically. We choose monolayer BP as drain (top layer) which has a lower valence band (VB) than multi-layer BP (bottom layer) whose VB offset serves as a barrier to minimize leakage current. Fig. 3 shows the simulated I-V using TCAD Sentaurus with top and bottom layer of the same thickness ~2.5 nm and channel length =75nm when S/D is highly doped, and as revealed by the results, the BP TFET exhibits the highest on current and the best on/off ratio. Thus, we choose BP as the channel material in the NEGF simulation to demonstrate our design. In Fig. 4, the DOS (on the left) extracted from the Hamiltonian of simulated device have similar band gaps in both bi-layer and monolayer regions to those from DFT, therefore it justifies the correctness of our

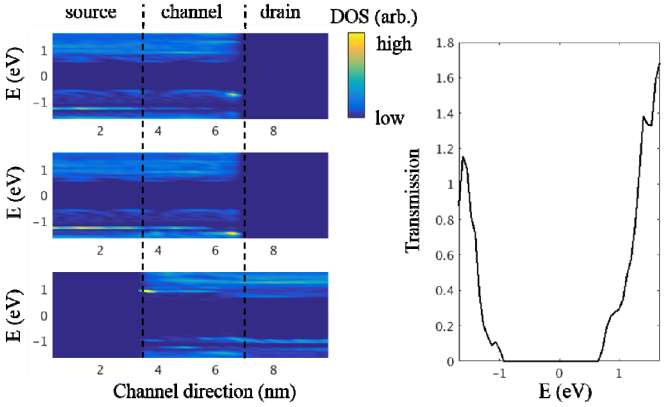

Fig. 4. DOS and transmission plot for 1L-2L BP TFET

Hamiltonian construction along with the clear gap in the transmission plot shown on the right. Taking advantage of the superior electrostatic controllability of a monolayer BP, we make the drain contact directly attached to the monolayer BP (see Fig. 1).Also, we evaluate the performance of the undoped drain contact and compare the results with the current characteristics of the device with a conventional doped drain contact. In Fig. 5, we benchmark our device (no drain doping) with a separate BP TFET device having a conventional opposite type of source and drain doping at L=3.3 nm. At channel length equal to 10 nm, our results show that both devices exhibit steep SS of less than 8 mV/dec. As the channel length decreases, device with conventional S/D doping shows significant degradation in SS and I_{on}/I_{off} due to the punch-through tunneling from the VB of source to the conduction band (CB) of drain in off state, while our proposed device maintains steep SS of ~6 mV/dec at L=3.3 nm.

IV. Conclusion

From our DFT-NEGF calculation, we find that undoped drain may be used for device operation and shows superior performance when the channel length is below 10 nm. Moreover, further simulation shows the on-current can be boosted by simply increasing the number of layers for the source without severely affecting the off-current where 4L BP TFET shows clearly improved I_{on} over 2L BP TFET using our design. It is worth noting that changing the channel orientation from zigzag to armchair direction can also effectively enhance the on-current by about 1 order of magnitude. Additionally, further consideration on changing the top layer number and integrating BP with direct bandgap bulk materials is expected to bring even higher drive-current because of the larger DOS introduced.

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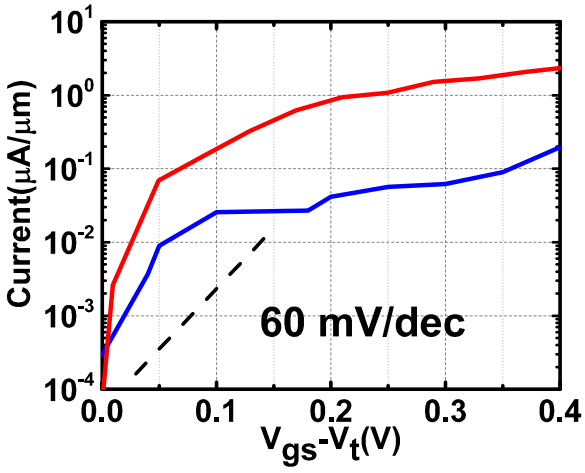

Fig. 5. Ids-Vgs curves for 3.3 nm long device with S/D doping (blue) and undoped D (red).

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