Optimization guidelines of A2RAM cell performance through TCAD simulations

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***Abstract*— A2RAM belongs to the 1T-DRAM family and is a potential candidate to replace the traditional 1T/1C-DRAM [1-2]. In this paper, we propose a TCAD simulation [3] methodology to assess A2RAM performance, validated through experimental measurement. It is then used to provide further insight in A2RAM and optimization guidelines.**

Keywords*— *A2RAM, DRAM, 1T-DRAM, TCAD, electrical characterization, optimization.

I. INTRODUCTION

The scaling of the traditional dynamic memory 1T/1C-DRAM is more and more complex. Indeed, the scaling of the access transistor follows the rules of the CMOS technology scaling. However, the storage capacitor needs to provide the same capacitance value for a lower footprint. Knowing that the reduction of the oxide thickness has reached its limit [4], the only way to keep the capacitance value constant is to use a 3D capacitor. It leads to very complex and costly process [5-6]. An alternative to continue DRAM scaling at lower cost is the introduction of new concepts of dynamic memory with the storage capacitor included inside the access transistor: 1T-DRAM. The first proposed architecture of 1T-DRAM is the ZRAM (Zero capacitor DRAM) [7]. Despite being promising, its scalability issues resulted in the discovery of many innovated architectures [8-9]. One of them is the A2RAM (Advanced secondary Random Access Memory) [1, 2]. Even if A2RAM functionality and performance have already been demonstrated in [2], a deep understanding of the cell parameters scaling and its impact on performance is needed to provide optimization guidelines.

In section 2, we describe the A2RAM cell structure and present the set-up used to assess its performance for memory application through experimental characterization and TCAD simulations. In section 3, we investigate the impact of the main technological parameters of the A2RAM cell on its performances: and finally we propose optimized A2RAM cell trends.

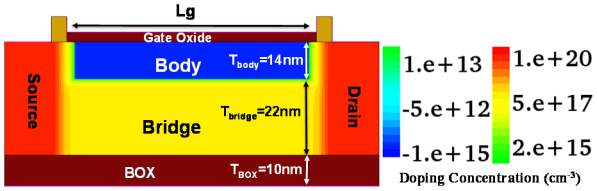


Fig.1. TCAD A2RAM structure with the main parameters definition.

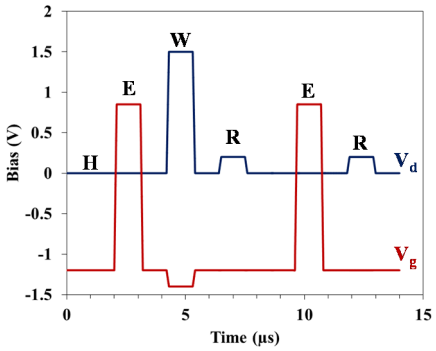


Fig.2. Vd & Vg vs time for E-H-W-R-E-R sequence.

II. TCAD SIMULATION:SET-UP AND VALIDATION WITH MEASUREMENT

A2RAM cell consists in a SOI MOS transistor with source and drain shorted by a resistive bridge, which is a doped layer (same type as source and drain) located at BOX/silicon film interface (Fig.1). When majority charges are generated in the body, they are stored because they are blocked by the gate oxide and a potential well built by the source/drain-body junctions and body-bridge junction. The current or memory state is read through the bridge which is modulated by the presence/absence of the charge in the body.

Several mechanisms have been already used to write the memory cell state [9], i.e. an excess of charges (with the same polarity as the body region doping) stored in the body. In this study, Gate Induced Drain Leakage (GIDL) [10] is considered for writing operation mainly because of its low power consumption and friendliness with reliability concerns. Considering GIDL and targeting maximum charge generation

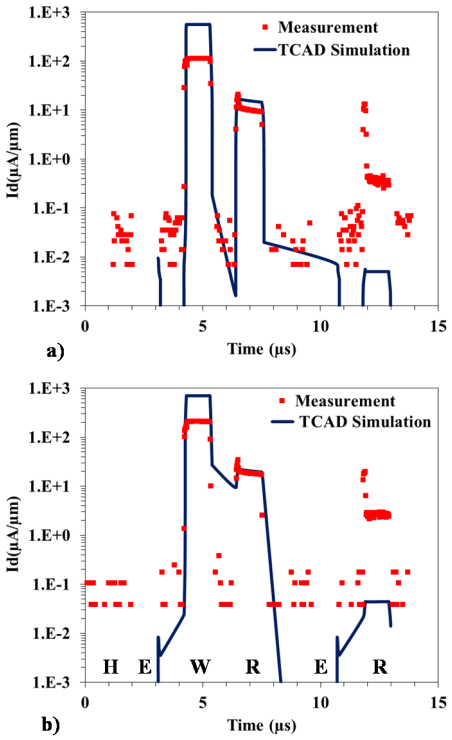


Fig 3. A2RAM drain current variation with time for W0-H-W1-R-W0-R from TCAD (line) and experimental (symbol). a) Lg=80nm, b) Lg=70nm.

while writing '1' require maximizing gate-to-drain electric field which means gate voltage V_{gw}<<0 and drain voltage V_{dw}>>0. Erasing (E) is performed through capacitive coupling (V_{gE}>0, V_{dE}=0) [9] with the same condition defined in [2]. The holding (H) phase is defined such as to keep electrostatically holes (information) in the body. We bias the gate at V_{gH}=-1.2V (with drain and source grounded) to guarantee high potential barriers between body and source-drain. During the reading (R), the current in the bridge resistance is sensed by keeping the front gate channel of the transistor in off-state. The drain must be biased slightly positively V_{dR}=0.2V to prevent parasitic writing (through GIDL). To read the '0' state, the gate bias V_{gR} must be chosen sufficiently negative to allow to the vertical electric field to cut off the conduction through the Bridge. On other hand, to read '1' state, we need V_{gR} sufficiently low (in absolute value) to have a vertical electric field screen by holes stored in the body to allow conduction through the bridge. In this paper we choose V_{gR}=V_{gH}.

Aiming at optimizing the cell operations, we developed a TCAD strategy (see Fig. 1). Physical model considered in our simulation are: Drift Diffusion model with doping dependent mobility and nonlocal path Band-to-Band Tunneling model to account for GIDL current. To evidence A2RAM memory operation, transient TCAD simulations are performed following the E-H-W-R-E-R sequence (voltages vs. time evolution shown on Fig.2). Note that to guarantee the memory initial state, the cell is first erased.

For validate our simulation methodology, A2RAM cells were experimentally characterized (process flow described in [2]) following the voltage pattern of Fig.2. The comparison

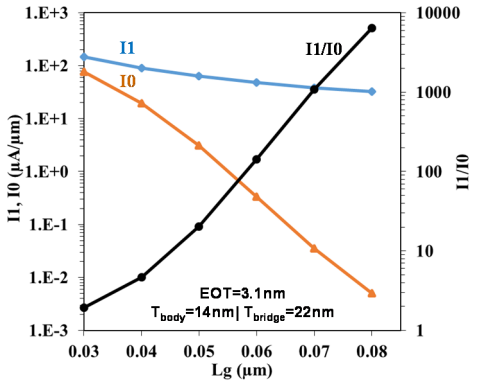


Fig.4. Evolution of I1, I0 and I1/I0 ratio from TCAD using voltage sequence of Fig. 2 with Vgw=-1.2V.

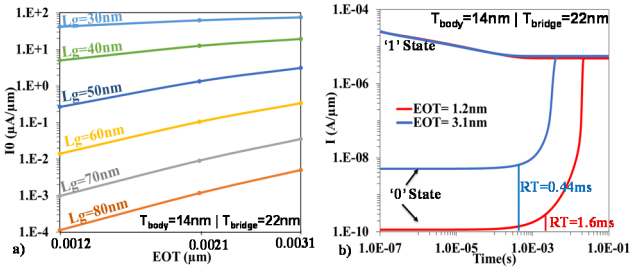


Fig.5. a) I0 evolution with EOT for different Lg using voltage sequence of Fig. 2 with V_{gw}=-1.2V. b) Evaluation of A2RAM retention time with EOT=3.1nm (blue curve) and EOT=1.2nm (red curve).

between TCAD results and experimental data for two gate lengths Lg (70nm and 80nm) is shown is Fig.3.a and Fig.3.b. While the simulated and the measured I1 current in '1' state are in good agreement in both cases, a significant difference is observed for current I0 read in '0' state. This difference is related to the doping profiles of the drain, source and the bridge mismatch between the simulated structures and the samples. In fact, V_{gR}=-1.2V is defined to cut-off the conduction of the bridge (with no holes stored in the body) during the reading of the '0' state for a bridge doping of 10^{18} cm^{-3}. If the sample has in reality a bridge doping higher than 10^{18} cm^{-3}, it is clear that the bridge is not totally depleted and thus I0 is not negligible.

III. Scaling of the A2RAM Memory Cell: Trends and Issues

Starting from the A2RAM structure geometry presented in [2] (Fig.1), the objective of our work is to give optimization guidelines for the performance and integration density of A2RAM based on a systematical analysis of TCAD simulations. To be closer to realistic DRAM operations, we have used the voltage sequence of Fig.2 with a 10ns pulse width and rising/falling time of 1ns.

We report on Fig.4 the '1' state reading current I1 after the writing phase (with V_{gW}=-1.2V and V_{dW}=1.5V) and the '0' state reading current I0 after the erasing phase (with V_{gE}=-1.2V and V_{dE}=0V) as a function of gate length (Lg). When Lg is reduced (from 80nm to 50nm), I1 increases because the length of the bridge and therefore its resistance decreases.

In the same time, due to the gate electrostatic control degradation and the shortness of the body (it is more easily filled

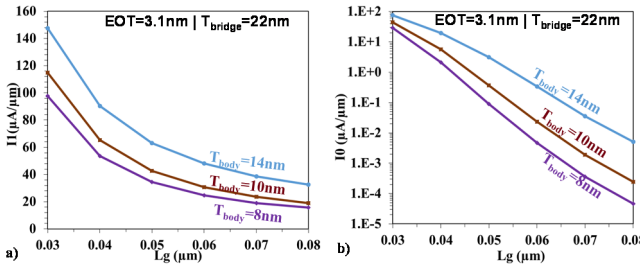


Fig.6. a) Evolution of I1 (a) and I0 (b) with Lg, for Tbody=14nm, 10nm & 8nm using voltage sequence of Fig. 2 with V_{gw}=-1.2V.

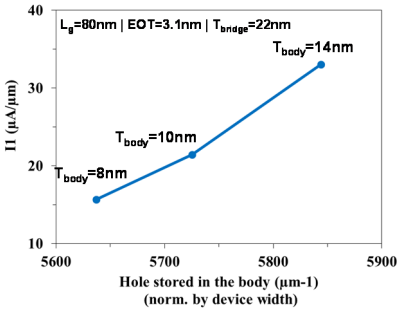


Fig.7. I1 vs holes quantity stored in the body using voltage sequence of Fig. 2 with V_{gw}=-1.2V.

by holes), I0 increases. Finally, around Lg=30nm, I1/I0 ratio is very close to 1 (right axis of Fig. 4), meaning that gate is too short to ensure A2RAM functionality.

The gate electrostatic control can be improved by using, thinner Equivalent Oxide thickness (EOT), thinner body (T_{body}) and bridge (T_{bridge}) or by tuning bridge doping (N_{bridge}).

A. *EOT reduction*

For thinner EOT, I1 remains constant when Lg is scaled down (not shown). But, I0 is reduced as can be seen on Fig. 5-a; since it is mainly related to the device leakage, so on gate electrostatic control. Smaller EOT also leads to an increase of retention time (albeit the gate insulator should be thick enough to prevent hole gate leakage). Retention time (RT) is evaluated as the time needed to reduce by half the initial current ratio I1/I0. We can observe on Fig.5-b that it is multiplied by 4 for EOT decreased from 3.1nm to 1.2nm, keeping constant the '1' state current.

B. *T_{body} reduction*

Reducing T_{body} leads to a I0 decrease, Fig.6-b shows that I0 is reduced due to the enhancement of gate electrostatic control through the reduction of the total silicon thickness $T_{si}=T_{body}+T_{bridge}$.

As it can be seen on Fig.6-a, I1 decreases for thinner "Body". In fact, the magnitude of I1 depends on the thickness and the doping of the bridge, but also on the quantity of holes stored. Since for the three structures presented in Fig.6-a, the bridge remains unchanged, the variation of I1 seen on Fig.6-a should be related to the quantity of holes stored. So, we evaluated the quantity of holes stored during the hold operation following '1' state writing in each device by integrating the

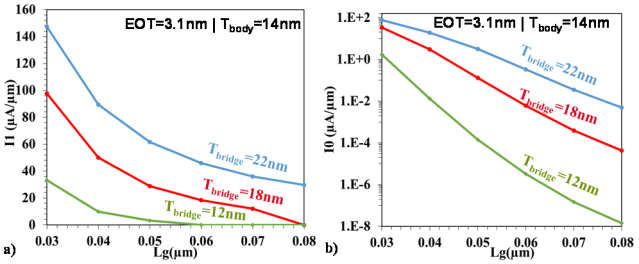


Fig.8. I1 (a) and I0 (b) as a function of Lg for Tbridge=22nm 18nm & 12nm. Same pattern of Fig. 2, except V_{gw}=-1.2V.

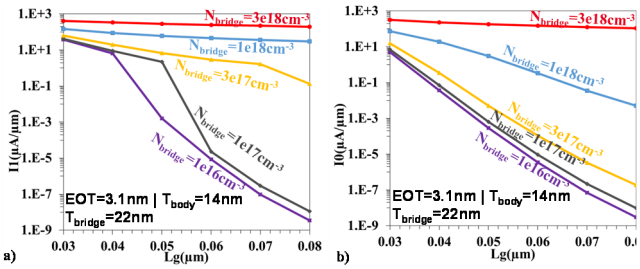


Fig.9. I1 (9.a) and I0 (9.b) as a function of Lg, Nbridge=1e16, 1e17, 3e17, 1e18(ref) & 3e18cm^{-3}. Same pattern of Fig. 2, except Vgw1=-1.2V.

density of holes in the "Body" (Fig.1). Finally, Fig.7 shows that both I1 and holes quantity stored increase with **T_{body}**.

C. *T_{bridge} reduction*

While reducing T_{bridge}, I1 decreases (Fig.8-a). Evaluating the same quantity of holes stored as in part B, we checked that this quantity is not impacted by the bridge thickness variation. Therefore, the variation of I1 seen on Fig.8-a is related to the change of the "Bridge" resistance of the of each device. So, for same Lg, T_{body} and N_{bridge}, reducing T_{bridge} increase as expected the resistance.

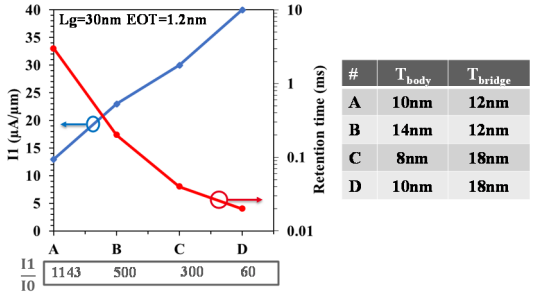
I0 is lowered (Fig.8-a) as a result of the enhancement of the gate electrostatic control (as for thinner body) but also thanks to the better bridge resistance.

As expected, thanks to the improvement of the gate electrostatic control, thinner body and bridge both improve the retention time from 1.6ms to 54ms when T_{body} is decreased to 10nm and increases from 1.6ms to 80ms when T_{bridge} is decreased to 18nm (at constant EOT=1.2nm, T_{body}=14nm).

D. *N_{bridge} reduction*

Bridge doping effect on I1 (Fig.9-a) is the same as bridge thickness effect, because the bridge doping impacts on the resistance of the bridge. I0 (Fig.9-b) decreases for lower bridge doping also because of the bridge resistivity increase. Note that if the bridge doping is too high (3e18cm^{-3}), the bridge remains always in conduction shorting the source and drain. Consequently, A2RAM is always in ON-state and then no longer functional (Fig.9-b).

In Table 1, we summarize optimization guidelines evidenced by our study. Reducing L_g, I1 increases since the bridge resistance is reduced and it is easier to fill the body. However, I0 and the retention time are degraded due to the poor electrostatic control. The reduction of EOT, T_{body}, T_{bridge}, and N_{bridge} decreases I0 and increase the retention time thanks to the



#	T_{body}	T_{bridge}
A	10nm	12nm
B	14nm	12nm
C	8nm	18nm
D	10nm	18nm

Fig.10. I1 (left axis) and retention time (right axis) for optimized structure. using voltage sequence of Fig. 2, with drain reading voltage equal to 0.1V.

better electrostatic control. But, for thinner T_{body}, I1 decreases because the volume of holes stored is reduced. Thinner T_{bridge} and lower N_{bridge} increase the bridge resistance leading to the reduction of I1 too.

Nevertheless, the optimized structure is application dependent: one needs high I1 while another one high retention time. Nevertheless, in matrix environment, I1 must be high enough to be detected by the surrounding circuits, leading to those conditions to guarantee memory operation: current margin I1-I0 > 6µA and ratio I1/I0 > 40. Fig.10 shows optimized parameters for a 30nm gate length A2RAM cell (to ensure high integration density), reaching previous conditions and with drain reading voltage reduced to 100mV to improve retention time.

TABLE I. A2RAM SCALING GUIDELINES

Scaling of	I1	I0	Retention time
L_g	↑ (bridge shorter & W1 enhanced by SCE)	↑ (SCE ↑, so leakages ↑)	Strong ↓ (SCE ↑, so leakages ↑)
EOT	Slight impact for short L_g	↓ thanks to better gate electrostatic control	↑ thanks to better gate electrostatic control
T_{body}	Slight ↓ due to ↓ hole storage capability	↓ better electrostatics thanks to thinner silicon film	↑ thanks to better gate electrostatic control
T_{bridge}	↓ due to thinner bridge resistance.	↓ better electrostatics thanks to thinner silicon film	~ less leakage but low I1
N_{bridge}	↓ due to the low doping of the resistance.	↓ better electrostatics thanks to the low doping of the bridge.	↑ thanks to better gate electrostatic control on the bridge.

IV. CONCLUSION

In this paper, we have developed a TCAD simulation methodology of A2RAM cell and validated through electrical measurement. Analyzing TCAD simulations, we observed that the electrostatic control degradation reduce the performance of the A2RAM cell when the gate length is scaled down. But, adjusting the A2RAM technological parameters such as EOT, T_{body}, T_{bridge} and N_{bridge} can improve its performances. Finally, thanks to this study, we proposed optimized A2RAM structures, which present sufficient performance to guarantee matrix functionality and enable high integration density.

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