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High Speed Low Power All Spin Logic Devices Assisted by Negative Capacitance Amplified Voltage Controlled Magnetic Anisotropy Effect

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Abstract—In this paper, we propose an all spin logic device with voltage controlled magnetic anisotropy (VCMA-ASL) and employ negative capacitance (NC) effect as a novel approach to amplify the VCMA effect. A new working strategy of 3-step operation scheme has been proposed, which reduces the energy consumption effectively as well as accelerates switching process.

Keywords—all spin logic device; voltage controlled magnetic anisotropy; negative capacitance

I. INTRODUCTION

All spin logic device is one of the most promising candidates to replace CMOS device [1]. It has been shown in our previous study that a lower power and shorter delay can be both achieved by employing voltage controlled magnetic anisotropy effect (VCMA-ASL) [2]. But the use of a bias in-plane magnetic field may not only consume extra energy, but also aggravate the fabrication complexity. On the other hand, the largest VCMA coefficient reported so far is not sufficient for scaled magnetic dimensions below 32 nm [3-4], which is a latent obstacle for VCMA-ASL device. In order to solve the problems above, a VCMA-ASL device with negative capacitance effect (NV-ASL) has been presented in this work. A novel 3-step operation scheme is proposed also to achieve high speed as well as low power.

II. AMPLIFICATION OF VCMA EFFECT BY NC

VCMA effect with different voltages are shown in Fig.1b. A positive (negative) voltage will lower (enhance) the barrier between the two stable magnetization states. The voltage across MgO barrier can be amplified by negative capacitance (NC) thus lead to an amplified effective VCMA coefficient. Fig.1c shows a simplified capacitance model for the amplification of VCMA effect with NC effect. The voltage V_x can be written as

$$V_x = \frac{V_2 C_{FE} + V_1 C_{MgO}}{C_{FE} + C_{MgO}} \quad (1)$$

assume $V_1 = 0$ and $C_{FE} + C_{MgO} \approx 0$, the voltage across MgO can be amplified to be much larger than V_2 , leading to a larger effective VCMA coefficient.

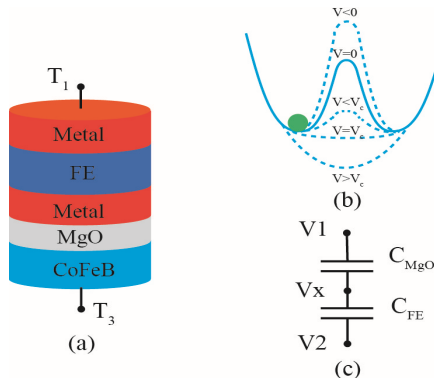


Fig.1 (a) The structure of a basic unit which can amplify VCMA effect by NC effect. (b) A schematic illustration of VCMA effect with different voltages. (c) A simplified capacitance model for the amplification of VCMA effect with NC.

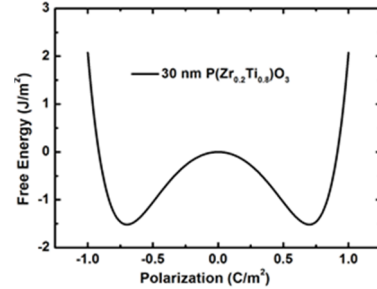


Fig.2 The free energy landscape of ferroelectric material $P(Zr_{0.2}Ti_{0.8})O_3$ (PZT) simulated with Landau theory. The negative capacitance region is between $-0.7 C/m^2$ and $0.7 C/m^2$.

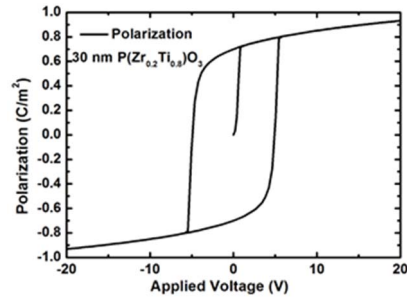


Fig.3 A simulation of the polarization-voltage hysteresis loop of a 30 nm PZT by Landau-khalatnikov equation. The ferroelectric PZT layer gets polarization around $0.7 C/m^2$ from $V = 0$ and $Q = 0$ and detached from the negative capacitance region.

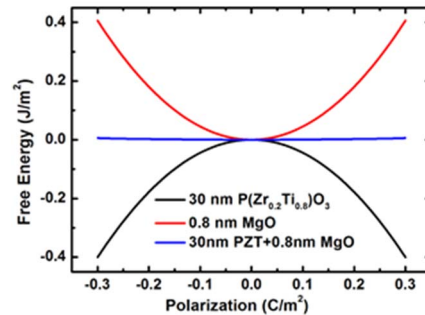


Fig.4 The free energy landscape of FE layer, DE layer and FE-DE double layer.

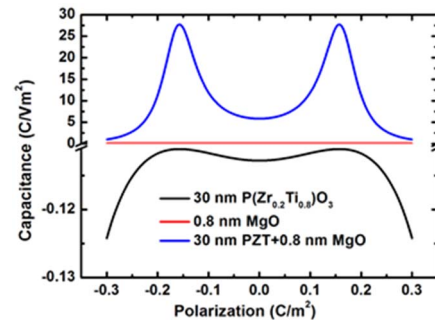


Fig.5 The capacitance of FE layer, DE layer and FE-DE double layer.

The NC effect can be achieved by ferroelectric material [5-6] and PZT is used in this paper. But the device proposed is not particularly dependent on the choice of the ferroelectric material.

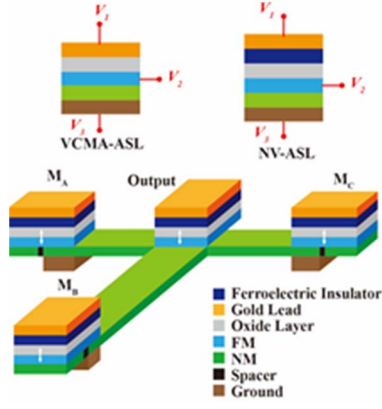


Fig.6 Layout of the proposed NV-ASL majority gate.

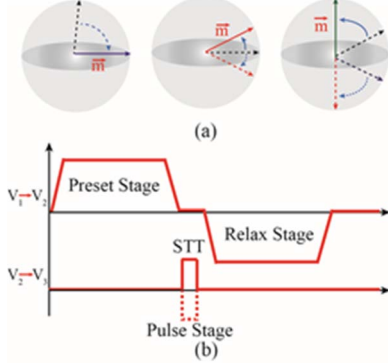


Fig.7 (a) The magnetization is driven to metastable state by demagnetization field at first. Afterwards, applying a STT pulse to tilt the magnetization to a prone state. Finally, the magnetization goes to the stable state under the anisotropy field. (b) Wave forms of the 3-step operation scheme.

In terms of free energy, the capacitance can be defined as

$$C = \left[\frac{d^2U}{dQ^2} \right]^{-1} \quad (2)$$

where U is the free energy and Q is charge (polarization). As shown in Fig. 2, a negative curvature of free energy landscape when $Q \approx 0$ can be considered as negative capacitance.

The instability of negative capacitance derived from the second derivative $d^2Q/dQ^2 < 0$ can be understood from the polarization-voltage hysteresis loop of 30 nm PZT shown in Fig.3. The free energy landscape of 30nm PZT layer, 0.8 nm MgO and PZT-MgO double layer is shown in Fig.4. It is obvious that the ferroelectric material can be stabilized in the negative capacitance region by FE-DE double layer [7-8]. And the calculated capacitance respectively is shown in Fig.5, the total capacitance is much larger than MgO capacitance, thus lead to a voltage amplification across MgO. Therefore, combined with NC effect the VCMA effect can be amplified effectively.

III. NOVEL 3-STEP OPERATION SCHEME

With a large VCMA voltage or a huge VCMA coefficient, the effective PMA field can be suppressed to be negative by demagnetization field and the stable magnetization state will be pushed to be in-plane, eliminating the requirement of in-plane magnetic bias field.

The layout of the proposed NV-ASL majority gate is shown in Fig. 6. Spin circuit theory proposed in [9] is employed to evaluate device performance and NC amplified VCMA effect is added as a new modular.

The novel 3-step operation scheme is shown in Fig. 7. First Step: A positive VCMA voltage will drive the magnetization (M_z) into a metastable in-plane state. Second Step: An ultra-short STT current is injected and make M_z be tilted away from in-plane. Third Step: M_z will move back to the desired state quickly

under the anisotropy field amplified with a negative VCMA voltage.

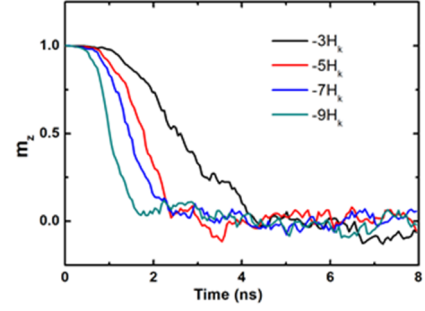


Fig.8 M_z is driven into in-plane direction in the first step by negative effective field in z direction. The negative effective field is resulted from NC amplified VCMA effect and demagnetization field. H_k is effective field when VCMA voltage is 0. Stochastic thermal fluctuation is considered in the simulation.

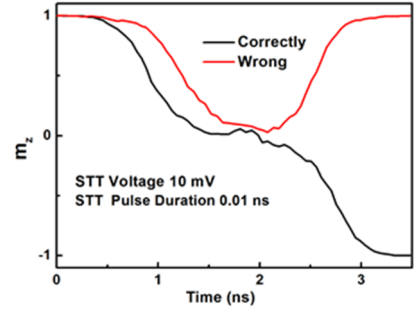


Fig.9 The simulation results for the 3-step operation scheme. First, applying the positive VCMA voltage until 2 ns. Second, a 0.01 ns STT voltage pulse of 10 mV is applied. Third, the magnetization will move under the reinforce anisotropy field by negative VCMA voltage. Sometimes the magnetization may fail to switch correctly according to the input due to the thermal fluctuation.

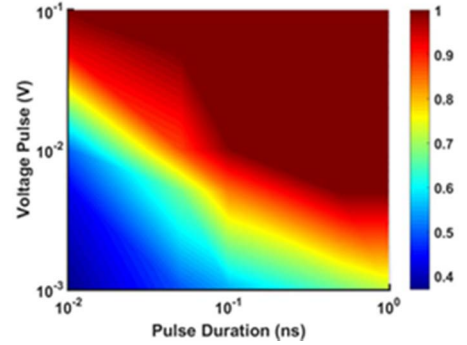


Fig.10 Contour map for the switching correct rate with varied STT voltage pulse and duration.

IV. RESULTS AND DISCUSSIONS

The thermal noise has been taken into account to evaluate the performance of the NV-ASL majority gate. With different amplification ratios of the negative capacitance, the incubation of the preset stage is shown in Fig.8. The larger the effective PMA field is, the faster M_z driven to the in-plane position.

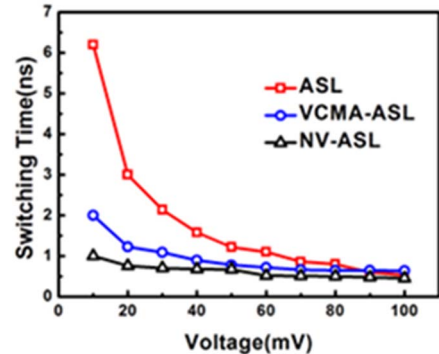


Fig.11 The switching delay of the NV-ASL majority gate with different applied STT pulse voltage. The switching time for NV-ASL is chosen with 100% switching correctness from Fig. 10.

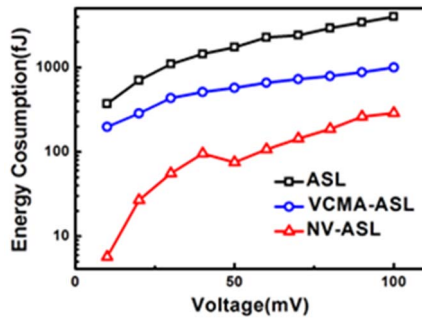


Fig.12 The energy consumption of the NV-ASL with varied applied STT pulse voltage. The energy consumption of NV-ASL is much smaller than ASL and VCMA-ASL.

As shown in Fig.9, if the signal of STT pulse is too weak or the pulse duration is too short, M_z may switch to wrong state owing to the thermal noise. Statistical simulation is performed and the correct rate of the switching is shown in Fig.10. An appropriate selection of the STT pulse amplitude and duration is pivotal to achieve high speed, low power and reliable operation.

The switching time can be counted by only second step while first step can be multiplexed in pipeline design. It is apparent in Fig. 11 that the NV-ASL can achieve high-speed operation, which is superior to that of ASL and VCMA-ASL.

The switching energy consumption of ASL, VCMA-ASL and NV-ASL with different STT voltages are shown in Fig.12. NV-ASL averts the leakage current because of thick FE layer, which occupies a large portion of the energy consumption in VCMA-ASL. Power consumption of NV-ASL is much lower than that of ASL and VCMA-ASL, thanks to the short pulse period in NV-ASL and smaller leakage current.

V. CONCLUSIONS

The proposed NV-ASL will avoid in-plane magnetic bias and leakage current. Moreover, with the strategy of 3-step operation, high speed and low power consumption can be achieved simultaneously.

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