Multi-Subband Ensemble Monte Carlo Study of Tunneling Leakage Mechanisms

C. Medina-Bailon, C. Sampedro, J.L. Padilla,
A. Godoy, L. Donetti, F. Gamiz
Nanoelectronics Research Group
University of Granada
18071 Granada, Spain
cmedba@ugr.es

T. Sadi, V. Georgiev, A. Asenov
School of Engineering
University of Glasgow
Glasgow G12 8LT
Scotland, UK.

***Abstract*— The reduction of the critical dimensions of transistor architectures makes mandatory the inclusion of quantum effects different than standard confinement becomes in advanced device simulators to describe the electrical behavior. In particular, direct tunneling from source to drain, band-to-band tunneling and gate leakage mechanisms considering direct and trap assisted tunneling are of especial interest. This work presents a study of these mechanisms in Fully Depleted Silicon-On-Insulator (FDSOI) and FinFET devices using a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator.**

Keywords—band-to-band tunneling; gate leakage mechanism; direct tunneling; trap assisted tunneling; MS-EMC; FDSOI; FinFET

I. INTRODUCTION

As electronic devices have been scaled down, the performance of conventional devices have been degraded due to the appearance of the short-channel effects (SCEs). They involve the loss of gate terminal control over the channel and the increase of the influence of source and drain regions being the degradation of the threshold voltage and the subthreshold characteristics some of the main effects to study [1-2]. In this way, device architecture optimizations are mainly focused on the reduction of SCEs. From a modeling point of view, it is mandatory the inclusion of additional phenomena not needed in previous technological nodes [3]. In particular, Source-to-Drain tunneling (S/D tunneling) allows electrons to go from the source to the drain through the narrow potential barrier (Fig. 1), escaping from gate control. Another leakage phenomenon is related to the use of ultra-thin insulators, where a high electric field appears, thus increasing the probability of tunneling through the thin gate oxide (Fig. 1) and resulting in the gate leakage mechanisms (GLM). Moreover, in reverse biased p-n junctions (such as drain-to-channel and source-to-channel) band-to-band tunneling (BTBT) can appear under certain conditions as in the drain region of MOSFETs under high drain bias, generating electron-hole pairs in the depletion region. In this work, S/D tunneling, GLM, and BTBT models have been implemented in a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator; then, the three effects have been simultaneously considered to study ultra-scaled Fully-Depleted Silicon-On-Insulator (FDSOI) and FinFET devices.

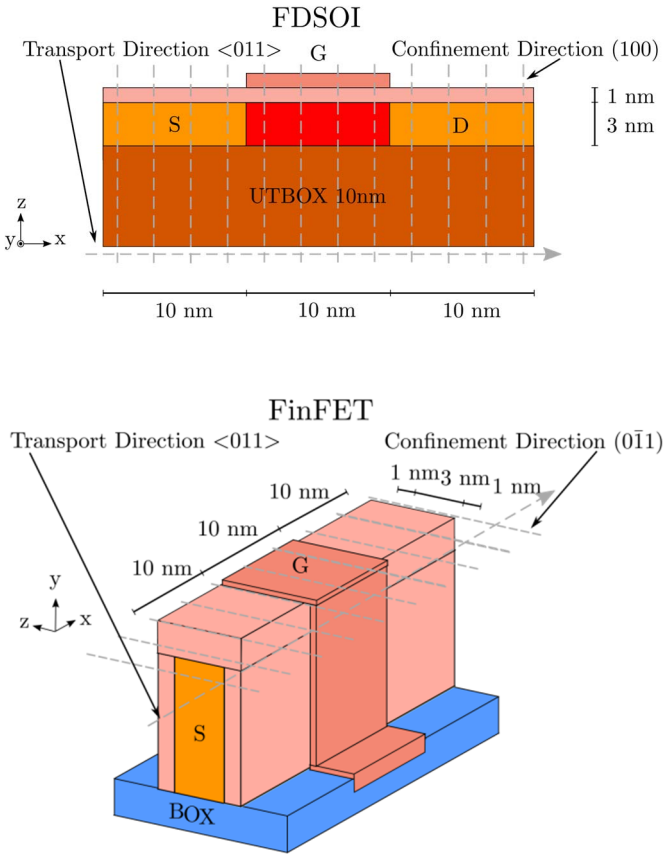

Fig. 1. FDSOI and FinFET structures analyzed in this work with L_G=10nm. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane. Summary of leakage current mechanisms herein simulated in the FDSOI structure: S/D tunneling, GLM, and BTBT.

II. Simulation Approach

The starting point of the simulation frame is a MS-EMC code that has already demonstrated its capabilities in different scenarios [4-5]. The tool, based on the mode-space approach of quantum transport, considers the system decoupled in the confinement direction, where the Schrödinger equation is solved for every considered slice, and the transport plane, using the Ensemble Monte Carlo solution of the Boltzmann Transport Equation (BTE) to describe the dynamics of charge carriers in the device. Finally, to keep the self-consistency of the solution, 2D Poisson's equation couples transport and confinement directions after every time step of the MS-EMC providing the potential profile needed to solve the Schrödinger equation.

To take into account the aforementioned tunneling mechanisms, the MS-EMC code has been modified to include each of the tunneling blocks in the corresponding part of the flowchart as independent routines (Fig. 2). It is possible then, to activate or deactivate any combination of them to study the impact of each tunneling mechanism, providing a high degree of flexibility.

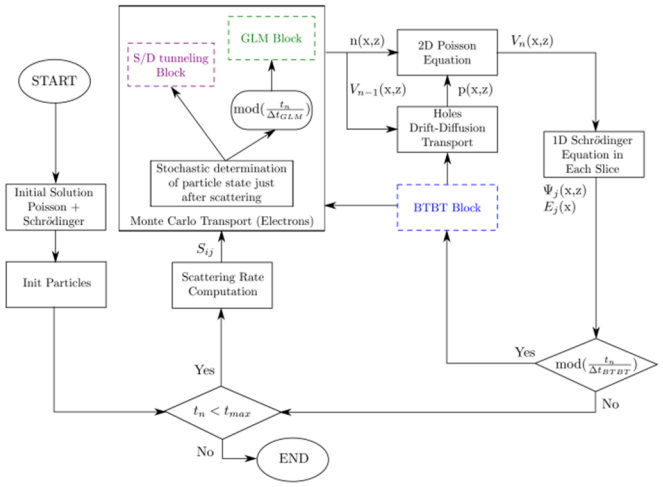

Fig. 2. Flowchart of the MS-EMC simulator with the additional blocks of the three tunneling leakage mechanisms herein implemented where *x* is the transport direction, *z* the confinement direction, *n(x,z)* and *p(x,z)* are the electron and hole concentrations, respectively, *V(x,z)* is the potential profile, E(x) is the subband energy, $\Psi_j(x,z)$ are the subband eigenfunctions, S_{ij} are the scattering rates, subscript *n* is the n-th iteration, and Δt_{GLM} and Δt_{BTBT} are the time step where GLM and BTBT are calculated, respectively.

Concerning the implementation of the tunnel mechanisms, both S/D tunneling [6] and GLM [7] are considered as stochastic mechanisms evaluated for each superparticle after a Monte Carlo flight. Direct tunneling (DT) from the substrate to the gate and elastic and inelastic trap assisted tunneling (TAT) are implemented in the simulator as shown in Fig. 3. The transmission coefficients are calculated according to the WKB approximation that depends on the position of the carrier in the device and specific parameters related to the tunneling phenomena such as the effective masses in the particular tunneling directions or band profiles. The tunneling probability is calculated then following (1):

$$T_{dt}(E) = exp\left\{-\frac{2}{\hbar}\int_a^b \sqrt{2m^* \left|E_{barrier}(x) - E\right|}\, dx\right\} \quad (1)$$

where *a* and *b* are the starting and ending points, *E* and m^* are the energy and the electron effective mass, respectively, and $E_{barrier}(x)$ corresponds to the energy profile of the barrier in the tunneling path. In the case of TAT, a rejection technique is used to ensure that trap occupation follows Pauli's exclusion principle and for the inelastic cases, energy-dependent phonon absorption-emission models are considered.

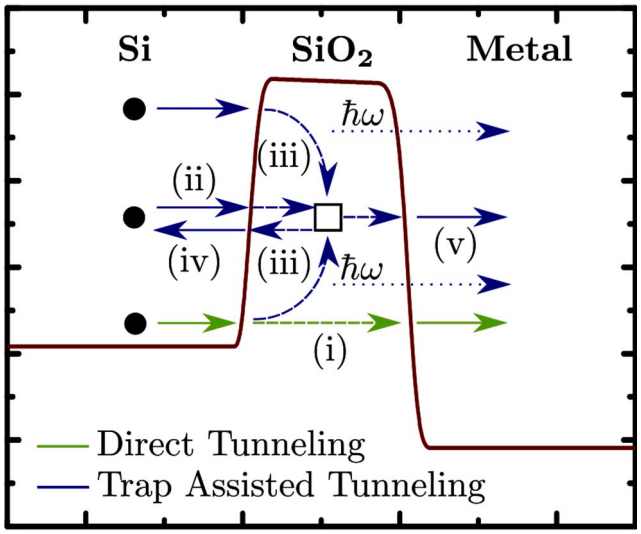

Fig. 3. Schematic band diagram of a MOS structure with metal gate and silicon substrate where transport mechanisms implemented in the MS-EMC simulator are described: (i) direct tunneling, (ii) elastic and (iii) inelastic tunneling into a trap emitting or capturing a phonon with energy ω, (iv) detrapping to the substrate, and (v) tunneling from the trap to the gate.

In the case of BTBT, the developed algorithm implements the non-local direct and phonon assisted tunneling considering quantum confinement [8]. It is based on the Kane's model to determine the BTBT generation rate per unit of volume for both electrons and holes. The non-locality is included in this approach by computing the electric field as a function of the tunneling path inside the barrier, which considers the carrier jump from one grid point to the next one provided that this leap follows the valence band maximum gradient trajectory (F_{max}). This tunneling path is dynamically modified according to the self-consistent potential computed during the simulation. Then, the generated charge is included in the simulation domain according to the time step and the generation rates. As holes are described by a drift diffusion approach, a correction in hole concentration is simply added to account for the generated holes. Finally, a number of superparticles representing electrons is generated in the

fundamental subband whose considered grid cells are calculated according to the probability distribution of the generation rates.

III. Results

Device parameters and orientations for the structures herein analyzed are shown in Fig.1. The considered confinement direction standard wafers changes from (100) for the FDSOI to (0-11) for FinFETs, whereas the transport direction is kept constant and equal to <011>. In this work a channel thickness T_{Si} = 3nm has been considered. The rest of main parameters are: the gate length L_G = 10nm, the gate oxide of SiO_2 with Equivalent Oxide Thickness EOT = 1nm, and the gate work function of 4.385eV. For the FDSOI device, a Back-Plane with an UTBOX = 10nm, Back-Bias polarization of V_{BB} = 0V, and Back-Plane work function of 5.17eV have been chosen. The inclusion of an additional gate in the FinFET and the differences in the orientation of the considered devices modify the electron distribution in the subbands and, consequently, the potential profile. In addition, both carrier transport and confinement effective masses vary for each considered case. Thus, the probability of undergoing one of these effects is different in each device.

At this point, different considerations must be pointed out: Firstly, the difference in the energy profile and in the fundamental subband energy level between the FDSOI and FinFET shows that the higher transport effective mass in the FinFET reduces the number of particles affected by the S/D tunneling, and therefore, the impact of this mechanism (Fig. 4 top). Secondly, the number of electrons tunneling through the gate oxide is higher in the single gate FDSOI in contrast to the vertical FinFET due to the larger electron confinement near the interface that shifts the charge centroid (Fig. 4) in the former case. Thirdly, the number of electrons generated by BTBT is higher in the FinFET because the asymmetry in the band curvature introduced by the single gate in the FDSOI increases the BTBT trajectories in the regions near the UTBOX and so the generation rates decreases (Fig. 4). Finally, it is important to emphasize that the most important tunnel phenomena for both devices is the GLM, being the direct tunneling (DT) through the gate oxide the dominant phenomenon due to the small oxide thickness.

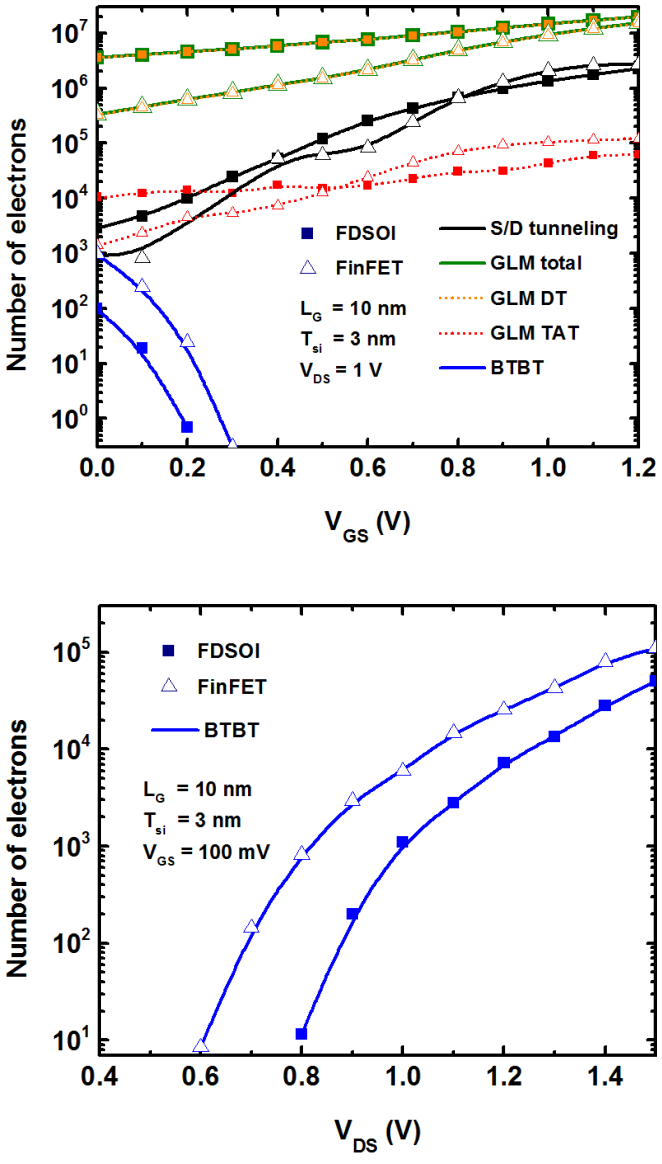

Fig. 4. Electrons generated by S/D tunneling, GLM (including the ones generated by direct tunneling and trap assisted tunneling), and BTBT as a function of V_{GS} at saturation regime (top) and BTBT as a function of V_{DS} with low V_{GS} (bottom) for both FDSOI and FinFET.

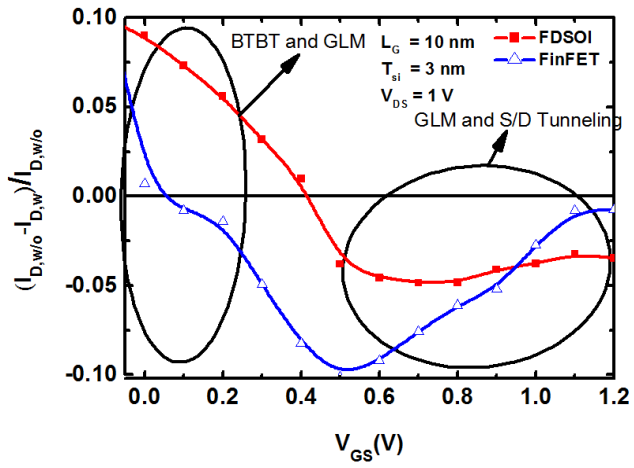

Fig. 5. Relative variation of the drain current respect to the drain current without taking into account S/D tunneling, GLM, and BTBT as a function of V_{GS} at saturation regime for both FDSOI and FinFET.

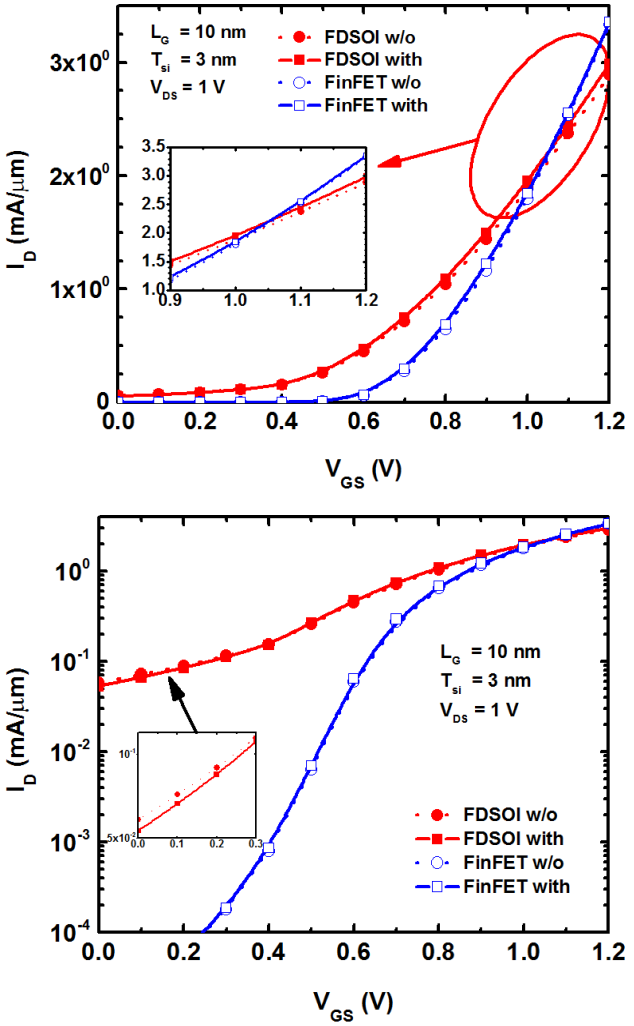

Fig. 6. I_{DS} vs. V_{GS} at saturation regime with and without tunneling for both FDSOI and FinFET in linear (top) and log (bottom) scales.

The inclusion of these effects has an important impact on the relative drain current variation respect to the case without tunneling as a function of the gate bias (Fig. 5) for both FDSOI and FinFET devices. The drain current calculated without any tunneling leakage mechanisms is bigger than the current considering the three phenomena for the OFF state because the dominant phenomenon is the GLM and thus there is a loss of the drain current through the thin gate oxide (especially in the FDSOI case) which is partially compensated by BTBT. Nevertheless, this fact is the contrary for the ON state, where the reduction of the barrier height induced by the gate enhances S/D tunneling and, therefore, the drain current (Fig 5 & 6).

IV. Conclusions

In this work, S/D tunneling, GLMs and BTBT have been implemented in a MS-EMC simulator to study the impact of tunneling in FDSOI and FinFET devices. Simulations show that GLM is the dominant mechanism for bias regimes being FinFETs less affected by this effect. Concerning the other tunneling models, BTBT becomes more important at low gate voltage whereas S/D tunneling probability increases as the barrier is reduced, i.e., at high gate bias.

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