The Impact of Hetero-junction and Oxide-interface Traps on the Performance of InAs/Si and InAs/GaAsSb Nanowire Tunnel FETs

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***Abstract*—Fabricated InAs/Si and InAs/GaAsSb vertical nanowire tunnel FETs are analyzed by physics-based TCAD with emphasis on the impact of hetero-junction and oxide-interface traps on their performance. After careful fitting of a minimum set of parameters, the effects of diameter scaling and gate alignment are predicted. Trap-assisted tunneling at the oxide interface is suppressed by scaling the diameter into the volume-inversion regime. Gate alignment steepens the slope and increases the ON-current. The 'trap-tolerant' device geometry can result in a small sub-threshold swing despite commonly present trap concentrations.**

Keywords—TCAD, nanowire TFETs, sub-thermal slope, trap-assisted tunneling

I. Introduction

Trap-assisted tunneling (TAT) at interfaces and in bulk regions is the most severe non-ideality effect in TFETs [1], much more important than channel quantization [6,4], surface roughness [7], and density-of-state tails. Temperature-dependent *IV*-measurements are mandatory to calibrate physical parameters like D_{it}, capture cross sections, and relaxation energies, and to assess the relative importance of Shockley-Read-Hall (SRH) and TAT for sub-threshold swing (SS) and ON-current. Fabricated and well characterized InAs/Si and InAs/GaAsSb vertical nanowire (NW) hetero TFETs are subject to an in-depth TCAD analysis with the aim to find a minimum set of fitting parameters which then allows to determine how far diameter scaling and gate alignment can improve SS and ON-current despite the trap densities entailed in state-of-the art NW growth technologies.

II. Simulation of InAs/Si NW TFETs

Fabricated bulk-like InAs/Si vertical NW TFETs with a diameter of ≈ 100 nm were used for the validation of simulation parameters. The devices have a p+ doped Si drain with a concentration of $N_A = 3\times10^{19}$ cm^{-3}, a 100 nm long intrinsic Si channel, and a 500 nm long n+ doped InAs region

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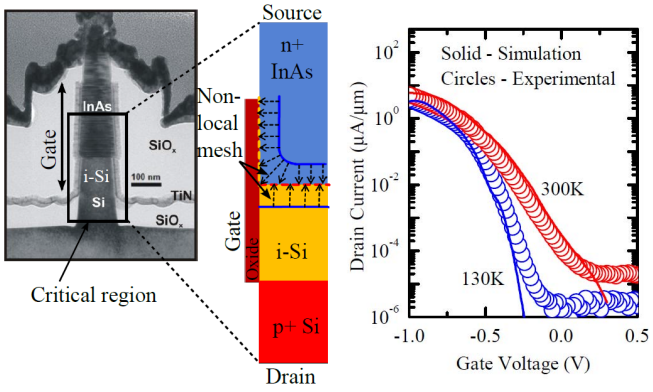

Fig. 1: (left) TEM image of the vertical InAs/Si nanowire TFET (taken from [2]). (middle) Radial cross section of the critical region (gated diode) with indicated tunnel paths. (right) Comparison of measured and simulated transfer characteristics at two temperatures [4].

with $N_D = 2\times10^{18}$ cm^{-3}. A TEM image is shown in Fig. 1(a) [2]. The Al_2O_3/HfO_2 gate stack has an effective oxide thickness (EOT) of 1.3 nm. The semi-classical TCAD simulator Sentaurus-Device [3] was used to simulate the critical region of the TFET sketched in Fig. 1(b). Band gaps in Si and InAs were set to their bulk values 1.1 eV and 0.36 eV, respectively. The valence band (VB) offset at the InAs/Si hetero-junction is still a matter of debate. Here, a value of 130 meV was assumed which had been found by an analysis of measured InAs/Si tunnel diode characteristics [5]. The work function was set to 4.8 eV. Channel quantization has a pronounced effect on the ON-current of bulk-like TFETs. A new band-to-band tunneling (BTBT) model based on the path rejection method [6,7] was implemented employing the *Physical Model Interface* of Sentaurus-Device. In this model, tunnel paths are only accepted if their energy is larger than the lowest sub-band energy, otherwise they are rejected. For the narrow TFET with $d = 20$ nm, the default *dynamic nonlocal path BTBT model* was used. Channel quantization is absent in these narrow wires because volume inversion prevents the formation of a sufficient vertical field. At the InAs/oxide interface, a uniform D_{it} of 1×10^{13} cm^{-2}eV^{-1} was used in accordance with Ref. [2]. The

'trap interaction volume' was fitted to 10 Å^3. The D_{it} at the InAs/Si hetero-interface was assumed to be Gaussian with a FWHM of 220 meV and a peak value of 1×10^{13} cm^{-2}eV^{-1} at the VB edge [7]. The trap interaction volume was fitted to 50 Å^3.

The comparison of simulated and measured transfer characteristics of the fabricated TFET [4] is shown in Fig. 1(c). Fig. 2 illustrates the effect of channel quantization, revealing a severe lowering of the ON-current (a factor of ~4 at V_{GS} = -1 V). No other effect was found that could attune simulated and measured transfer curves at high V_{GS}, which provides some confidence that the channel quantization effect is real in these devices. The ON-current is reduced by channel quantization because the rejected tunnel paths are shorter than the accepted, which leads to an increase of the average tunnel length and, therefore, a decrease of the BTBT generation rate.

Fig. 2 depicts the impact of TAT on SS at 300 K. In the sub-threshold region, the drain current is entirely dominated by TAT with negligible contribution from BTBT. The initial branch of the I_D-V_{GS} up to -0.25V curve is even solely caused by surface SRH generation [9]. With increasing gate voltage and band bending, tunneling from trap levels into the conduction band (CB) starts to play a role. The multi-phonon excitation becomes tunnel-assisted. Since this field-enhancement effect is small compared to zero-phonon trap-to-band tunneling, the drain current increases quite slowly resulting in a large SS. At 300 K, InAs/Si TAT and InAs/oxide TAT contribute commensurately to the total sub-threshold drain current. However, at 130 K the influence of InAs/oxide traps becomes negligibly small due to the exponential downslide of the multi-phonon transition probability from the VB to the trap levels with decreasing temperature. Therefore, hetero-interface TAT is dominant in the sub-threshold region which reduces the SS at lower temperatures. The fact that both the InAs/oxide and InAs/Si traps determine the room-temperature drain current makes it necessary to suppress the trap density at both interfaces to achieve a sub-thermal SS.

It is difficult to passivate traps at the InAs/oxide interface, but their contribution to the drain current via TAT can be reduced by shrinking the NW diameter d to 20 nm. This leads to the steep I_D-V_{GS} curves shown in Fig. 3. The bulk-like NW

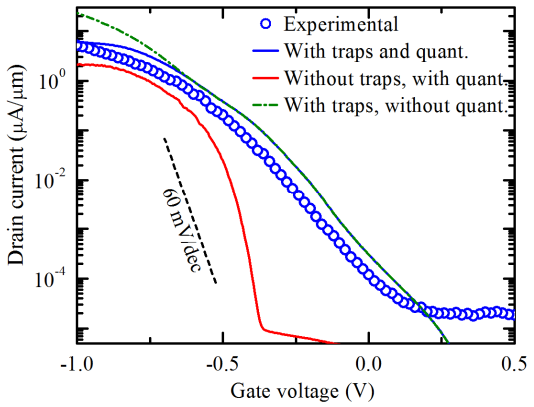

Fig. 2: Comparison of simulated transfer characteristics with/without channel quantization, and with/without interface traps [13].

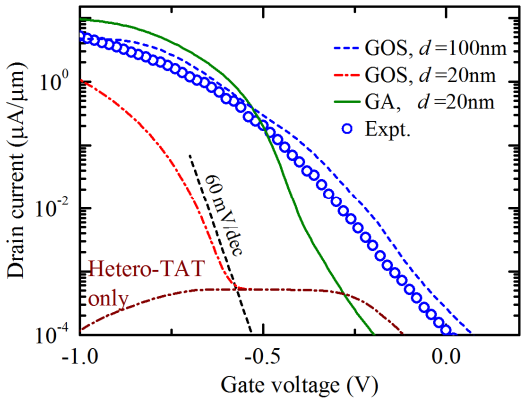

Fig. 3: Impact of scaling the nanowire diameter on the I_DV_{GS}-curves of InAs/Si TFETs (dashed blue vs. dash-dotted red). TAT at the oxide interface is inhibited, but active at the hetero-interface [13]. The joint effect of diameter scaling *and* gate alignment is shown by the solid green curve.

TFET with d = 100 nm undergoes surface inversion, and the resulting triangular-like potential well at the InAs/oxide interface significantly enhances tunneling between traps and the CB edge. In contrast, the TFET with d = 20 nm undergoes volume inversion which leads to flat band conditions at the InAs/oxide interface. In this case, only multi-phonon excitation can take place, tunnel-assistance is inhibited due to insufficient band bending. Electrostatic screening of the channel by the charged interface traps [10] is still present. However, it does not increase the SS as much as TAT.

Diameter scaling suppresses TAT only at the oxide interface, but not TAT at the InAs/Si hetero-junction. The latter gives rise to a high leakage floor at the onset of BTBT in the pTFET (see Fig. 3) which makes the transistor unusable for low-power application. This can be remedied by aligning the gate with the InAs/Si hetero-interface. Simulation results for the narrow NW TFET (d = 20 nm) with gate alignment (GA) and with gate-overlapped-source (GOS) geometry, respectively, are compared in Fig. 3. A perfectly aligned gate advances the onset of BTBT by ~0.3 V. As can be inferred from the band edge diagram along the axis of the NWs (not shown), in the GA TFET the onset of BTBT occurs at the InAs/Si hetero-interface, whereas in the GOS TFET the (small) BTBT generation rate at the same gate voltage is located at the source end of the gate. In the GOS geometry, strong BTBT can only happen when the entire overlapped region had undergone volume inversion since only then the voltage drops sharply at the gate edge in the source. This explains the higher onset voltage (by ~0.3 V). The observed leakage basin is, therefore, the consequence of the delayed onset of BTBT relative to TAT. On the contrary, in the GA geometry BTBT begins just as accumulation starts in the i-Si channel. Thus, the onset of hetero-junction TAT coincides with the onset of BTBT. This simultaneous onset of TAT and BTBT in the GA TFET reduces the minimum SS to ~59 mV/dec (from 69 mV/dec in the GOS geometry). More importantly, it also lowers the leakage floor. As a side effect of the advanced BTBT onset, the GA geometry yields a higher ON-current compared to the GOS geometry. BTBT at the hetero-interface also offers a lower tunnel barrier due to the staggered band alignment. Note, that the improvements in SS and ON-current are achieved with the unaltered high D_{it}.

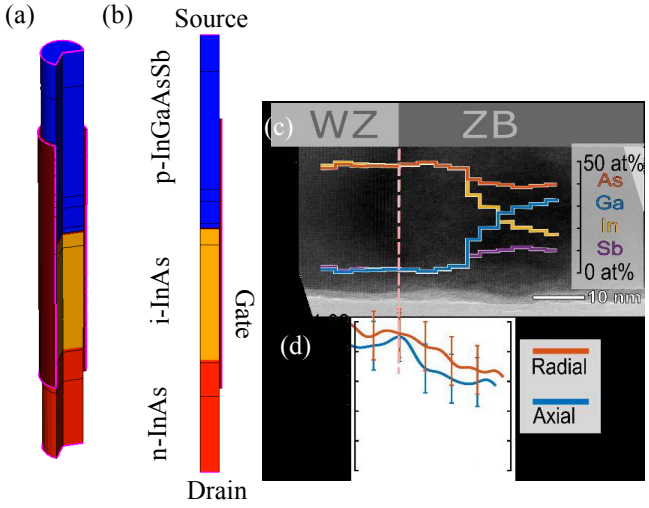

Fig. 4: (a) Schematic and (b) radial cross-section of the nanowire. (c) TEM image of the hetero-interface. (d) Uni-axial strain profiles [11].

III. Simulation of InAs/InGaAsSb NW TFETs

The vertical NW TFET with a diameter of 20 nm consists of an intrinsically doped InAs channel, a p+ doped InGaAsSb source and a n+ doped InAs drain. It was grown by Metal Oxide Vapor Phase Epitaxy from Au seed particles which were patterned on Si (111) substrate by electron beam lithography. The Al_2O_3/HfO_2 gate stack has an EOT of 1.4 nm. A detailed description of the device fabrication can be found in [11]. The radial cross section of the NW is shown in Fig. 4(b). Symmetry allows to apply cylindrical coordinates which reduces the 3D simulation task to an effective 2D problem. A TEM analysis was performed to identify the composition of the material layer system as well as its crystal structure along the axis of the NW [11]. It was found that the unintentionally doped channel (background doping of 10^{17} cm^{-3}) consists of a wurtzite (WZ) segment of InAs followed by a 10 nm zincblende (ZB) segment, topped by the quaternary alloy InGaAsSb. The InGaAsSb segment, which forms the source, is *in-situ* doped with $N_A = 1\times10^{19}$ cm^{-3}. The InAs segment in the drain is *in-situ* doped with $N_D = 1\times10^{19}$ cm^{-3}. The gate overlaps a 60 nm long part of the InGaAsSb source making the device a GOS TFET. The TEM image of the hetero-interface is shown in Fig. 4(c) along with the plot of the composition of InGaAsSb as well as the uni-axial strain along the NW axis.

Knowing the material composition and strain profile, simulations of the InAs/InGaAsSb/GaSb NW TFET were performed using the semi-classical TCAD simulator Sentaurus-Device. The actual device geometry and doping profile were used. All band structure parameters were taken from Ref. [12] without further fitting. The InGaAsSb segment was partitioned into sub-regions based on its composition (Fig. 5). The triangular-like potential well at the InAs WZ-ZB interface results in one quantization level close to the CB edge of the WZ side. It was approximated by a pseudo-grading of the material in this region (Fig. 5).

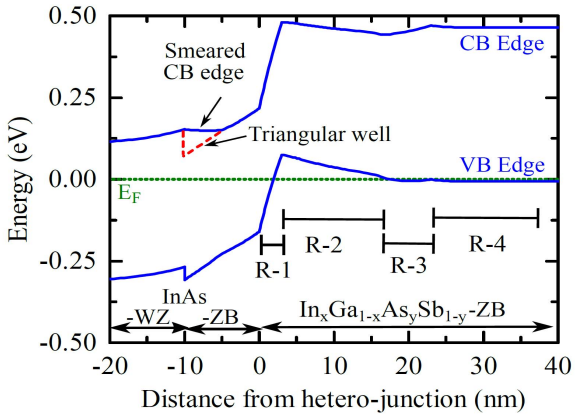

Fig. 5: Band edge diagram along the axis of the nanowire at $V_{DS} = V_{GS} = 0$ V. A triangular-like quantum well is present at the InAs-ZB/InAs-WZ interface which is mimicked by gradually changing the band gap of the material [11].

From the TEM analysis, a rapid change of the mole fraction in the 3 nm long InGaAsSb segment R-1 turned out (see Fig. 5). Simulations revealed that the TFET is most sensitive to defects within this small region (called "bulk traps" in the following). A best fit to the measured *IV*-data was obtained by choosing a concentration of $N_t = 1.6\times10^{18}$ cm^{-3}, which corresponds to exactly one defect level in the segment R-1 on spatial integration. The energy variation of this level within the gap then leads to the best fit if it is located 0.1 eV above the VB edge. The 'trap interaction volume' was adjusted to 50 Å^3 to match the magnitude of simulated and measured TAT currents. At the InAs/oxide interface the presence of donor-like defects was assumed. The good agreement of simulated and measured transfer characteristics in the temperature range between 223 K and 298 K confirms the selected parameter set and simulation set-up (compare Fig. 6). The shift of the onset voltage with temperature is attributed to a change of the oxide properties during the measurement cycle and was empirically modelled by adjustments of the work function. With a minimal number of fitting parameters it is possible to determine the

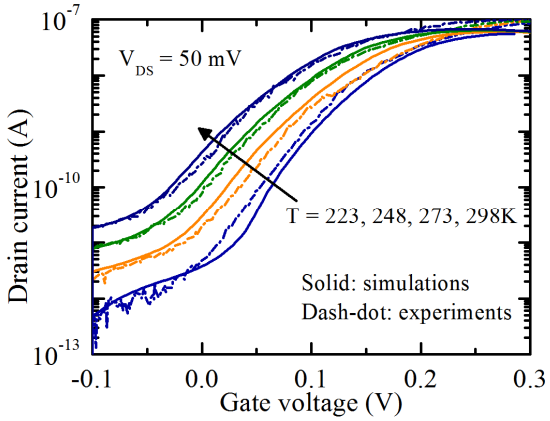

Fig. 6: Comparison of simulated and measured temperature-dependent transfer characteristics of the InAs/InGaAsSb/GaSb nanowire TFET [11].

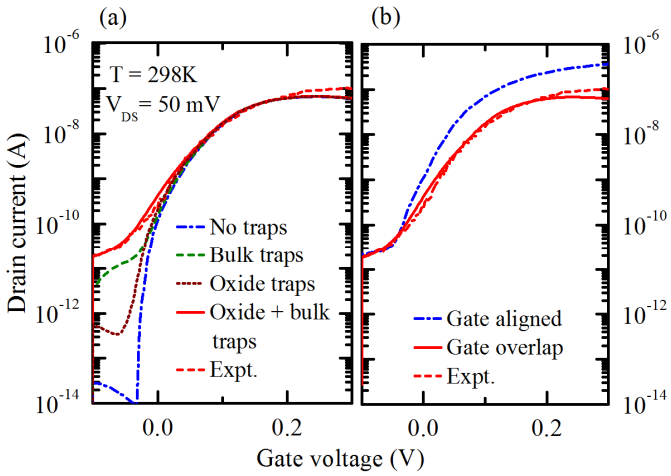

Fig. 7: (a) Transfer characteristics with various trap configurations. (b) Effect of gate alignment with the hetero-interface.

impact of individual degradation mechanisms on the performance. The effect of each trap type (bulk or interface) on the transfer characteristics is shown in Fig. 7(a). The SS could be significantly decreased if all traps were suppressed. Notably, the defects at the InAs/oxide interface alone cause only a minor SS degradation. As in the case of the InAs/Si devices in Section II, this is due to the absence of surface inversion at the oxide/semiconductor interface of the narrow diameter wires, which inhibits the strong normal field necessary for TAT. Nevertheless, InAs/oxide trap levels contribute to the SS degradation when they are occupied, since they screen the gate charge which results in a weaker gate coupling. They also cause surface SRH generation of electron-hole pairs by multi-phonon excitation, which adds to the leakage current at very low current levels. The bulk defects present in region R-1 close to the hetero-junction are the ones that mainly increase SS. Therefore, removing these traps would have a stronger impact on the improvement of the TFET performance. Although the I_{60}-current (20 nA in Fig. 7(a)) is hardly affected by the traps, the ON/OFF ratio can only be improved by a further reduction of their density.

In the study of InAs/Si NW TFETs [13], gate alignment was found to improve the SS even in the presence of a high trap density at the hetero-interface. In the InAs/InGaAsSb TFET, mainly bulk traps close to the hetero-junction increase the swing. To assess whether gate alignment can improve the situation here, a perfect alignment of the gate edge with the InAs/InGaAsSb hetero-junction was introduced. Fig. 7(b) shows that SS and ON-current improve as soon as the gate is aligned with the InAs-InGaAsSb hetero-interface. The minimum SS changes from 46 mV/dec to 32 mV/dec, the SS averaged over two decades from 54 mV/dec to 38 mV/dec. Note, that the distributions of all traps (bulk and oxide/InAs) were kept unaltered.

IV. Conclusion

Low trap densities in InAs/Si and InAs/GaAsSb NW TFETs are crucial to achieve a steep slope. Physics-based TCAD simulation based on defect characterization and temperature-dependent *IV*-measurements can assess the D_{it}-limit needed to push SS below 60 mV/dec. Scaling the diameter of the InAs/Si NW TFETs into the volume-inversion regime suppresses TAT at the oxide interface, but increases the leakage current floor and reduces the ON-current. Gate alignment accelerates the onset of BTBT. It yields an extended branch with sub-60mV/dec slope and recovers the ON-current. In the InAs/GaAsSb NW TFETs, gate alignment improves the SS. On the downside, diameter scaling makes the TFET susceptible to the electrostatic effect of single charges at the oxide interface or in the oxide if they are located close to the point of maximum tunnel generation. A misalignment of 1-2 nanometers between gate edge and hetero-interface can notably alter the slope and cause large performance fluctuations from sample to sample.

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