

# Simulation of Turn-off Oscillation Suppression in Silicon Insulated Gate Bipolar Transistors

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**Abstract**— The mechanism of the suppression of turn-off oscillation by a neutral region remaining in a silicon insulated gate bipolar transistor was investigated. From the AC analysis of the neutral region using device simulation, we found that the turn-off oscillation is not damped by the resistance of the neutral region. We proposed a model in which a current source (tail current) connected between the collector and emitter terminals in series with the capacitance can suppress the turn-off oscillation. The results of circuit simulation based on this model, it became clear that the tail current acts as a damping resistance upon the LC resonance circuit. We concluded that the turn-off oscillation is suppressed by the tail current caused by the remaining neutral region.

**Keywords**— Turn-off oscillation; Thin-wafer; IGBT; Dynamic punch-through

## I. INTRODUCTION

Oscillation of current and voltage unexpectedly occurs in Silicon Insulated Gate Bipolar Transistors (Si-IGBTs) during turn-off, as shown in Fig.1. This may be due to the depletion layer reaching the rear n-buffer layer and completely sweeping out the carriers in the drift region. This is called “dynamic punch-through” [1-2]. This phenomenon causes EMI noise and

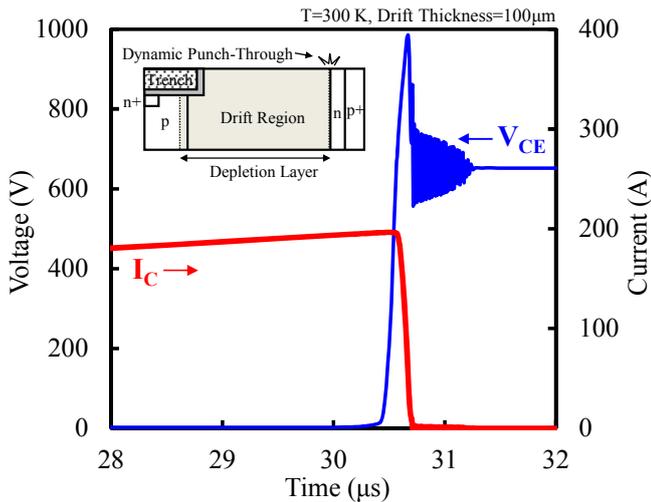


Fig. 1. Simulated turn-off waveforms of thin-wafer IGBT. Inset: schematic diagram at time of oscillation occurrence.

device disruption. To suppress the oscillation, a neutral (electron-hole plasma) region has been formed during turn-off in experiments by improving the n-buffer layer or expanding the drift region [3-4]. On the other hand, there has been an increasing demand to make wafers of Si-IGBTs thinner to reduce the conduction loss to its material limit [5-6]. Therefore, the trade-off relation between oscillation suppression and reduction of on-state voltage becomes a serious issue especially in thin-wafer IGBTs. Nevertheless, the mechanism of oscillation suppression by retaining a neutral region has not yet made clear.

This paper reports on our clarification of the mechanism of this turn-off oscillation suppression using device and circuit simulation. We confirmed, for the first time, that a tail current derived from the retention of the neutral region acts as a damping resistance on the LC resonance circuit. We conclude that the control of the amount of tail current during turn-off plays a crucial role in the further improvement of thin-wafer IGBTs.

## II. AC ANALYSIS OF NEUTRAL REGION

### A. Estimation of Damping Resistance

The turn-off oscillation has a strong correlation with the junction capacitance ( $C_d$ ) and stray inductance ( $L_s$ ), i.e., the LC resonance phenomenon. It is well-known that the LC resonance can be damped by resistance. Therefore, we surmised that a neutral region during turn-off acts as damping resistance ( $R_s$ ). To verify this prediction, in this section, we compared the resistance of the neutral region under AC operation ( $R_{AC}$ ) and the critical resistance required to suppress the LC resonance oscillation ( $R_{SC}$ ).

The circuit equation of the LCR series circuit with the DC source  $E$  can be expressed as

$$E = v(t) = R_s i(t) + L_s \frac{di(t)}{dt} + \frac{1}{C_d} \int i(t) dt, \quad (1)$$

Where  $v(t)$  and  $i(t)$  are the time variation of the voltage and current, respectively. Equation (1) can be transformed by Laplace operator  $s$  into

$$\frac{E}{s} = I(s) \left( R_s + sL_s + \frac{1}{sC_d} \right), \quad (2)$$

Equation (2) can be expressed as

$$I(s) = \frac{E}{L_S \left[ \left( s + \frac{R_S}{2L_S} \right)^2 + \left\{ \frac{1}{L_S C_d} - \left( \frac{R_S}{2L_S} \right)^2 \right\} \right]} \quad (3)$$

The resonance oscillation does not occur when the second term of the denominator in Equation (3) is less than zero (non-resonant condition). Then,  $R_{SC}$  can be given by

$$R_{SC} \geq 2 \sqrt{\frac{L_S}{C_d}} \quad (4)$$

Setting  $L_S=100$  nH and  $C_d=0.1$   $\mu$ F which corresponds to depletion layer width  $W_d=100$   $\mu$ m and dielectric constant of silicon  $\epsilon_s=11.7$ , we estimated  $R_{SC}=63$   $\Omega$ .

### B. Estimation of Neutral Region Resistance

In order to estimate  $R_{AC}$ , AC analysis was performed using a Sentaurus TCAD simulation (Synopsys) model as shown in Fig. 2. A field-stop trench IGBT with  $W_d=100$   $\mu$ m was formed. Large amounts of carriers were injected into the drift region of Si-IGBT under on-state conditions ( $V_{GE}>V_{TH}$ ,  $V_{CE}>V_{ON}$ ), where  $V_{GE}$ ,  $V_{TH}$ ,  $V_{CE}$  and  $V_{ON}$  are the gate to emitter voltage, threshold voltage, collector to emitter voltage and on-state voltage, respectively. The conductance ( $G_{AC}$ ) of the components connected between the collector and emitter terminals in an AC biased IGBT in a high injection state was calculated.  $R_{AC}$  was then determined as the inverse of  $G_{AC}$ .

Figure 3 shows the frequency dependence of  $R_{AC}$ .  $R_{AC}$  was almost independent of the frequency and is almost the same as  $R_{DC}$ , which was obtained from I-V characteristics as shown in the inset of Fig.3. The resonant frequency  $f_c$  of the LCR series circuit can be expressed as

$$f_c = \frac{1}{2\pi\sqrt{L_S C_d}} \quad (5)$$

$R_{AC}$  was estimated to be approximately 6.0 m $\Omega$  at  $f_c \approx 50$  MHz ( $L_S=100$  nH,  $C_d=0.1$   $\mu$ F). This is a quite small  $R_{AC}$  value compared to the dumping resistance  $R_{SC}=63$   $\Omega$ . These results indicate that the neutral region does not act as damping resistance.

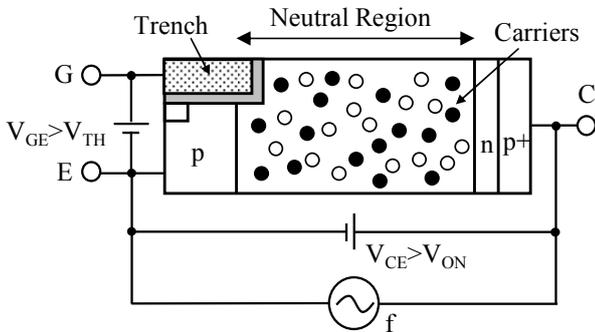


Fig. 2. Mixed mode simulation of IGBT for AC analysis.

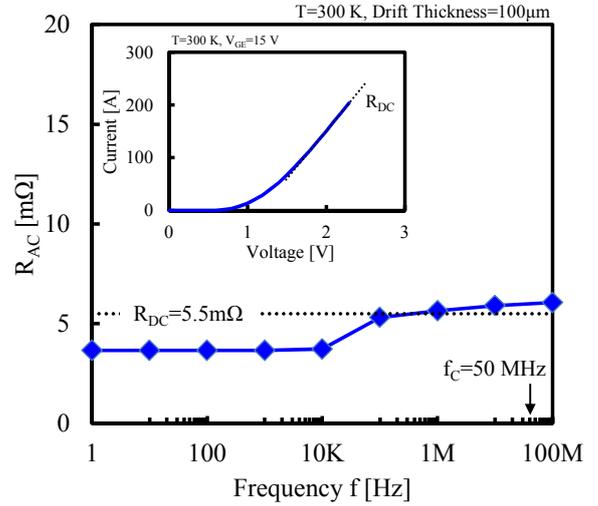


Fig. 3. Frequency dependence of neutral region resistance of IGBT. Inset: IV characteristics for extracting resistance under DC operation.

## III. CIRCUIT SIMULATION

### A. Proposed Circuit Model

In this section, we focus on the internal dynamics in the neutral region during turn-off. The stored carriers within the neutral region are swept out as a tail current during turn-off. Hence, in the remaining neutral region, enforced current flow toward the external circuit can be generated. We constructed an equivalent circuit model of the circuit between the collector and emitter terminals during turn-off, as depicted in Fig. 4. The turn-off waveforms are divided into three periods which correspond to the (a) on-state, (b) transition-state (tail current generation) and (c) off-state. In the case of the tail current period,  $C_d$  and current source ( $I_{tail}$ ) are connected in series. Since an ideal current source has infinite internal impedance [7], LC resonance suppression can be expected when a current source is connected between the collector and emitter terminals in series.

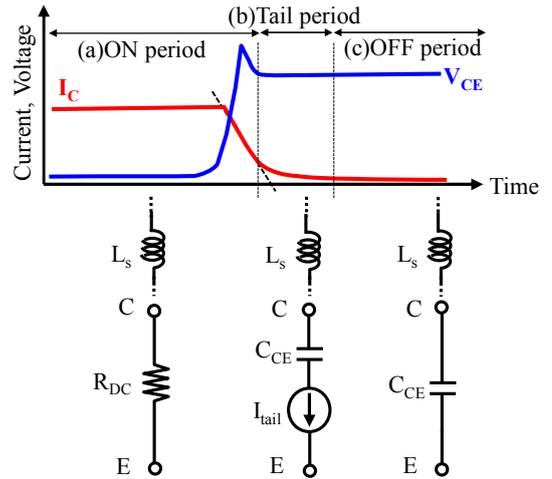


Fig. 4. Proposed models between collector to emitter terminal in each period during turn-off.

Figure 5 shows a Simplorer 7.0 (ANSYS) circuit model with inductive load using. The IGBT model includes an N-channel MOSFET and PNP bipolar transistor connected in a Darlington configuration. The detailed circuit parameters and device models are also shown in Fig. 5. The default values of the device models (NMOS6, PNP6 and Diode60) were used.

To verify our proposed model, we prepared three models of circuit topology between the collector and emitter terminals:  $C_d$  (Type A),  $C_d$  and  $I_{tail}$  connected in parallel (Type B),  $C_d$  and  $I_{tail}$  connected in series (Type C), as shown in the upper portion of Fig. 6. The equations for determining  $I_{tail}$  are shown in the lower portion of Fig. 6.  $I_{tail}$  has an initial current value at the time  $t_0$  ( $I_{tail0}$ ) and afterwards this decays exponentially with a certain time constant ( $\tau_{tail}$ ).  $t_0$  was defined as the time of maximum surge voltage. In this simulation,  $t_0=31.05 \mu\text{sec}$ ,  $I_{tail0}=50 \text{ A}$ ,  $\tau_{tail}=1 \mu\text{sec}$  were selected as tail current parameters.  $I_{tail}$  was set in accordance with the state transition model.

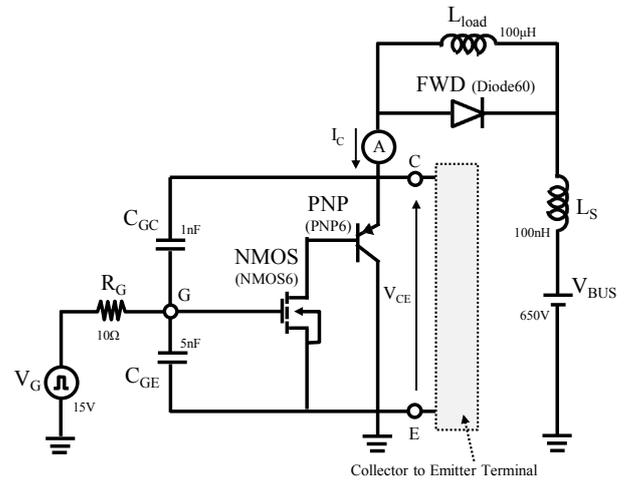


Fig. 5. Equivalent circuit configuration of inductive load with IGBT for circuit simulation.

### B. Simulation Results

Figure 7 shows the simulated turn-off waveforms with the different types of circuit topology depicted in Figure 6. The components of the tail current are also shown. The turn-off oscillation occurred in the case of Type A. Obviously, this is due to the LC resonance between  $C_{CE}$  and  $L_S$ . In Type B, turn-off oscillation also occurred even in the presence of tail current. This means that the turn-off waveform oscillates in the series circuit consisting only of  $C_{CE}$  and  $L_S$  even when  $I_{tail}$  was also connected between the collector and emitter terminals. However, the turn-off oscillation disappeared when  $I_{tail}$  was connected to the LC resonance circuit in series as seen in Type C. We thus confirmed that the suppression of the turn-off oscillation is attributed to the damping of the tail current.

To investigate the correlation between the amount of tail current and turn-off oscillation in Type C, the turn-off waveforms were obtained with different values of the  $\tau_{tail}$  and  $I_{tail0}$ . Figure 8 shows the simulated turn-off waveforms with shorter  $\tau_{tail}$  than that of Fig. 7 (c). Figure 9 also shows the results with decreased  $I_{tail0}$  in addition to shortened  $\tau_{tail}$

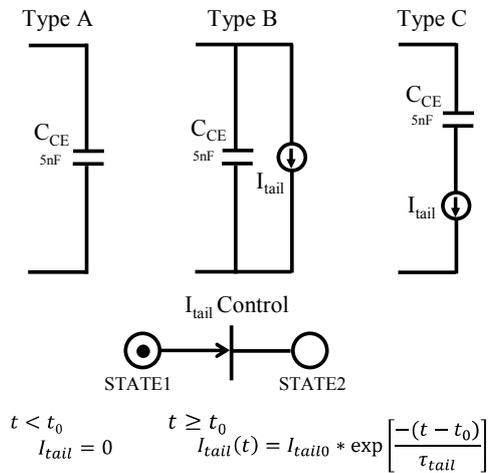


Fig. 6. (above) Model circuits between collector and emitter terminals. (below) State transition model for tail current.

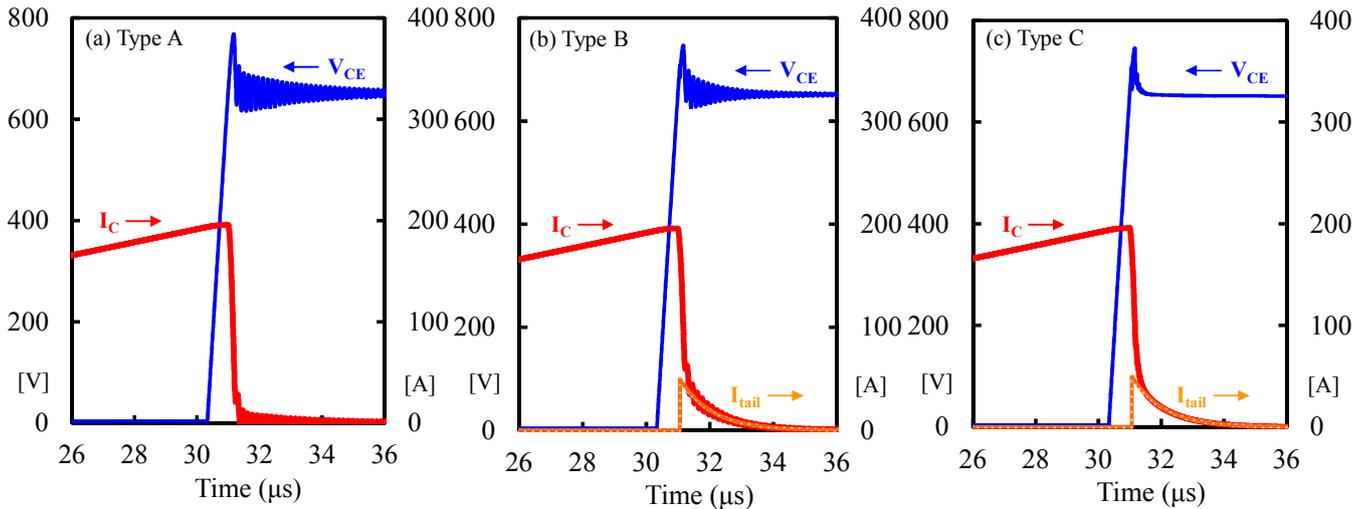


Fig. 7. Simulated results with different types of circuit topology ( $t_0= 31.05 \mu\text{sec}$ ,  $I_{tail0}= 50 \text{ A}$ ,  $\tau_{tail}= 1 \mu\text{sec}$ ).

( $\tau_{tail}=100$  nsec). In spite of the decrease of internal impedance resulting from the reduction of tail current level, the turn-off oscillation does not appear. These results indicate that even a small amount of the tail current during turn-off suppresses the turn-off oscillation.

Wide band-gap devices such as SiC and GaN are promising candidates for the next generation power devices [8-9]. Compatibility between high speed switching and suppression of turn-off oscillation become an essential issue. In order to get the maximum benefits of adopting the wide band-gap devices, the aggressive utilization of the tail current should be considered while giving attention of switching speed and turn-off loss.

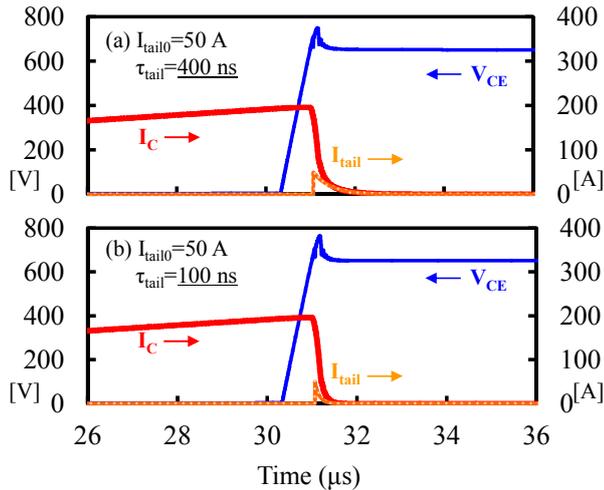


Fig. 8. Simulated turn-off waveforms with different values of time constant of tail current.

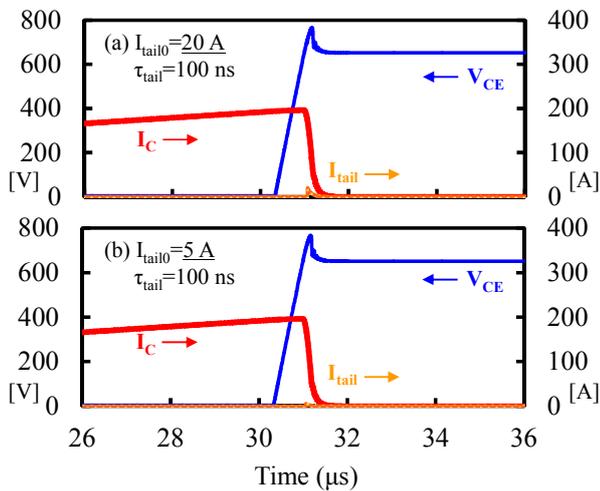


Fig. 9. Simulated turn-off waveforms with different initial values of tail current.

#### IV. CONCLUSIONS

The mechanism of the suppression of turn-off oscillation was investigated. We focused on the tail current originating from the stored carriers in the neutral region. The turn-off oscillation was suppressed by a current source that was connected between the collector and emitter terminals in series with the capacitance. As a result, we found that the tail current acts as a damping resistance upon the LC resonance circuit.

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