Electrothermal Analysis of Power Multifinger HEMTs Supported by Advanced 3-D Device Simulation

Aleš Chvála, Juraj Marek, Patrik Príbytný, Alexander Šatka, Daniel Donoval
Institute of Electronics and Photonics
Slovak University of Technology in Bratislava
Ilkovičova 3, 812 19 Bratislava, Slovakia
e-mail: ales.chvala@stuba.sk

Steve Stoffels, Niels Posthuma, Stefaan Decoutere
IMEC
Kapeldreef 75, 3001 Heverlee, Belgium

***Abstract*— In this paper we present results of the electrothermal analysis of multifinger power high-electron mobility transistors (HEMTs). The analysis is supported by effective 3-D electrothermal device simulation method developed for Synopsys TCAD Sentaurus environment using mixed-mode setup. The effects of multifinger HEMT structure metallization layout design are studied and described. Simulation results depict significant effect of metallization geometry on electrothermal properties and behavior of the power multifinger HEMTs. Very good comparison between simulation results and experimental data demonstrate validity of the proposed simulation methodology and HEMT structures analysis.**

Keywords—3-D electrothermal simulation, power multifinger HEMT, metallization layout

I. Introduction

GaN-based high-electron-mobility transistors (HEMTs) have proven their worth as next-generation high-power devices due to their wide bandgap properties. Compared to conventional semiconductor devices, GaN-based HEMTs have advantages for high-frequency, high-current, high-voltage, and high-power operations. In addition, their high-temperature operation is very attractive for electric vehicle applications [1]–[2]. However, non-uniform self-heating and thermal dissipation inside the power HEMTs with compact multifinger layout is one of the critical issues due to their capability to locally reach high power density and temperature which reduces overall device performance and reliability. Therefore, electrothermal management is crucially important to the viability of power HEMTs. Analysis and optimization using finite element modeling (FEM) electrothermal simulations are very time consuming and require high-performance hardware particularly for complex 3-D structures. Lot of existing works propose effective approaches to improve simulation time and accuracy applied in many applications demonstrates the very active research in recent electrothermal modeling [3]–[5].

In this paper, the electrothermal analysis of power multifinger HEMTs supported by advanced 3-D device simulation is presented. Analysis and optimization strategy of the metallization layer geometry design are performed and discussed. We used advanced efficient 3-D electrothermal device simulation methodology based on coupling FEM thermal and electrical circuit simulation in Synopsys TCAD Sentaurus mixed-mode setup [6], [7]. The advantage of the proposed method is in the high speed of the electrothermal simulation with respect to take into account the current non-uniformity caused by parasitic electrical resistance of the multifinger metallization to electrothermal behavior of the device. The method can be also applied to a complex power HEMTs as well as systems such as monolithic integrated converters and/or logic cells with power amplifier [8], [9]. Finally, the analysis and simulation results are validated experimentally.

II. Simulation Method

A. Structure description

The structure under investigation is the enhancement-mode AlGaN/GaN HEMT structure with a p-GaN gate. The heterostructure is grown on a silicon substrate. The epitaxial layer consists of a 200 nm AlN nucleation layer, a 1 µm AlGaN backbarrier, a 2 µm AlGaN buffer layer, a 300 nm GaN channel layer, a 15 nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 70 nm p-GaN layer. A TiN gate metal is used to form a Schottky contact on the p-GaN layer. A Ti/Al based metal stack is deposited as ohmic drain/source contacts and power metallization layers with total thickness 3.5 µm. The gate length, gate to drain distance, and gate to source distance are 0.8 µm, 6 µm, and 0.75 µm, respectively [10]. The multifinger metallization uses one collection pad for drain and source bars on the opposite sides. The 3-D thermal model includes whole power HEMT structure packaged in SMD package suitable for power GaN and placed on a printed circuit board (PCB) (Fig. 1).

B. 3-D mixed-mode simulation method

Mixed-mode setup in Sentaurus Device was used for electrothermal simulations of the proposed HEMT model. The approach interconnects HEMT circuit temperature dependent

© 2017 The Japan Society of Applied Physics

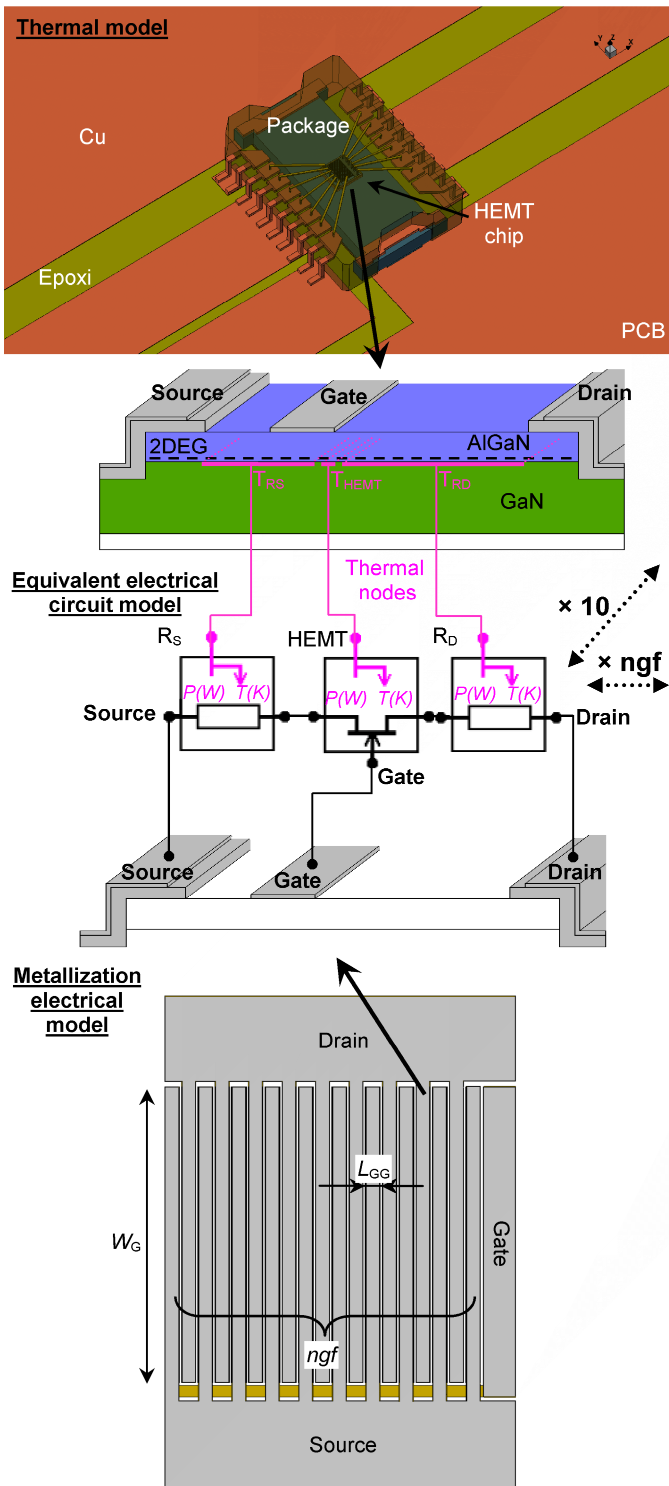

Fig. 1. Schematic diagram of mixed-mode approach for electrothermal simulation of power multifinger HEMT. Thermal nodes provide temperature exchange and heat flux between 3-D FEM thermal model and HEMT equivalent electrical circuit model. Current flow is solved in 3-D FEM metallization electrical model.

model with 3-D thermal model and 3-D electrical model of the metallization by thermal nodes and electrical nodes, respectively (Fig. 1) [11].

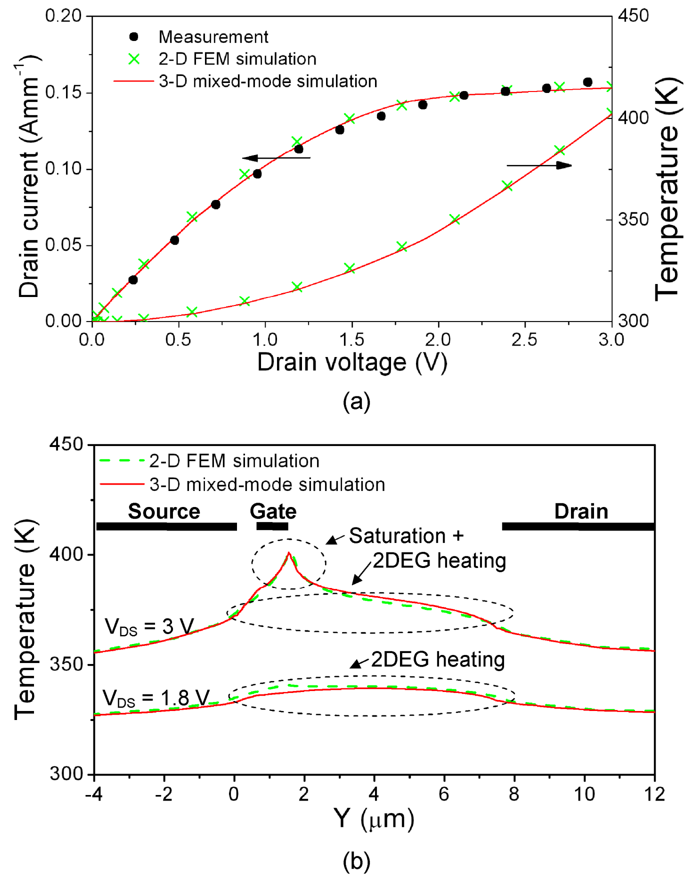

Fig. 2. (a) Comparison of measured and simulated *I-V* characteristics of the HEMT. (b) Temperature distribution inside the HEMT structure at different bias conditions.

Heat generation and heat transfer are calculated in the 3-D thermal FEM model. The temperatures on the thermal nodes are taken to drive the temperature dependent electrical parameters of the HEMT circuit model. The circuit model consists of main HEMT transistor and drain/source access resistances R_S and R_D. The HEMT circuit model coefficients are calibrated according the *I-V* measurement and 2-D FEM electrothermal simulation (Fig. 2a). The dissipated power on the model components is transferred to the 3-D thermal model via thermal nodes. The distribution of the power sources better corresponds to the temperature profile along 2DEG at different bias conditions [12], [13]. Fig. 2b compares the temperature distribution inside the HEMT structure for 2-D FEM electrothermal simulation and proposed approach.

3-D model of the structure is uniformly split into several segments along each gate what allows take into account nonuniform distribution of the current density and the temperature. The HEMT segments are electrically connected to the 3-D FEM electrical model of the metallization where the current density distribution and the voltage drop on parasitic metallization resistance are solved.

The short time of simulation is assured by solving only the heat equation in the 3-D FEM model of the package and Poisson equation in the metallization layer, and fast solving of the equivalent circuit electrical model. This methodology allows fast and effective simulation of complex systems

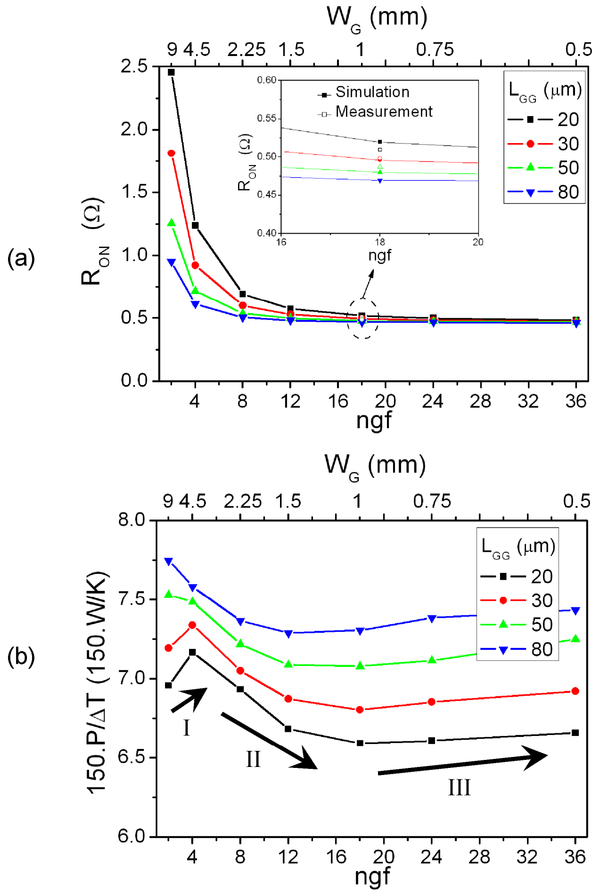

Fig. 3. Dependences of (a) on-state resistance R_{ON} and (b) dissipated power capability $P/\Delta T$ on metallization layer geometry.

including all semiconductor layers, metallization, package, and up to cooling assemblies. Depending on amount of FEM mesh elements simulation of one *I-V* curve with self-heating effects takes about 3 – 40 min for structure with 2 – 36 gate fingers, respectively.

III. Results of Electrothermal Analysis

The analysis of the multifinger power HEMT is focused on the influence of the metallization layer geometry on electrothermal properties and overall transistor behavior. The simulation variables are the number of the gate fingers *ngf* and their width W_G for different fingers spacing L_{GG}.

Fig. 3 shows geometry dependence of the on-state resistance R_{ON} and dissipated power capability $P/\Delta T$ corresponding to a channel temperature increase of 150 K for different finger spacing. The parasitic resistance of the metallization is more dominant for higher W_G and lower *ngf*, which increases R_{ON} of the analyzed HEMT. The decrease of R_{ON} with W_G lowering is caused by decreasing of metallization resistance. The lowest value of the R_{ON} is given mainly by properly selected electrophysical properties of HEMT structure. The higher R_{ON} at lower L_{GG} is caused by lower width of drain/source metallization layer with higher resistance.

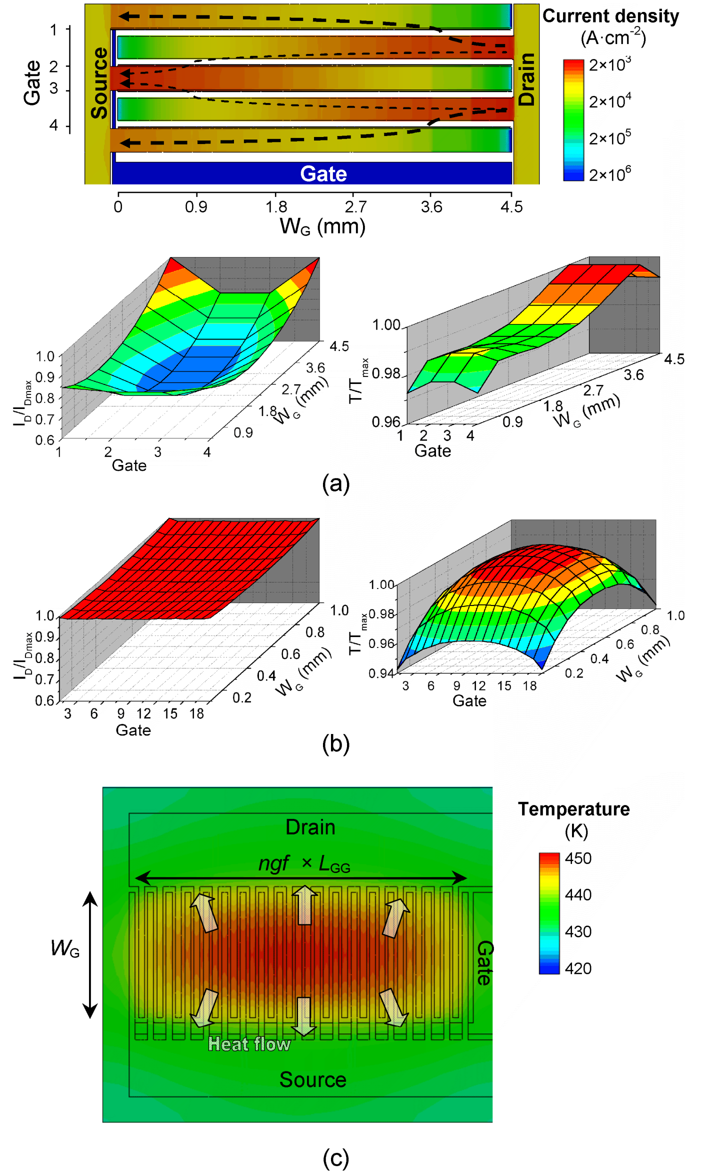

Fig. 4. Current density and temperature distribution for different geometries of HEMT structure metallization layers ((a) *ngf* = 4 and (b) *ngf* = 18). (c) Temperature distribution inside the HEMT structure with *ngf* = 36. (L_{GG} = 30 μm)

The dependence of dissipated power capability $P/\Delta T$ on the *ngf* and corresponding W_G can be split into three regions I, II and III with different behavior. Due to additional voltage drop on the relatively high metallization resistance, the current density and power load are nonuniformly distributed in the structure. The nonuniform power load reduces dissipated power capability $P/\Delta T$ of the structure. As can be seen in Fig. 4a, the most of current density flows through gate 1 and gate 4 on the drain pad side, where maximal power load and temperature occur. The $P/\Delta T$ increases in the region I (Fig. 3b) due to the current flow uniformity improvement when metallization resistance becomes negligible compared to HEMT structure resistance. Current density is homogeneously distributed in structures with shorter W_G (Fig. 4b) where the metallization resistance is lower. However, the following $P/\Delta T$

drop in the region II (Fig. 3b) is caused by the dominant thermal interaction of individual gate fingers [11]. As *ngf* increases, the maximal temperature is higher and $P/\Delta T$ decreases. At the interface of regions II and III the structure geometry has approximately square shape with the worst case heat sink condition. There is local minimum of the dissipated power capability. The structures with shorter W_G and higher *ngf* are more effectively cooled along its width (Fig. 4c). Therefore, the $P/\Delta T$ increases in the region III. In all regions it is valid that the increasing distance of the gate fingers L_{GG} provides lower thermal coupling and higher $P/\Delta T$.

The electrothermal simulation results and the analysis have been validated experimentally for four manufactured samples. Table I. compares simulated and measured R_{ON} for HEMT structures with different finger spacing (L_{GG} = 20 µm, 30 µm, and 50 µm @ *ngf* = 18 and W_G = 1 mm) and structure with L_{GG} = 50 µm, *ngf* = 36, and W_G = 1 mm. Very good agreement between simulation and measurement confirms validity of the proposed electrothermal simulation methodology and multifinger HEMT structures analysis.

TABLE I. COMPARISON OF SIMULATED AND MEASURED R_{ON} FOR DIFFERENT HEMT STRUCTURES

Structure		R_{ON} (Ω)		Error (%)
		Measurement	Simulation	
L_{GG} = 20 µm	W_G = 1 mm *ngf* = 18	0.510 Ω	0.520 Ω	+1.94 %
L_{GG} = 30 µm		0.498 Ω	0.496 Ω	-0.44 %
L_{GG} = 50 µm		0.487 Ω	0.480 Ω	-1.45 %
L_{GG} = 50 µm	W_G = 1 mm *ngf* = 36	0.252 Ω	0.250 Ω	-0.65 %

IV. CONCLUSION

The electrothermal analysis and optimization of the multifinger power HEMTs has been presented. The analysis of thermal and electrical behaviour was supported by proposed effective 3-D electrothermal device simulation using mixed-mode setup in Synopsys TCAD Sentaurus environment. The proposed simulation approach allows effective analysis of the power HEMTs as a complex system from semiconductor layers, metallization up to package and cooling assemblies operating under different bias conditions in a short time. The influence of HEMT metallization layers geometry has been studied and described. The analysis and simulation results have been validated experimentally. Undesirable impact of the high parasitic metallization resistance on the R_{ON} and dissipated power capability is dominant mainly for the structures with high gate fingers width and low fingers spacing. However, higher number of the gate fingers provides higher thermal interaction of individual gate fingers and lower dissipated power capability. The structure with very short gate fingers and high number of the gate fingers is more effectively cooled along its width. It provides highest dissipated power capability for lowest R_{ON} of the HEMT.

Acknowledgment

This work was supported by the Project PowerBase. This project has received funding from the Electronic Component Systems for European Leadership Joint Undertaking under grant agreement No 662133. This Joint Undertaking receives support from the European Union's Horizon 2020 Research and Innovation Programme and Austria, Belgium, Germany, Italy, Netherlands, Norway, Slovakia, Spain and United Kingdom. This work was also supported by the Slovak Research and Development Agency under the contract No. APVV-14-0749 and by Grant VEGA 1/0491/15 supported by Ministry of Education, Science, Research and Sport of Slovakia.

References

[1] S. Keller, Y.-F. Wu, G. Parish, N. Ziang, J. J. Xu, B. P. Keller, et al., "Gallium Nitride Based High Power Heterojunction Field Effect Transistors: Process Development and Present Status at UCSB," IEEE Trans. on Electron Devices, vol. 48, no. 3, pp. 552–559, Mar. 2001.

[2] Q. Zhou, S. Yang, W. Chen, B. Zhang, Z Feng, S. Cai, et al. "High voltage InAlN/GaN HEMTs with nonalloyed Source/Drain for RF power applications," Solid-State Electronics, vol. 91, pp. 19–23, 2014.

[3] F. Nallet, L. Silvestri, and T. Cilento, "TCAD simulation methodology for electrothermal analysis of discrete devices including package," in Proc.26th Int. Symp. Power Semicond. Devices ICs, 2014, pp. 334–337.

[4] L. Codecasa, V. Dalessandro, A. Magnani, A. Irace, "Circuit-based electrothermal simulation of power devices by an ultrafast nonlinear MOR approach," IEEE Trans. on Power Electronics, vol. 31, no. 8, pp. 5906–5916, Aug. 2016.

[5] H. Kock, S. Eiser, and M. Kaltenbacher, "Electrothermal Multiscale Modeling and Simulation Concepts for Power Electronics," IEEE Trans. on Power Electronics, vol. 31, no. 4, pp. 3128–3140, Apr. 2016.

[6] A. Chvála, D. Donoval, A. Šatka, M. Molnár, J. Marek, and P. Príbytný, "Advanced Methodology for Fast 3-D TCAD Device/Circuit Electrothermal Simulation and Analysis of Power HEMTs," IEEE Trans. Electron Devices, vol. 62, no. 3, pp. 828–834, Mar. 2015.

[7] Sentaurus™ Device User Guide, Ver. M-2016.16, Synopsys TCAD Sentaurus, San Jose, CA, USA, 2016.

[8] X. Li, M. V. Hove, M. Zhao, K. Geens, V.-P. Lempinen, J. Sormunen, et al., "200 V Enhancement-Mode p-GaN HEMTs Fabricated on 200 mm GaN-on-SOI With Trench Isolation for Monolithic Integration," IEEE Electron Device Letters, Vol. 38, no. 7, pp. 918–921, July 2017.

[9] L. Nagy, V. Stopjaková, A. Šatka, "Design Of Digital Logic Cells On InAlN/GaN Heterostructure," in Int. Conf. on merging eLearning Technologies and Applications (ICETA), Stary Smokovec, Slovakia, 2015.

[10] M. Meneghini, I. Rossetto, V. Rizzato, S. Stoffels, M. V. Hove, N. Posthuma, et al., "Gate Stability of GaN-Based HEMTs with P-Type Gate," Electronics, vol. 5, no. 14, pp. 1–8, 2016.

[11] A. Chvála, J. Marek, P. Príbytný, A. Šatka, M. Donoval, D. Donoval, "Effective 3-D Device Electrothermal Simulation Analysis of Influence of Metallization Geometry on Multifinger Power HEMTs Properties," IEEE Trans. on Electron Devices, vol. 64, no. 1, pp. 333–337, Jan. 2017.

[12] V. Šodan, S. Stoffels, H. Oprins, M. Baelmans, S. Decoutere, I. De Wolf, "A Modeling and Experimental Method for Accurate Thermal Analysis of AlGaN/GaN Powerbars," in Proc. 27th Int. Symp. on Power Semiconductor Devices & IC's, ISPSD 2015, Hong Kong, China, pp. 377–380, 2015.

[13] V. Šodan, H. Oprins, S. Stoffels, M. Baelmans, I. De Wolf, " Influence of Field-Plate Configuration on Power Dissipation and Temperature Profiles in AlGaN/GaN on Silicon HEMTs," IEEE Trans. Electron Devices, vol. 68, no. 8, pp. 2416–2422, 2015.