TCAD Simulation Methodology for Full 3-D Electro-Physical and Advanced Thermal Analysis of Power Modules

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***Abstract*—High reliability and performance of power semiconductor devices depends on an optimized design based on a good understanding of their electro-thermal behavior and influence of parasitic components on their operation. In this paper we present the analysis and the geometry optimization of the high power PIN diode structure supported by the advanced full 3-D mixed mode electro-thermal device and circuit simulation. Lowering the operation temperature by better power management and heat dissipation related to optimized structure design will allow withstanding of higher current pulses and suppressing the damage of the analyzed structure by thermal breakdown. The structure under investigation is a P^+NN^+ power diode packaged in power module. It is designed for reverse voltages up to 1800V and high forward currents up to 100 A with maximum forward surge current up to 2,7 kA**

Keywords*—power diode,3-D numerical modeling and simulation, thermal management, power and heat dissipation

I. Introduction

This paper investigates the behavior of selected Si-PiN in multichip power modules during current surge event conditions. Surges can occur in high power converters used for motor drives and grid connected systems. Based on the limited tests done so far, it can be seen that Si PiN diodes still retain an advantage as far as surge current limitation is concerned. [1, 2]

Non-uniform thermal dissipation inside the power module and corresponding self-heating is one of the critical issues when device is exposed to high current and voltage pulses. Even small electrical/mechanical (increased serial resistance, shifted contact) fluctuation in the module may lead to a catastrophic failure during real operation. Therefore, 3-D electrothermal simulations are nowadays essential in semiconductor device modeling in order to study these fluctuation effects.

II. Problem escription

Maximum peak forward current is the maximum current which diode can sustain in forward bias mode. Its value is limited by the diode junction's thermal resistance and thermal capacity and is usually much higher than the average operational current due to thermal inertia. It is based on a fact that it takes a non negligible finite interval of time for the diode to reach maximum temperature for a given current. Ideally, this figure should be infinity. This peak current can generate high heat (Joule losses) and due to the thermal resistance of metallization and passivation layers and their interfaces the heat dissipation may be insufficient and can lead to uncontrolled rise of temperature which finally destroys the diode. It is therefore necessary to find critical regions and optimize the structure and package. 2/3-D numerical electro-thermal modeling and simulation provides a very effective solution of this problem.

In a full 3-D electro-thermal modeling and simulation mode we combined the electro-thermal simulation of diode chip with analysis of the chip packages from a thermal management perspective. The framework required for such analysis is developed and some examples are presented to illustrate its role and effectiveness. [3]

III. Structure and Model Description

The structure under investigation is the P^+NN^+ power diode designed for the reverse voltages up to 1800 V and high forward currents up to 100 A with maximum forward surge current up to 2,7 kA (Fig. 1). Due to the large diode dimensions (9,8 x 9,8 mm) and approximate symmetry of the device only a small part of the structure marked by rectangle was used for standard 2/3-D simulation. But for our methodology for full 3-D electro-physical and advanced thermal analysis we simulated full package. The cathode of the diode is created by diffusion of a highly doped n-type layer (N_d = 2 x 10^{20} cm^{-3}) into the highly resistive (63 Ωcm) n-type substrate layer with thickness of 350 µm. The anode is formed simultaneously by highly doped p-type layer (N_a = 2 x 10^{20} cm^{-3}) on the opposite side of substrate with a pn junction located 290 µm from cathode.

Vertical concentration profile in the centre of analyzed structure corresponding to experimentally fabricated diode is

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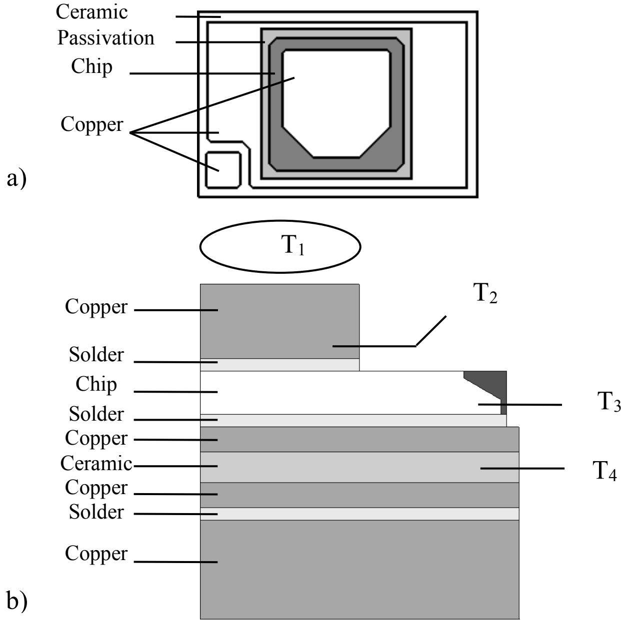

Fig. 1 a) Diode layout, b) Cross-sectional view of chip package

shown in the Fig. 2 a). The measured and simulated *I-V* characteristics are in the Fig. 3 b), c). One can clearly see that a value of average experimentally measured breakdown voltage $V_{BR}^{exp} = 2187$ V differs from simulated value $V_{BR}^{sim} = 1788$ V considerably. To obtain the good correlation of measured and simulated breakdown voltage calibration of used electrophysical models had to be done. For simulation of *I-V* characteristics we used University of Bologna model (UniBo) [7] with default values of carrier lifetime for generation-recombination mechanisms equal to τ_{max} *(electrons)* $= 1 \times 10^{-5}$ s, τ_{max} *(holes)* $= 3 \times 10^{-6}$ s and corresponding value of parameters characterizing Trap Assisted Auger recombination (TAA) $c_n^{TAA} = c_p^{TAA} = 1\times10^{-12}$ cm^3s^{-1} [8, 9]. Instead of default values τ_{max} *(electrons, holes)* $= 1 \times 10^{-3}$ s and $c_{pn}^{TAA} = 1{,}3\times10^{-12}$ cm^3s^{-1} which corresponds to the TAA lifetimes dependent on the carrier densities were used. The doping dependence of the SRH lifetimes was modeled in DESSIS by the Scharfetter relation. *I-V* characteristics simulated with the calibrated parameters fit very well the experimental ones and the $V_{BR}^{sim} = 2161$ V corresponds to experimental value of $V_{BR}^{exp} = 2187$ V within low experimental error.

As the proper thermal modeling plays a significant role in the combined electro-thermal modeling and simulation of power devices the additional metallic and passivation layers were added to perform more realistic heat dissipation from the diode structure. Suitable model of the device structure related to experimental sample was prepared using Synopsis tool Mesh and subsequent electro-thermal simulations were performed by TCAD program [4]. For simulation of power devices the proper thermal management is extremely important. It depends on the good heat dissipation and temperature distribution in the power devices with additional metallic and passivation layers.

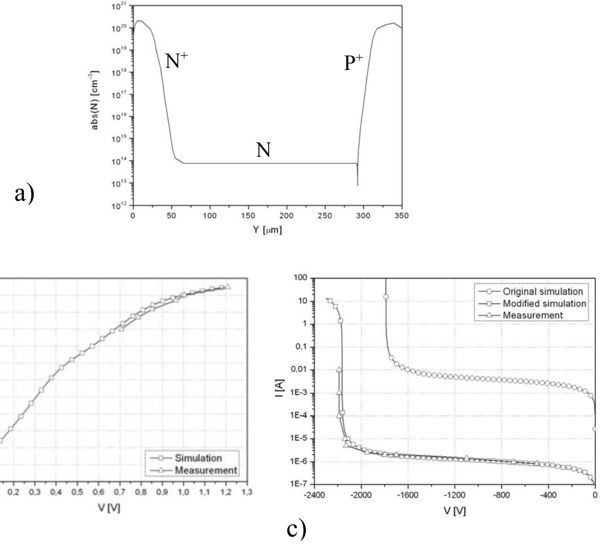

Fig. 2 a) Structure doping profile. Measure and simulation forward (b) and reserve (c) IV curve.

We explore these issues by analyzing chip packages from a thermal management perspective. The methodology required for such analysis and obtained results are illustrated on following examples.

Fig. 1 b) shows a typical chip in package with a simplified thermal resistance network model. For short current pulses up to 10 ms we can assume that the primary heat transfer path through the interface material, spreader and heat sink to the ambient at the top of the structure is of sufficiently low resistance so that any heat dissipation through the secondary path can be neglected due to high thermal resistance of ceramic block. Thus only three thermal resistances are considered: chip-to-copper (R_2), chip-to-DCB (plate Cu-Al_2O_3-Cu) (R_3), and copper-to-ambient (R_1). Both contact and component resistances are included in these quantities. High thermal resistance of metallization and passivation layers and their interfaces prevents the heat dissipation from the chip which subsequently can destroy the diode [5].

IV. Simulation Methodologies

We have created a 3-D complete package of power diodes with an electro-physical complete 3-D model. In order to understand the heating process during surge operation, we performed a 3D simulation. 3D FEM was used to model a 9.8 mm 9.8 mm square chip and a complete package of modules. The aim of the simulation is to show the difference in temperature distribution by selecting different metal materials and different thicknesses as well as changing the chip geometry. To bring locally generated current information on the cell into the electro-physical simulation of the device, a possible solution is the splitting of the single node into several ones, each of them being connected to a single 2-D or 3-D power module [7, 8]. Fig. 3 shows model of the enhanced combined-mode approach.

In our setup, the single node is discretized into three nodes: one is placed on the surface, one fills the light area, and one is located at the interface between contact and silicon. Therefore,

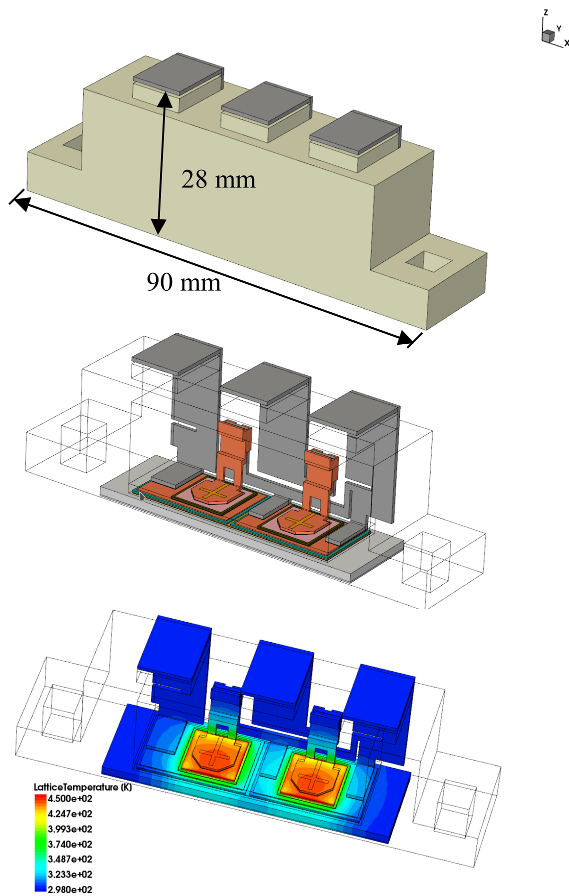

Fig. 3. Simulated temperature distribution for 3100 A puls at time 7.5×10^{-3} s.

the simulation requires solving the drift-diffusion and the Poisson equations in three power module instead of one, and carrier continuity equation is solved in the power module as previously.

In realistic devices, the active area consists of many power chip, which make a full 3-D TCAD approach almost impracticable. A simplified setup can be built to overcome this problem. This solution consists of splitting the full simulation model into a 3-D TCAD model of the package (including die) and a "classical" TCAD description of the device (a "classical" TCAD model here refers to an elementary cell in 2-D or 3-D, depending on the device structure itself). The two parts are connected to each other in "combined-mode" setup. The "classical" TCAD device model is based on a 2-D cross section of a cell. The combined-mode setup is built to allow current density and thermal energy exchange between the package and device via electric and thermal nodes. The package setup includes part of the power module the discrete device package and silicon die.

V. FULL 3-D MODELING

The full 3-D modeling provides accurate results (parameters of power module) and a complex interaction of current distribution on the device electrical behavior. However, such an approach can be applied to the part of structure alone, but it is difficult to apply it to the full system. Building a TCAD model from a complex device design would easily lead to several millions of mesh nodes without even getting a sufficiently accurate grid. To bring local generated current information on the structure into the electro-physical simulation of the device, a possible solution is the splitting of the single node into several ones, each of them being connected to a single 2-D or 3-D structure. The partitioning of the original problem into a multiple mixed-mode approach seems to be the most attractive one, since it couples the accuracy of TCAD simulation of the device embedded into a solar cell and a short simulation time, while preserving information on the non-uniformity of generated current with self-consistent coupling to TCAD elementary devices. For our analysis, we used simulation in mixed-mode setup. FEM Simulations were performed using commercial simulator Synopsys TCAD Sentaurus. Fig. 3 shows the temperature distribution for power diode with additional layer during surge current operation, which reached a peak temperature of 438 K. For simulations without full package model temperature peak position is same for 2-D and 3-D simulations and is located close to the chip edge. But for simulations with included package and contacts two temperature peaks were observed, one in the centre of the chip and second one close to the contact edge. Also, temperature distribution strongly depends on the bottom contact geometry. Critical temperature T = 450 K for analyzed diodes were determined from measurements. The simple diode structure (without passivation and metallic layers) sustain maximum peak current I=1100 A in the dynamic simulation, while the measured maximum peak current was I=2700 A. Thermodynamic physical model with additional layers was used for the simulations analysis of diode structure internal properties during the peak current pulse I=3100 A.

All simulations were performed at the same conditions. With increasing angle of edge termination, the maximum temperature is decreasing. With increasing width and depth of the edge termination profile the temperature rises (Fig. 4). The lowest temperature was observed for a structure with the angle of 60°. While for lower angles minimum temperature of 430 K was obtained for structure with the angle of 60° the temperature reaches a maximum at 429 K for all simulations.

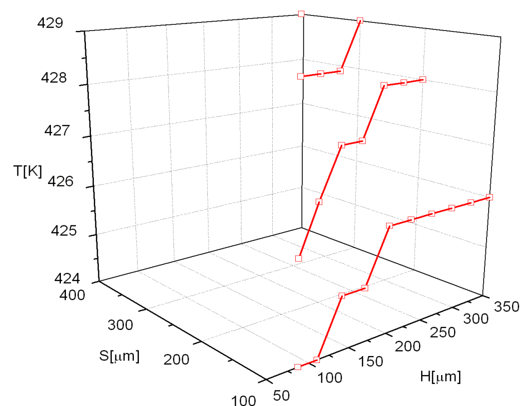

Fig. 4 Max. temperature dependence on height, width and angles 60° of side wall fewer than 3100 A puls at time 7.5×10^{-3} s.

Theoretically, the more dense mesh provides more accurate simulation results. However, practically, a good mesh

is refined sufficiently to provide the required accuracy but not over refined to consume a reasonable simulation time. Example of a test is shown in the Fig. 5 . For total number of mesh nodes $N = 20000$, the simulation result is inaccurate with an error of more than 6.5%. On the other hand, for N more than 100000 nodes, the simulation time becomes too long. Neither of them is considered as a good approach. In this particular case, a good trade-off is achieved with a locally refined mesh with 30000 nodes, which gives a 0.8% error and allows the simulation to finish within 60 minutes of CPU time (Fig. 5). Different modeling approaches already exist, which typically rely on compact models. However, these approaches neglect the spatial nature of the device of the electrical and thermal parameters, which can play an important role in the application. In this paper, a 3-D simulation analysis of the solar cell includes a complete description of the semiconductor structure in terms of thermal profile, and an electro-physical modeling of the device using drift-diffusion transport.

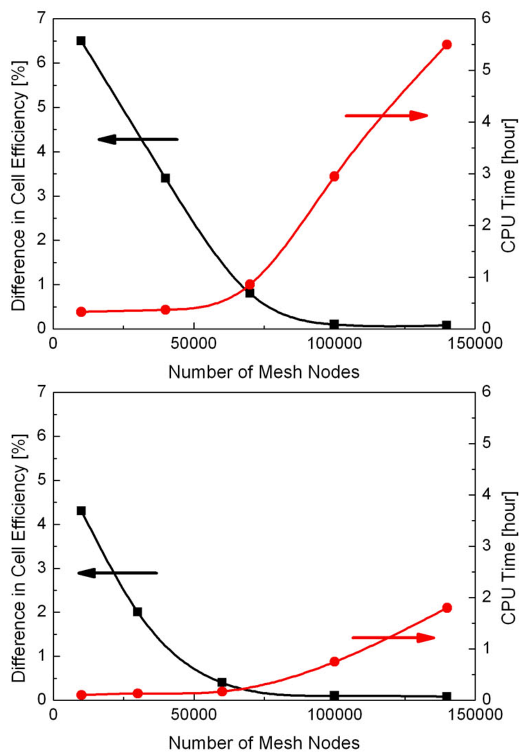

Fig. 5 Simple study on meshing strategies: accuracy versus CPU time trade-off, Top: Full 3-D simulation [8], Bottom: Combined 2-D/3-D

VI. Conclusion

In this paper, TCAD simulations of power modules including accurate modeling of electro-thermal properties were performed. Due to a device complexity many of them cannot be simulated in the full 3-D setup in the reasonable time. Therefore derived solutions based on the combined-mode setup coupling the 3-D TCAD model of the power module to a "classical" TCAD (2-D or 3-D) model of the active device are proposed. The latter methodology provides both good accuracy with respect to full 3-D modeling and short simulation time. The advantages of the proposed method are in the high speed of simulation and simplicity of implementation for complete, high complexity structure analysis. The analysis of thermal and electrical behavior can help during the design and optimization of parameters and geometry from semiconductor layers, metallization, package, and up to full package. The simulation of static breakdown voltage V_{BR} was used for the calibration of model parameters and showed very good correlation with experimental results. Thermodynamic simulation allows analysis of the influence of structure edge termination profile on the electrical properties of analyzed diode. Lowering the diode temperature by structure edge termination shape will allow withstanding the higher current pulses and suppressing the damage of the analyzed structure by thermal breakdown. Finally, the good agreement between simulation, measurement and theoretically computed critical temperature for diode structure confirms the validity of our approach very well.

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