# Performance Evaluation of Ferroelectric MOSFETs based on Gibbs Free Energy

Xiaoyi Zhang[$] and Gengchiau Liang[#]
Department of Electrical and Computer Engineering,
National University of Singapore, Singapore 117583
Email: [$]a0094165@u.nus.edu; [#]elelg@nus.edu.sg

***Abstract*—A comprehensive simulation scheme based on Gibbs free energy calculation is developed to accurately evaluate the device performance of ferroelectric MOSFETs. Its operation region is captured based on the minimum energy point of the whole system involving FE, oxide layer, as well as atomic charge calculation in semiconductor materials. The MOS structure can achieve hysteresis-free mode with negative capacitance effect with both forward and reverse scans. However, for MOSFET structure, the operation region can be affected by different gate lengths of devices and ferroelectric materials. In the selected device, negative capacitance mode can appear with forward scan meanwhile the normal hysteresis effect can appear with reverse scan. This shows hysteresis *I-V* characteristics and non-symmetric operation loop.**

***Keywords— Negative capacitance MOSFETs; ferroelectric material; 3-D Poisson Solver; Gibbs free energy***

## I. Introduction

Power consumption has become the main challenge in highly scaled devices for current CMOS technology. To overcome this issue, negative capacitance effect has been found in ferroelectric (FE) materials theoretically and experimentally which can break the Boltzmann limitation and achieve a steeper subthreshold swing (*SS*) [1-3]. The single layer of FE material has the hysteresis polarization vs. electric field (***P-E***) mode. With parallel connection to a normal capacitor, the negative capacitance effect could be achieved because the Gibbs free energy of the system should be minimized based on Landau theory [4]. The calculation of Gibbs free energy has been discussed for FE capacitor as well as FE- normal dielectric (DE) bilayer capacitor [5]. However, the minimum energy point of the whole MOSFETs system hasn't been investigated in previous studies based on the operation principle of FE material as the gate dielectric of the MOSFET. While the energy of semiconductor channel with atomic charge plays an important role in ultra-scaled devices, it hasn't been involved in the calculation as well. As explained in [6-7], an atomic simulation scheme with full complex bandstructure of device performance evaluation has been developed especially for devices with novel gate dielectric design such as FE-MOSFETs. ***P-E*** relationships of different FE layers got from database or experimental measurement [8-10] based on Landau theory can be involved in the Poisson solver with the proposed simulation scheme.

In this work, unlike previous studies that use simple capacitance model [4-5], we develop a comprehensive scheme for performance evaluation of FE-MOSFETs based on the Gibbs free energy calculation of the complete device. The operation region is obtained based on the lowest point of Gibbs free energy and is able to investigate the performance of FE-MOSFETs more thoroughly. The operation window will change with different gate lengths and FE materials of device, offering the option to customize the FE materials and device structures.

The paper is organized as follows. Section II details the methodologies proposed and device parameters used in our simulations. In Section III-1, the proposed model is used to assess the operation window of MOS structure to validate the idea of negative capacitance effect with Gibbs free energy based on atomic charge system. The operation region and performance of MOSFETs with different gate lengths and ferroelectric materials are calculated and discussed in section III-2. Finally, the conclusions are drawn in Section IV.

## II. Simulation Methodology

The device with the atomic crystal structure of channel materials investigated in this work is shown in Fig. 1(a). The n-channel Si ultra-thin-body (UTB) double gate (DG) FE-MOSFET has 16 atomic layers (2.2 nm). A $V_{DD}$ of 0.6 V and a $SiO_2$ layer with thickness of 1 nm are used in this work. FE layer with thickness of 5 nm is formed on top $SiO_2$ layer and beneath the top gate. The overall simulation procedure is summarized in the block diagram in Fig. 1(b). The potential at each atomic site with its associated atomic charge for entire device structure are self-consistently solved via the Poisson's equation using the finite element method (FEM) in COMSOL [11]. The energy dispersion of the ultrathin Si channel is calculated by the $sp^3d^5s^*$ tight-binding Hamiltonian including the effects of spin-orbit coupling [12]. The surface dangling bonds of Si layer are assumed to be passivated with hydrogen atoms [14]. For charge calculation, each unit cell along transport direction is treated individually using its own Hamiltonian with atomic-potential profile applied on it [6].

This scheme captures the real-space potential under given bias conditions. The current has two components: thermionic current calculated by top of barrier (ToB) model and source to drain (S-D) tunneling current calculated by WKB approximation. With the atomic potential profile, thermionic current and tunneling current based on full real and imaginary band structure are computed independently [6].

The Gibbs free energy of the total system is expressed as the sum of three parts: the energy of the FE layer, the energy of the normal gate dielectric (DE) and semiconductor channel (SEM),

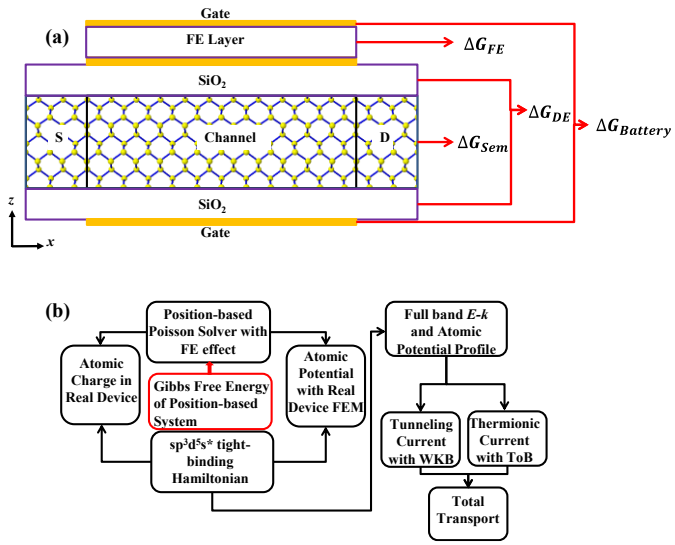


Fig. 1. (a) Cross-sectional view of device structure investigated in this work with atomic channel structure. The components of total Gibbs free energy are also indicated. (b) Procedures of the self-consistently solved atomic device performance simulation. Gibbs free energy calculation is involved in the Poisson Solver.

and the energy of the battery. The semiconductor material has been involved in the calculation with atomic point charge in the meanwhile. Instead of capacitance model used in previous works which discuss the Gibbs free energy calculation of FE devices, real device structure with self-consistently solved atomic charge and potential is investigated in this model. For FE layer, the Gibbs free energy based on Landau-Khalatnikov Equation can be written as

$$\Delta G_{FE} = t_{fe} \cdot (\alpha P^2 + \beta P^4 + \gamma P^6 + \cdots) \cdot A, \quad (1)$$

where $t_{fe}$ is the thickness of FE layer, $\alpha$, $\beta$, and $\gamma$ are the fitting parameters in Landau equation for the FE materials, $P$ is the polarization, and $A$ is the area of FE layer.

For the non-ferroelectric dielectric material and semiconductor material, the Gibbs free energy can be represented as electrostatic energy with constant temperature and pressure. The Gibbs free energy of dielectric layer and Si layer can be calculated as

$$\Delta G_{DE+SEM} = \frac{1}{2}\int D \cdot E dV, \quad (2)$$

where $D$ is the displacement, $E$ is the electric field, and $V$ is the total volume.

Since the device structure has two gates, the battery energy can be expressed as

$$\Delta G_B = -(Q_{TOP} \cdot V_{GTOP} + Q_{BTM} \cdot V_{GBTM}), \quad (3)$$

where $Q_{TOP}$ ($Q_{BTM}$) is the surface charge of top (bottom) gate and $V_{GTOP}$ ($V_{GBTM}$) is the top (bottom) gate voltage.

The total Gibbs free energy of the whole system can be calculated as

$$\Delta G_{TOTAL} = \Delta G_{FE} + \Delta G_{DE+SEM} + \Delta G_B. \quad (4)$$

For capacitance model used in the Gibbs free energy calculation, the polarization (or displacement) is uniformly distributed in the entire FE layer or DE layer. However, the

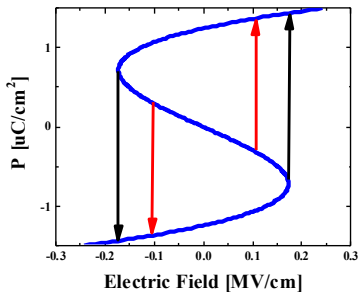


Fig. 2 ***P-E*** relationship of FE material based on Landau theory. The negative *dP/dE* part is unstable in a single FE capacitor. With parallel connection with semiconductor, the negative region will become stable and be used to achieve negative capacitance effect.

polarization related to the electric field is non-uniform for different positions in the FE layer. Because of different potentials and charges in the $SiO_2$ and Si layers, the displacement is non-uniformly distributed in the device. In our solver, the 3-D information can be captured with the discretized device structure associated with the Poisson solver. The total Gibbs free energy is calculated by integrating all the contributions in each discretized block. Therefore, the effect of polarization (or displacement) variation can be integrated in our model. In addition, the effect of atomic charge on the displacement in channel is involved in the Poisson calculation. This effect has never been considered before.

As shown in Fig. 2, the ***P-E*** relationship of P(VDF-TrFE) materials is used in the Poisson solver of device simulation based on Landau theory. The Landau parameters $\alpha$ and $\beta$ is fitted based on minor loop experimental result [9] which shows the negative capacitance effect. In the calculation, the Landau parameters of PVDF are $\alpha = -1.8 \times 10^9$- m/F and $\beta = -5.8 \times 10^{12}$ m$^5$/F/C$^2$. In the figure, the negative *dP/dE* part is unstable in a single FE capacitor (as shown in black arrows). While connected to the normal dielectric material, part or all of the negative curves can become stable as pointed by red arrows based on the minimum Gibbs free energy. The negative capacitance effect will be obtained for device operated in this negative region. For FE-MOSFET, the ***P-E*** relationship based on Landau theory is built in the Poisson solver. The minimum Gibbs free energy of total device system is calculated to determine the operation region of the MOSFET.

## III. Reseult and Discussion

While the calculation of Gibbs free energy has been discussed in prior works [4-5] for FE capacitor as well as FE-DE bilayer capacitor with the simple capacitance model, it is the first time the Gibbs free energy of FE-MOSFET system with real device structure is calculated in this work. The atomic charge in semiconductor channel is involved in the calculation and it is found it can also affect the polarization and energy of the whole system.

### *III-1. Operation region of MOS structure*

Firstly, a MOS structure with three layers (FE, $SiO_2$, and Si layers) has been investigated by calculating the Gibbs free energy of the whole system and obtaining the minimum energy

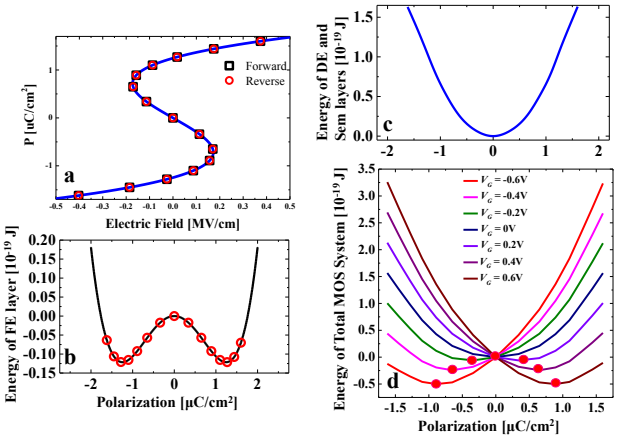


Fig. 3. (a) Operation path for MOS Capacitor with three layers: FE layer, $SiO_2$ layer, and Si layer. For Si layer, the atomic charge has been calculated and involved in the scheme which has the effect on operation region. The gate voltage range is -1.4 : 0.2 :1.4 V. The loop can follow hysteresis-free mode for both direction. Gibbs free energy of the MOS structure: (b) the energy of FE layer (c) the energy of oxide and Si layer (d) the total energy with different gate bias (lowest energy point is indicated in red symbols ).

point. The calculation of atomic charge in Si layer is also involved to get the accurate polarization and energy. Fig. 3a shows the operation path of the MOS in ***P-E*** curve. For both scan directions, the capacitor can operate in the hysteresis-free mode. The negative capacitance effect can be obtained with gate bias of [-0.4 V, 0.4 V]. The operation path can verify the original idea for NC-FET that the unstable negative *dP/dE* path can become stable when FE layer is parallel connected to the normal dielectric material and semiconductor channel. In addition, the relationship of Gibbs free energy vs. *P* is shown in Fig. 3. The energy of FE layer has bi-stable energy while the energy of DE and Si layer has single stable energy. With different gate biases, the position of total minimum energy point will move from negative to positive polarization field (Red point in Fig. 3d). This can match the NC loop in ***P-E*** curve. With $V_G$ in [-0.4 V, 0.4 V] region, the total energy of the system has single energy minimum point and leads to NC mode.

### *III-2. Operation region of MOSFET structure*

Next, the FE-nMOSFET has been investigated with gate length of 6 nm. The operation path in ***P-E*** curve is shown in Fig. 4(a). The average polarization $P_Z$ and electric field $E_Z$ along vertical direction is shown in symbol as reference. When the gate voltage is applied from 0.0 V to 1.2 V, the device will follow the hysteresis-free mode (blue path in Fig.1(c)). However, when we change the scan direction of gate bias from 1.2 V to 0.0 V, the device will follow the normal hysteresis effect loop which has no negative capacitance effect. This is caused by the internal charge from doping and depletion in the channel which change the energy of the whole system. In addition, when gate bias is lower than 1.0 V, the device operates in positive ***P-E*** region which cannot obtain negative capacitance effect as well with forward scan. The $I_D$-$V_G$ characteristics are shown in Fig. 4(b). *SS* of forward and reverse scans are 109 and 107 mV/decade, respectively, which shows the device operated as the normal FE-MOSFET with hysteresis mode especially in OFF-state.

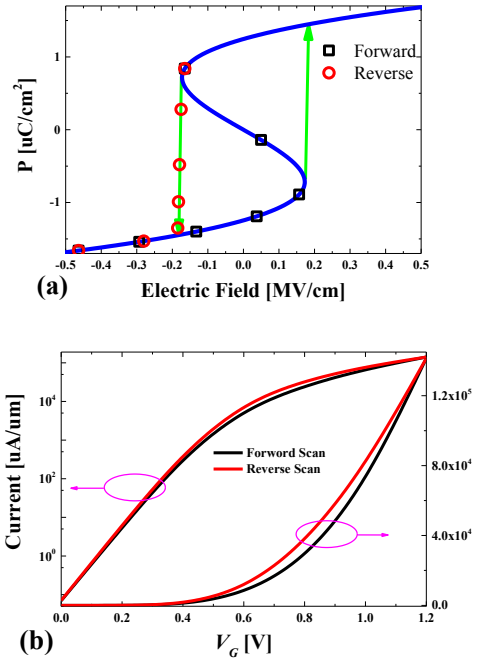


Fig. 4. (a) Operation path for Si nMOSFETs with gate length of 6 nm. (b) $I_D$-$V_G$ characteristics for Si nMOSFETs with gate length of 6 nm. The gate voltage range is 0.0 to 1.2 V.

Furthermore, a FE-nMOSFET with gate length of 14 nm is also investigated in this work. The operation path is shown in Fig. 5(a). When gate length increases to 14 nm, the gate bias range operated in negative capacitance region for forward scan is extended to [0.6V, 1.0V] because of less short channel effects (SCE). The $I_D$-$V_G$ curve is shown in Fig. 5(b). *SS* of forward and reverse scans are 65 and 61 mV/decade, respectively. Since the gate control is better than that of 6 nm, device with 14 nm channel can have a better *SS* for both directions. With steady increase of the gate length, the operation region with OFF-state gate bias can be involved in the negative capacitance curve. However, the device with gate length of less than 10 nm should be investigated for future CMOS technology.

To make the whole operation path in NC region for device with 6 nm channel, MOSFET with FE materials $HfO_2$ is investigated to affect the operation path of the device with forward gate voltage scan from 0.0 to 1.2 V. The Landau parameters used in the calculation fitted from experimental result [13] are $\alpha = -3.7 \times 10^9$ m/F and $\beta = 3.75 \times 10^9 \mathrm{m}^5/\mathrm{F}/\mathrm{C}^2$. As shown in Fig. 6 a and b, devices with PVDF and $HfO_2$ materials can obtain the hysteresis-free mode for forward scan. With a different Landau parameter ($HfO_2$), the operation window can be involved in negative capacitance region of ***P-E*** relationship. The $I_D$-$V_G$ curve of the two devices are shown in Fig. 6 c. The *SS* of MOSFET with $HfO_2$ is 78 mV/decade which is much lower than that of same device with PVDF. In this way, FE materials can be compared and selected to obtain a better device performance.

## IV. Conclusion

In this work, we demonstrated a comprehensive scheme for investigating the device performance of FE-MOSFETs related

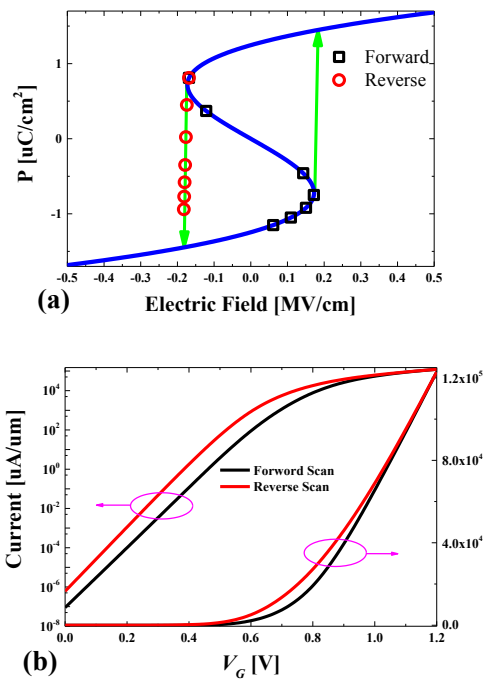


Fig. 5. (a) Operation path for Si nMOSFETs with gate length of 14 nm. (b) $I_D$-$V_G$ characteristics for Si nMOSFETs with gate length of 14 nm. The gate voltage range is 0.0 V to 1.2 V.

to the energy minimum path of Gibbs free energy. The energy of whole device system involving the semiconductor channel with atomic charge calculated. MOS structure can achieve hysteresis-free mode for forward and reverse scans. While in MOSFET structure, the operation paths can be affected by different device parameters based on the total Gibbs free energy of system. Normal hysteresis mode and negative capacitance mode can appear in the same selected device with different scan directions. The operation paths with forward and reverse scan are non-symmetric because of the effect of charge in the semiconductor channel. Moreover, different device structures and FE materials can cause the change of operation window in ***P-E*** curve of the FE layer. Our method is potentially useful for device optimization to get a steep *SS* and reduce power consumption.

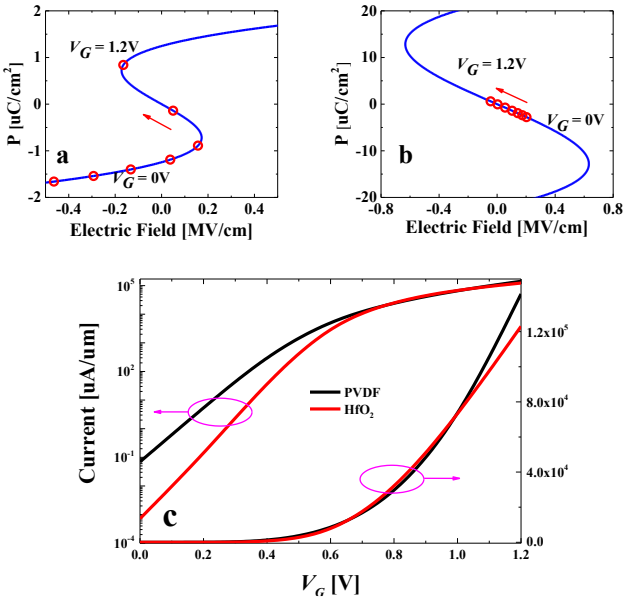


Fig. 6. (a) Operation path for Si nMOSFETs with FE material PVDF. (b) Operation path for Si nMOSFETs with FE material Si doped $HfO_2$. (c) $I_D$-$V_G$ characteristics for Si nMOSFETs with PVDF and $HfO_2$. Gate length = 6nm. Gate bias is applied from 0.0 V to 1.2 V.

## REFERENCES


[1] S. Salahuddin and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices," Nano Lett., vol. 8, no. 2, pp. 405-410, 2008.

[2] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh and S. Salahuddin, "Negative capacitance in a ferroelectric capacitor", Nature Materials, vol. 14, pp 182-186, Dec. 2015.

[3] M. H. Lee, P. -G. Chen, C. Liu, K-Y. Chu, C. -C. Cheng, M. -J. Xie, S. -N. Liu, J. -W. Lee, S. -J. Huang, M. -H. Liao, M. Tang, K. -S. Li and M. -C. Chen, "Prospects for Ferroelectric $HfZrO_x$ FETs with Experimentally CET=0.98nm, $SS_{for}$=42mV/dec, $SS_{rev}$=28mV/dec, Switch-OFF <0.2V, and Hysteresis-Free Strategies," in IEDM, Tech. Dig., pp. 616-619, 2015.

[4] K. Karda, C. Mouli and M. A. Alam, "Switching Dynamics and Hot Atom Damage in Landau Switches", IEEE Electron Device Letters, vol. 37, no. 6, pp. 801-804, June 2016.

[5] K. Majumdar, S. Datta and S. P. Rao, "Revisiting the Theory of Ferroelectric Negative Capacitance", IEEE Trans. Electron Devices, vol. 63, no. 5, pp. 2043-2047, May 2016.

[6] Y. Guo, X. Zhang, K. L. Low, K.-T. Lam, Y. –C. Yeo and G. Liang, "Effect of Body Thickness on the Electrical Performance of Ballistic N-Channel GaSb Double-Gate Ultra-Thin-Body Transistor," IEEE Trans. Electron Device, vol. 62, no. 3, pp. 788-794, Mar. 2015.

[7] X. Zhang, K.-T. Lam, K. L. Low, Y.-C. Yeo and G. Liang, "Nanoscale FETs Simulation Based on Full-Complex-Band Structure and Self-consistently Solved Atomic Potential", IEEE Trans. Electron Devices, vol. 64, no. 1, pp. 58-65, Jan 2017.

[8] J. Jo and C. Shin, "Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/Decade Switching", IEEE Trans. Electron Devices, vol. 37, no. 3, pp. 245-248, Mar. 2016.

[9] A. Rusu, A. M. Ionescu, "Analytical Model for Predicting Subthreshold Slope Improvement versus Negative Swing of S-shape Improvement versus Negative Swing of S-shape Polarization in a Ferroelectric FET", in MIXDES, 2012.

[10] J. Muller, T. S. Boscke, U. Schroder, S. Mueller, D. Brauhaus, U. Bottger, L. Frey and T. Mikolajick, "Ferroelectricity in Simple Binary ZrO2 and HfO2", Nano Lett., vol. 12, no. 8, pp 4318-4323, 2012.

[11] COMSOL, Inc., LiveLink™ for MATLAB User's Guide LiveLink™ for MATLAB® User's Guide.

[12] T. Boykin, G. Klimeck, and F. Oyafuso, "Valence band effective-mass expressions in the $sp^3d^5s^*$ empirical tight-binding model applied to a Si and Ge parametrization," Phys. Rev. B, vol. 69, no. 11, p115201, Mar. 2004.

[13] D. Zhou, Y. Guan, M. Vopson, J. Xu, H. Liang, F. Cao, X. Dong and J. Mueller, "Electric field and temperature scaling of polarization reversal in silicon doped hafnium oxide ferroelectric thin films," Acta Materialia, vol. 99, pp. 240-246, 2015.

[14] K. Alam, S.Takagi, and M. Takenaka, "Analysis and Comparison of L-Valley Transport in GaAs, GaSb, and Ge Ultrathin-Body Ballistic nMOSFETs," IEEE Trans. Electron Devices, vol. 60, no. 12, pp. 4213-4218, 2013.