Evaluation of reconfigurable tunnel FETs for low power and high performance operation

Stefan Blawid*, Denise L.M. de Andrade*, Florian Wolf†, Sven Mothes†‡ and Martin Claus†‡
*Department of Electrical Engineering, Universidade de Brasília, Brazil
†Chair for Electron Devices and Integrated Circuits, Technische Universität Dresden, Germany
‡Center for Advancing Electronics Dresden (Cfaed), Technische Universität Dresden, Germany, Email: martin.claus@tu-dresden.de

***Abstract*—Undoped channel materials and multiple independent gates allow reconfiguration of the transistor operation between n- and p-type behavior. Materials with low effective masses allow in addition to switch on demand between a high-performance (HP) and a low-power (LP) mode, operating the transistor beyond and below the $60\,\mathrm{mV/dec}$ subthreshold slope limit, respectively. Based on $22\,\mathrm{nm}$ double-pattering design rules, a reconfigurable tunnel nanoFET device architecture is proposed, which allows n/p- as well as HP/LP-mode reconfiguration. Important key performance indicators for the technology evaluation at the device level are extracted by means of an augmented drift-diffusion simulator and at the inverter level by means of an empirical compact model.**

***Index Terms*—Reconfiguration, Tunnel FETs, CNTFETs, high-performance, low-power**

I. Introduction

Tunnel (T) field-effect transistors (FETs) circumvent the $S_0 = 60\,\mathrm{mV/dec}$ limit for the subthreshold slope of conventional transistors, as has already been demonstrated experimentally by various groups (e. g. [1]). However, providing the expected currents J per gate width for low-standby power (LP, $10^{-4}\,\mu\mathrm{A}\,\mu\mathrm{m}^{-1}$), for low operating power ($10^{-2}\,\mu\mathrm{A}\,\mu\mathrm{m}^{-1}$) and for high performance operations (HP, $100\,\mu\mathrm{A}\,\mu\mathrm{m}^{-1}$) [2] remains challenging for TFETs. One possible solution would be to reconfigure (R) the transistor's functionality on demand. N/p reconfigurability has been demonstrated for one (1G) [3], two (2G) [4] and three gate (3G) transistors [5]. Interestingly, 3G nanoFETs can also be configured as TFETs by electrostatically doping the source- and drain-sided part of the channel differently, paving the way to LP/HP reconfigurability. Electrostatic doping avoids also chemically or structurally induced traps, which prevents TFETs to operate below the S_0 limit. Here, we evaluate the theoretical performance of a 3G nanoFET based on carbon nanotubes (CNTs). The low effective mass of the charge carriers promises high current levels in TFETs. Moreover, band-to-band tunneling enabling operation below the S_0 limit has already been shown experimentally in CNTFETs [1].

II. Device Design and simulation

The architecture of the suggested RT-nanoFET is based on the 22 nm double-patterning design rules employed in [6]. The device geometry is shown in the inset of Fig. 1. The two programming gates allow a reprogramming of the transistor between n and p as well as LP and HP mode. The slight asymmetric design of the control gate is required to suppress an ambipolar charge flow, which would increase the off current significantly. For the gate insulator a $5\,\mathrm{nm}$ thick $\mathrm{HfO_2}$ layer is assumed. Since the employed $22\,\mathrm{nm}$ design rules limit the minimum distance between the source-sided program gate and the control gate to $20\,\mathrm{nm}$ no further optimization has been attempted, although geometric optimization would improve the device performance. For the chosen moderate channel length of $134\,\mathrm{nm}$, we resort to an augmented drift-diffusion transport model taking into account band-to-band (btb) tunneling. The transport model is self-consistently solved with the 3D Poisson equation. The tunneling probabilities are estimated via the WKB approximation employing fully self-consistent potential barriers. The corresponding numerical solver has been implemented in the in-house multi-scale simulation framework COOS and supplements already existing solvers for the effective-mass Schrödinger [7] and the Boltzmann transport [8] equations, which have been also employed to verify the present approach.

Fig. 1 shows the transfer characteristics for the nLP/nHP and pLP/pHP configurations of the RT-nanoFET. The current can be changed by almost ten orders of magnitude due to the LP/HP reconfigurability. As expected, the HP mode delivers at $(V_\mathrm{G}, V_\mathrm{DS})$ = (0.8 V,0.8 V) a relative high on-current $I_\mathrm{on}^\mathrm{HP} = 1.9\,\mu\mathrm{A/CNT}$ but the transistor cannot be properly switched off due to the S_0 limit. The low sub-threshold slope of the LP mode, however, allows to achieve a much lower off current. The useful range of supply voltages for the control gate ranges from $0.2\,\mathrm{V}$ to $0.4\,\mathrm{V}$, which gives $I_\mathrm{on}/I_\mathrm{off}$ ratios between ten and million, respectively, see Fig. 2. The drain current is carried by a single CNT in the simulated RT-nanoTFET but can be scaled with tube density. For $n_\mathrm{t} = 60\,\mu\mathrm{m}^{-1}$, the current density at $(V_\mathrm{G}, V_\mathrm{DS})$ = (0 V,0.4 V) and (0.4 V,0.4 V) amounts to $J_\mathrm{off}^\mathrm{LP} = 1.6 \times 10^{-8}\,\mu\mathrm{A}\,\mu\mathrm{m}^{-1}$ and $J_\mathrm{on}^\mathrm{LP} = 1.3 \times 10^{-2}\,\mu\mathrm{A}\,\mu\mathrm{m}^{-1}$, respectively. Therefore, the LP mode is well suited for low operating power applications [2].

Fig. 3 reports on the shape of the output characteristics of the HP and LP modes of the evaluated RT-nanoFET. As expected, the LP mode shows S-shaped output characteristics, typical for TFETs. Low bias resistances are therefore considerably higher for the LP than for the HP mode. The characteristic shape difference of $I_\mathrm{D}(V_\mathrm{DS})$ between TFETs and FETs may

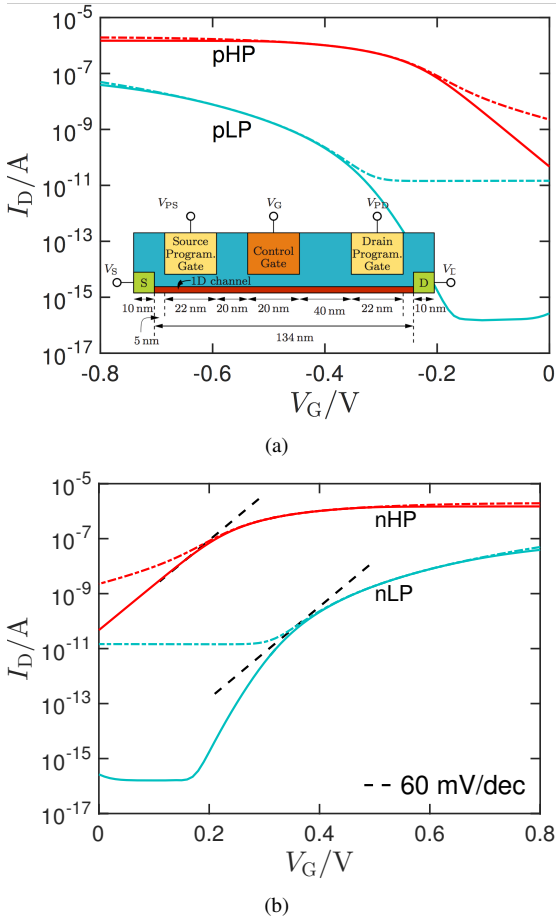

Figure 1. Transfer characteristics at $|V_{DS}| = 0.4\,V$ for the low-power (LP) and high-performance (HP) configurations in **(a)** p-mode and **(b)** n-mode. The dash-dotted lines indicate the drain current at $|V_{DS}| = 0.8\,V$. The 60 mV/dec line serves as guide to the eye. The inset in **(a)** shows the cross-section of the simulated device.

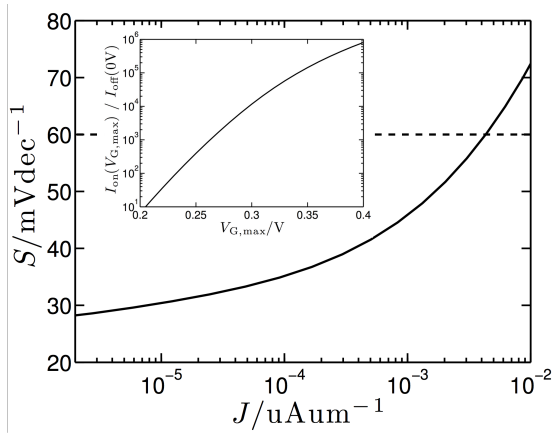

Figure 2. Sub-threshold slope S as function of the current per gate width for a tube density of $60\,\mu m^{-1}$. The inset shows the ratio between the on and off current of the RT-nanoFET in nLP mode. The onset of leakage limits a useful control-gate supply to $V_{G,max} > 0.2\,V$ at $V_{DS} = 0.4\,V$.

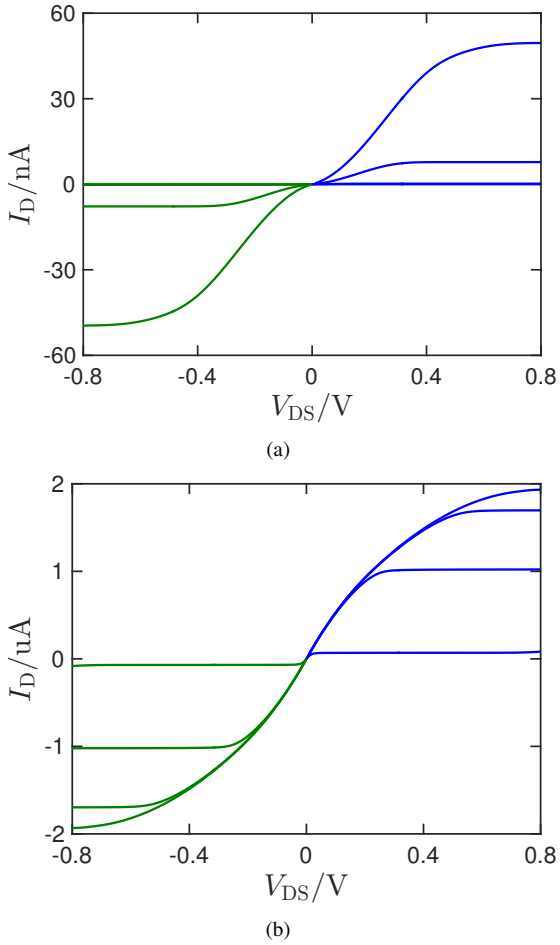

Figure 3. Output characteristics for (**a**) low power and (**b**) high performance mode. Saturation currents increases with the applied gate voltage of $|V_G| = 0.2\,V$, $0.4\,V$, $0.6\,V$ and $0.8\,V$. The HP configurations gives more than ten times higher saturation currents than the LP mode.

be explored for certain application as recently demonstrated for neural networks [9].

Finally, Fig. 4 shows the temperature dependence of the transfer characteristics. Obviously, the off-current, the sub-threshold slope as well as the threshold voltage in HP mode significantly depends on the temperature while in LP mode only the off current increases with increasing temperature.

III. Compact Model and Circuit Evaluation

Reconfigurability on transistor level is an emergent feature of electronic devices based on intrinsic channel materials. The impact on circuit and system level remains to be explored. As a preliminary step, we discuss here important figures-of-merit of a fan-out four (FO4) complementary FET inverter operating in HP and LP mode and employing a supply voltage of $V_{dd} = 0.4\,V$. For the circuit simulation, a compact model is required. Due to the lack of a dedicated model for reconfigurable TFETs, an empirical compact model has been developed based on the virtual source model equations [10] and partially based on the carbon nanotube model from Stanford University [11]. In addition, equations for tube screening

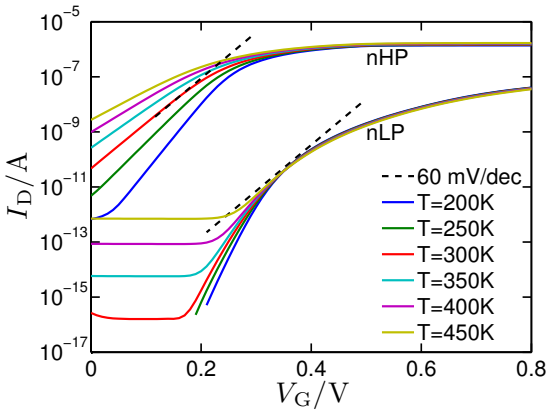

Figure 4. Temperature dependence of the transfer characteristics in LP and HP mode.

effects, S-shaped output characteristics, constant off-currents and mobility degradation have been added. The resulting model is versatile in all regions of operation and sufficiently accurate for the circuit design studies envisioned here.

The model parameters are extracted using the numerical device simulation results at room temperature discussed in Section II. Since the compact model does not provide the ability to switch between the modes of operation, different parameter sets have been extracted for the HP and the LP characteristics. The device architecture is the same for both modes of operation and the parasitic elements have to be extracted only once and remain the same for both employed parameter sets. The parasitic capacitances between the gate, control gates and source/drain contacts are shown in table I. Their values have been calculated using a Poisson solver for the given device structure without the CNT.

Table I
PARASITIC CAPACITANCES.

$C'_{s,ps}$	$C'_{ps,g}$	$C'_{pd,g}$	$C'_{d,pd}$
$0.71\,\mathrm{fF\,\mu m^{-1}}$	$0.28\,\mathrm{fF\,\mu m^{-1}}$	$0.14\,\mathrm{fF\,\mu m^{-1}}$	$0.71\,\mathrm{fF\,\mu m^{-1}}$

Fig. 5 shows a comparison between the numerical device and the compact model simulations of the transfer and output characteristics of the RT-nanoFET configured in nHP mode. A good agreement between compact model and device simulation has been achieved except for the drain-voltage dependent subthreshold slope at high V_{ds}. However, an accurate modeling for large V_{ds} is not required in the present study, since we evaluate only the FO4 inverter with a supply voltage of $V_{dd} = 0.4\,V$. For the LP-operation a separate parameter set has been extracted. A comparison between compact model and device simulation results are shown in Fig. 6. The S-shape of the output characteristic at small V_{ds} is nicely captured by the compact model, which is essential for a correct estimation of the delay times of digital benchmark circuits. However, the non-exponential gate voltage dependence of the subthreshold current is not well represented by the empirical model and needs to be refined in the future.

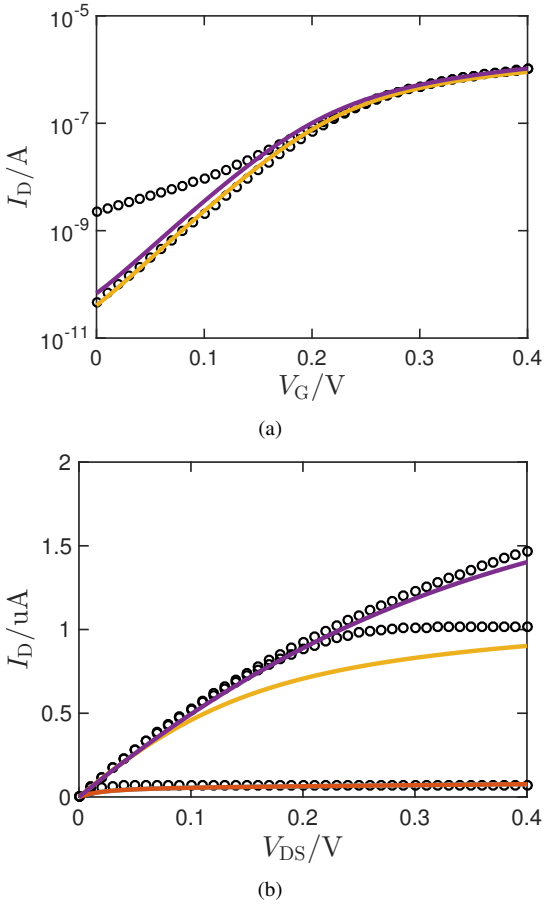

Figure 5. Comparison between the numerical device simulation results (symbols) and the compact model (solid line) for a single tube RT-FET in *nHP-mode*: (**a**) transfer characteristic for $V_{DS} = 0.4\,V$ and $0.8\,V$; (**b**) output characteristic for $V_{GS} = 0.2\,V$, $0.4\,V$ and $0.6\,V$.

Based on the calibrated compact model, some key figures-of-merit (FOMs) (see Tab. II) for the FO4 inverter are calculated assuming the same width of $W = 1\,\mu m$ for both transistors. A schematic representation of the inverter operating in LP and HP mode is shown in Fig. 7.

Table II
INVERTER FIGURES OF MERIT. VALUES IN BRACKETS REPRESENT ANALYTIC ESTIMATES.

n_t	FOM	LP	HP
60 tubes/µm	P_{DC}	4.8 fW (6.4 fW)	783 pW (1100 pW)
	E_{dyn}	0.59 fJ (0.53 fJ)	0.63 fJ (0.53 fJ)
	$t_{r/f}$	243 ns (100 ns)	44.7 ps (35 ps)
200 tubes/µm	P_{DC}	16 fW (21 fW)	1640 pW (3800 pW)
	E_{dyn}	0.61 fJ (0.53 fJ)	0.65 fJ (0.53 fJ)
	$t_{r/f}$	142 ns (30 ns)	24.5 ps (10 ps)

The determined FOMs agree reasonably well with simple analytic estimations: (i) The static power consumption amounts to $P_S = V_{dd} I_{off}$, (ii) the dissipated energy by once charging and discharging an external capacitive FO4 load C_L equals $E_L = C_L V_{dd}^2$ and (iii) the rise and fall time of the

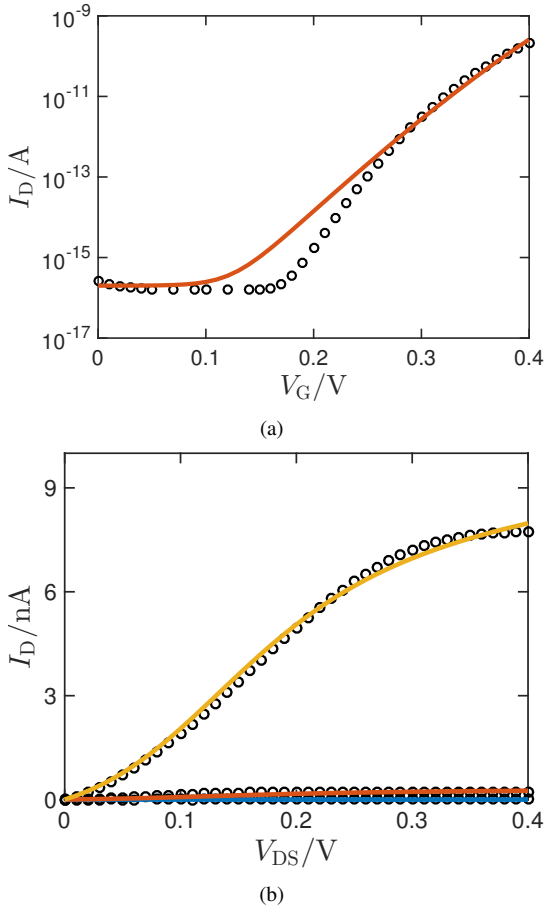

Figure 6. Comparison between the numerical device simulation results (symbols) and the compact model (solid line) for a single tube RT-FET in *nLP-mode*: (**a**) transfer characteristic for $V_{\mathrm{DS}} = 0.4\,\mathrm{V}$; (**b**) output characteristic for $V_{\mathrm{GS}} = 0.2\,\mathrm{V}$, $0.4\,\mathrm{V}$ and $0.6\,\mathrm{V}$.

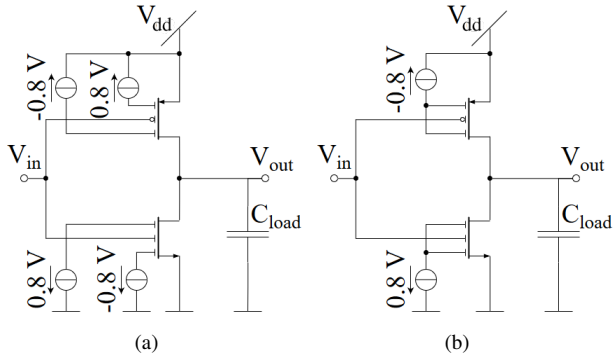

Figure 7. Schematic of the inverter in (**a**) LP-mode and (**b**) HP-mode configuration.

FO4 inverter can be estimated as $t_{\mathrm{r/f}} \approx 3\,R_{\mathrm{on}}\,C_{\mathrm{L}}$, where R_{on} is the output resistance in the linear regime at $V_{\mathrm{G}} = V_{\mathrm{dd}}$. The corresponding values are given in brackets in Tab. II. The analytic estimate of P_{dyn} neglects the internal power consumption of the inverter, which appears to be justified. Note that the compact model predicts non-linear n_{t} scaling due to internal screening and capacitance effects.

In HP mode, delay times of tenth of picoseconds are predicted. When reconfiguring the FO4 inverter from HP to LP mode, the static power consumption P_{DC} decreases significantly, whereas the dynamically consumed power P_{dyn} only changes marginally. As the operation frequency is strongly reduced for the LP TFET and the switching process occurs less often, the overall consumed energy of the inverter operating in low-power mode is drastically reduced.

IV. Conclusion

The theoretical performance of a reconfigurable nanoFET based on intrinsic carbon nanotubes (CNTs) with two programming and one control gate has been evaluated at the transistor and the inverter level. Electrostatic doping, avoiding chemically or structurally induced traps, and the low effective mass of the charge carriers enable low power and high performance configurations of the transistor. For low power consumption, the transistor operates below the $60\,\mathrm{mV/dec}$ subthreshold limit of conventional transistors, but on demand the current can be increased by almost ten orders of magnitude.

V. Acknowledgment

This project is partially supported by the German National Science Foundation DFG (CL384/2-2).

References

[1] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Physical Review Letters*, vol. 93, p. 196805, 2004.

[2] W. G. Vandenberghe, A. S. Verhulst, B. Sorée, W. Magnus, G. Groeseneken, Q. Smets, M. Heyns, and M. V. Fischetti, "Figure of merit for and identification of sub 60mV/decade devices," *Appl. Phys. Lett.*, vol. 102, pp. 013510–5, Jan. 2013.

[3] G. Darbandy, M. Claus, and M. Schröter, "High-performance reconfigurable si nanowire field-effect transistor based on simplified device design," *IEEE Transactions on Nanotechnology*, vol. 15, pp. 289–294, March 2016.

[4] S. Glassner, C. Zeiner, P. Periwal, T. Baron, E. Bertagnolli, and A. Lugstein, "Multimode silicon nanowire transistors," *Nano Letters*, vol. 14, pp. 6699–6703, nov 2014.

[5] M. Mongillo, P. Spathis, G. Katsaros, P. Gentile, and S. De Franceschi, "Multifunctional Devices and Logic Gates With Undoped Silicon Nanowires," *Nano Lett*, vol. 12, pp. 3074–3079, June 2012.

[6] R. Carter *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, pp. 2.2.1–2.2.4, Global Foundries, Germany, Dresden, Germany, IEEE, 2016.

[7] M. Claus, S. Mothes, S. Blawid, and M. Schröter, "COOS – A wavefunction based Schrödinger-Poisson solver for ballistic nanotube transistors," *Journal of Computational Electronics*, vol. 13, no. 2, pp. 689–700, 2014.

[8] S. Mothes, M. Claus, and M. Schroter, "Toward linearity in schottky barrier cntfets," *IEEE Transactions on Nanotechnology*, vol. 14, pp. 372–378, March 2015.

[9] B. Sedighi, X. S. Hu, J. J. Nahas, and M. Niemier, "Nontraditional computation using beyond-CMOS tunneling devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, pp. 438–449, dec 2014.

[10] A. Khakifirooz, O. Nayfeh, and D. Antoniadis, "A simple semiempirical short-channel mosfet current voltage model continuous across all regions of operation and employing only physical parameters," *Electron Devices, IEEE Transactions on*, vol. 56, pp. 1674–1680, Aug 2009.

[11] C. S. Lee, E. Pop, A. D. Franklin, W. Haensch, and H. S. P. Wong, "A compact virtual-source model for carbon nanotube fets in the sub-10-nm regime; part i: Intrinsic elements," *IEEE Transactions on Electron Devices*, vol. 62, pp. 3061–3069, Sept 2015.