Analysis of Neutron-induced Soft Error Rates on 28nm FD-SOI and 22nm FinFET Latches by the PHITS-TCAD Simulation System

Jun Furuta, Shigehiro Umehara and Kazutoshi Kobayashi
Graduate School of Science & Technology, Kyoto Institute of Technology

Abstract— **FinFET and FD-SOI processes reduce radiation-induced temporal errors and improve circuit reliability without any performance overhead. We calculate neutron-induced SEU (Single Event Upset) rates on 28nm FD-SOI and 22nm FinFET Flip-Flops by using TCAD and PHITS in order to compare SEU rates in advanced planar and 3D transistor processes. Simulation results show that SEU rate on 22nm FinFET is about 1/10 that on 28nm FD-SOI.**

I. Introduction

Leakage current by the short-channel effect is critical for the process scaling in the planar bulk processes. To reduce leakage current, FD-SOI transistors and FinFET are used in advanced process nodes. These transistors have higher level of gate control over the channel, reduce parasitic capacitance by depletion layer and improve drive current and sub-threshold slope. In addition, these transistors also have higher immunity against radiation-induced temporal errors than conventional bulk planar transistors [1]. In bulk process, radiation-induced temporal errors on sequential elements are increased by process scaling and radiation-hardened designs must be prepared for supercomputers, cloud servers and driving systems [2]. In FinFET and FD-SOI processes, conventional radiation-hardened design methodologies become excess protection with huge performance overhead for circuit reliability. To effectively improve reliability, error rates on a FinFET and a FD-SOI processes need to be calculated accurately.

In this paper, we calculate neutron-induced temporal error rates in a 28nm FD-SOI latch and a 22nm FinFET latch by using TCAD and PHITS simulation tools to compare radiation immunity in the terrestrial environment. In our simulation framework, secondary-ion production by nuclear reactions is simulated by PHITS, while ionizing effects by secondary ions are calculated by TCAD. This paper is organized as follows. Section II explains mechanism of radiation-induced temporal errors. Section III introduce PHITS-TCAD simulation system for evaluating neutron-induced soft error rate. Section IV shows simulation results and Section V concludes this paper.

II. Radiation Effects on Bulk, FinFET and FD-SOI Processes

When a charged particle passes through semiconductor, a huge number of electron-hole pairs are generated along its track. In an nMOS bulk transistor, generated electrons are collected to diffusion area by funneling, drift and diffusion as shown in Fig. 1. Thus, its output is transiently flipped by a

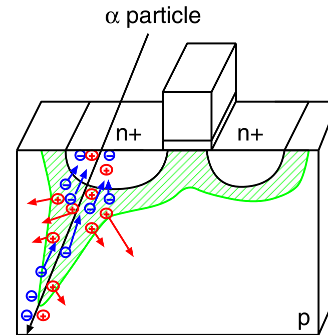

Fig. 1. Radiation effects on a bulk transistor.

charged particle. A stored value in a sequential element have possibility to be flipped when a particle pass through it. The radiation-induced temporal data flip is called single event upset (SEU) and radiation-induced malfunction is called soft error. Soft error rates on bulk processes are increased by process scaling since the number of sequential elements is increased exponentially [3].

In FinFET, the number of collected electrons and probability of radiation strike is smaller than in bulk because of small PN junction area in a FinFET structure. In contrast, the FD-SOI transistor has no PN junction between diffusion area and substrate. Charge collection is extremely suppressed by buried oxide layer. However, a parasitic bipolar turn on by a radiation strike and collected charge is increased because of floating body layer (back-gate node). As a result, soft error rate is reduced in FinFET and FD-SOI processes, but soft error cannot be ignored in highly-reliable systems.

In the ground level, soft errors are caused by α particles emitted from package material and neutrons generated in the atmosphere by cosmic rays [4]. Since neutron is not a charged particle, electron-hole pairs are deposited through a neutron collision with silicon atom which generates secondary ions. To calculate neutron-induced SEU rate and estimate soft error rate in the ground level, device simulation and nuclear reaction simulation are required.

III. Neutron-induced Soft Error Simulation

A. PHITS-TCAD Simulation

Fig. 2 shows mechanism of neutron-induced temporal error occurrence. Secondary ions provided by nuclear reaction between neutron and silicon generate electron-hole pairs that charge or discharge a circuit node. In TCAD simulation, electrical effects by charged particles and electrical behavior

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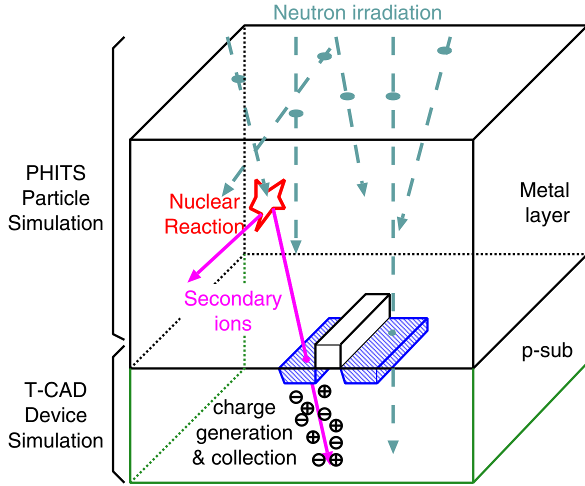

Fig. 2. Device structures for PHITS particle and TCAD device simulations

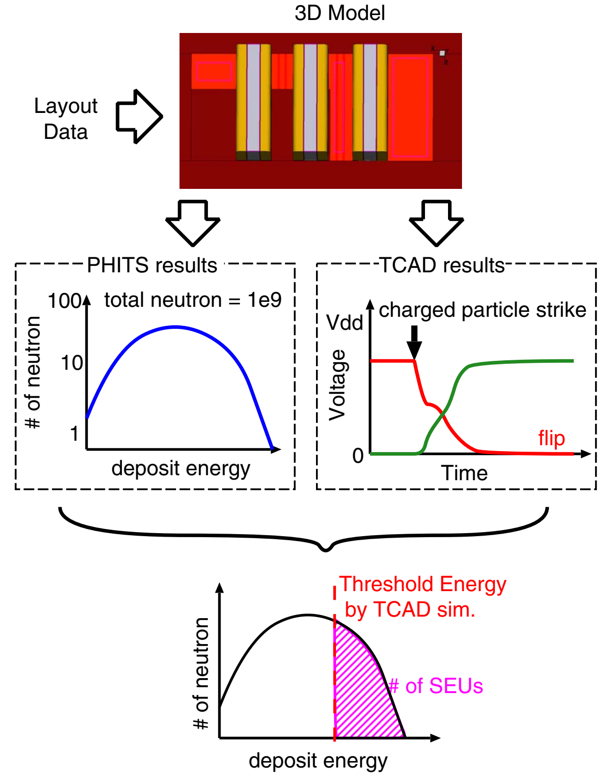

Fig. 3. Flow chart of PHITS-TCAD simulation system.

of semiconductor devices are only simulated. Thus neutron-induced SEUs are not directly evaluated. The probability of nuclear reaction, species of provided secondary ions, energies and directions are calculated by Monte Carlo particle transport simulation code, named PHITS [5]. Deposited energy by secondary ions in user-defined regions is also calculated by PHITS, which indicates the amount of electron-hole pairs. Fig. 3 shows the flow chart of the PHITS-TCAD simulation system [6]. The probability of nuclear reaction and deposited energy (charge) distribution are calculated by PHITS simulation. TCAD simulation calculate threshold charge on a latch, which is the minimum charge that can flip a stored value. Then we obtain the ratio of neutrons that cause SEUs on the latch and SEU rates on the terrestrial environment.

B. Simulation Setup

In 3D device models, transistor dimensions of a 28 nm FD-SOI and a 22 nm FinFET are defined by referring to [7], [8]. The Id-Vg characteristics of these transistors are almost equivalent by controlling doping parameters and gate work functions in TCAD simulations. Our 3D device models do not have metal layers and vias in order to reduce simulation time. Therefore, parasitic capacitance and resistance are not considered in this simulation. Since n-type transistors are more sensitive to radiation effect than p-type transistors, we only show simulation results when a particle pass through channel region of target n-type transistors.

In PHITS simulation, the total number of irradiated neutrons is 10^{10} and all neutrons are perpendicularly incident. Energy spectra of irradiated neutrons is consisted with that at ground level of New York.

C. Definition of Sensitive Volume

The distribution of deposited energy strongly depends on the size of a user-defined region. The user-defined region should conform to the sensitive volume where deposited charge is collected to the drain region entirely. The sensitive volume of FD-SOI is almost equivalent to the body (channel) region since the buried oxide layer intercept deposited charge in the substrate. In contrast, that of FinFET on bulk substrate collects deposited charge from the substrate. The amount of the deposited charge on FinFET Latch depends on sensitive volume. We evaluate the depth of the sensitive volume by TCAD simulations.

To evaluate sensitive volume, charged particles are horizontally incident to a FinFET and particle-induced currents are calculated by TCAD simulations. Incident positions (P_i) are changed with 0 – 100 nm below the top of the channel as shown in Fig. 4. Fig. 5 shows simulation results of particle-induced currents for all incident positions. At P_i = 30 nm, particle-induced current has the highest peak. It is because generated charge density has a spatial Gaussian distribution with standard deviation (σ) of 30 nm [9]. In contrast, the peak amount of current reduced to less than 60% at $P_i > 60$ nm. Therefore, we define the depth of the sensitive volume in FinFET as 60 nm.

IV. Simulation Results

Fig. 6 shows simulation results of threshold LET (linear energy transfer) by TCAD simulation. Threshold LET can be converted to threshold charge or energy. Threshold LETs are almost linearly increased according to supply voltage but the difference between the 28nm FD-SOI and the 22nm FinFET become smaller at higher supply voltage. Figs. 7 and 8 show threshold LET depending on body bias on the 28nm FD-SOI and the 22m FinFET, respectively. Note that all results

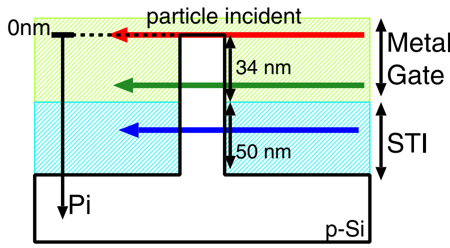

Fig. 4. TCAD simulation to evaluate sensitive volume in FinFET.

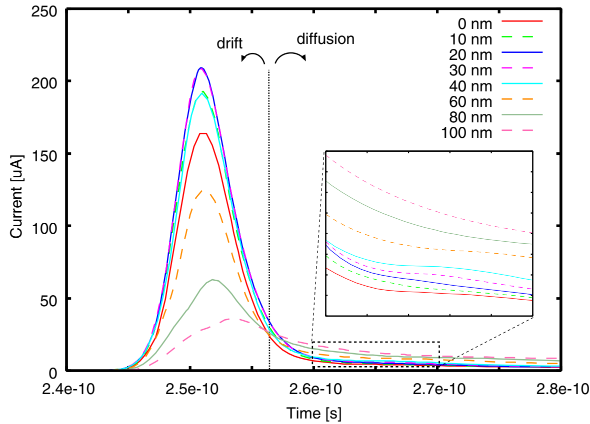

Fig. 5. TCAD simulation results of current caused by charged particle which is incident horizontally.

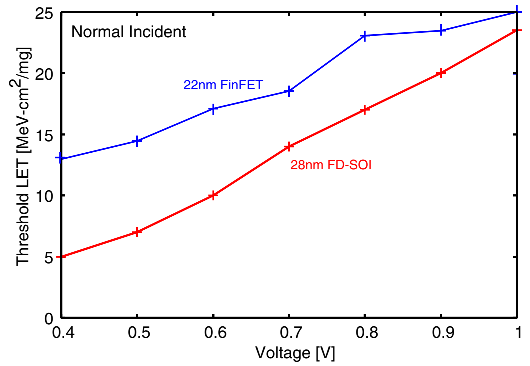

Fig. 6. Simulation results of threshold LET on 28nm FD-SOI and 22nm FinFET by TCAD simulation.

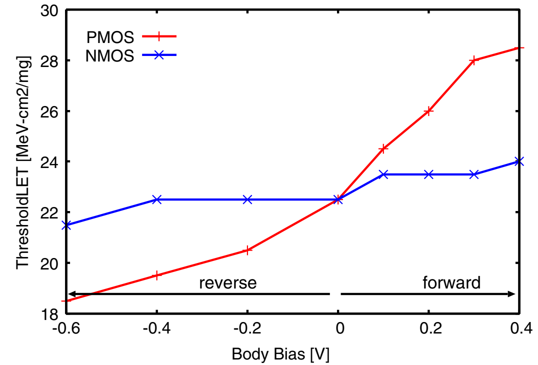

Fig. 7. Simulation results of threshold LET depending on body bias on 28nm FD-SOI.

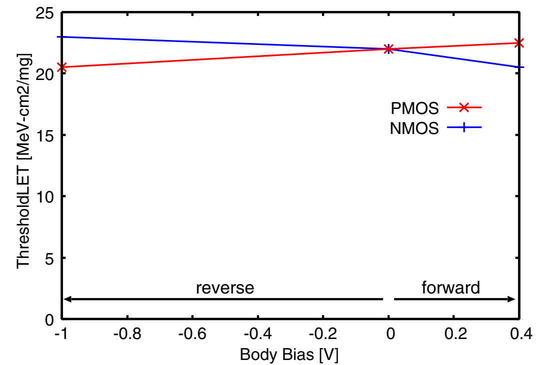

Fig. 8. Simulation results of threshold LET depending on body bias on 22nm FinFET.

shows threshold LET when a charged particle pass through an nMOS transistor. Compared with supply voltage, body bias does not affect threshold LETs. It is because threshold voltages of FD-SOI and FinFET does not depends on body bias because of their structure.

Fig. 9 shows SEU rates of latches on 28nm and 22nm by changing supply voltages calculated by PHITS=TCAD system. SEU rates exponentially increase. SEU rate of the FD-SOI latch is about 10 times bigger that of the FinFET latch at 0.8 V, although the difference of threshold LET is the smallest value at VDD = 1.0 V. It is because the area of the sensitive volume projected from the normal incident angle is 1/13 in the FD-SOI than in the FinFET.

V. Conclusion

We calculate neutron-induced SEU rates on the 28nm FD-SOI and the 22nm FinFET Flip-Flops by using TCAD and PHITS simulations. Simulation results show that SEU rates on 22nm FinFET is about 1/10 that in 28nm FD-SOI when supply voltage is 0.4 – 1.0 V. It is because 22nm FinFET has the high LET immunity and the area of the sensitive volume projected from the normal incident angle is 1/13 than in the FinFET.

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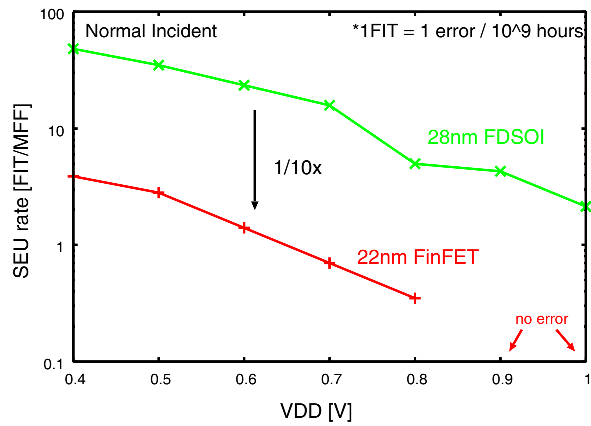

Fig. 9. Neutron-induced SEU rates on 28nm FD-SOI and 22nm FinFET by the PHITS-TCAD system.

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