# A SPICE-compatible model of SG-MONOS for 28nm flash macro design considering the parasitic resistance caused by trapped charges

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***Abstract*— A SPICE-compatible model for the read current of split-gate MONOS (SG-MONOS) cell has been developed for 28nm embedded flash macro design. The influence of trapped charges on the read current has been analyzed by using TCAD. It has been found that trapped charges located on top of the gap region strongly decrease the cell current. It has been also found that the shape of $I_d$-$V_{sg}$ curve changes drastically depending on the positon of trapped charge and trap density. This paper proposes a new model which reproduces the above behavior by using a synthesis of several resistances in which every resistance changes its value exponentially to the gate voltage. The model shows an excellent fitting accuracy for 28nm generation cell.**

***Keywords—SPICE; compact model; MONOS; Split-gate; flash***

## I. INTRODUCTION

SG-MONOS is an attractive flash memory cell structure since it provides a high-speed operation, a low power operation, and a long retention [1-4]. In this work, we report a spice-compatible model of SG-MONOS cell read currents which is required for designing circuits of SG-MONOS memories.

Although elaborated SPICE-compatible models for floating split-gate cells have already been published [5-7], the SG-MONOS has not fully modeled yet. A gap resistance which is modified by trapped charges is an issue for modeling such a split-gate charge-trap memory. This paper reports a novel model for the SG-MONOS cell in which a gap resistance is approximated by a synthesis of several resistances whose value are exponentially depending on the select gate voltage. The model has been verified by using measurements of read current of 28nm generation SG-MONOS cell. The proposed model accurately reproduces the cell current in all conditions.

## II. DEVICE STRUCTURE AND THE GOAL OF MODELING

Fig. 1 shows the device structure of SG-MONOS cell [1-4]. A charge trapping layer are placed under the memory gate (MG). In the program condition, electrons are injected to the charge trapped layer (Fig. 2(c)). This makes the threshold voltage of MG transistor high. A datum "0" is stored in this condition. In the erase condition, the trapped electrons are erased and the threshold voltage of MG transistor becomes low

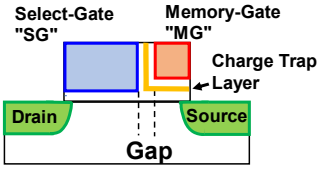


**Fig. 1** The device structure of Split-Gate (SG) MONOS cell.

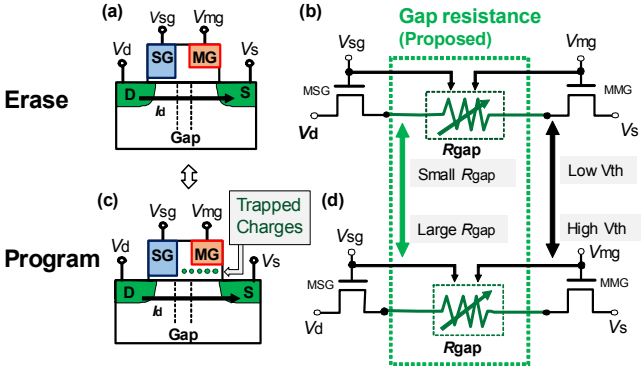


**Fig. 2** The strategy of SG-MONOS read current modeling. $R_{gap}$ is the gap resistance whose value is dependent on $V_{sg}$ and $V_{mg}$. $R_{gap}$ also changes between the program condition model and the erase condition model.

(Fig. 2(a)). This is the condition that a datum "1" is stored. A select-gate (SG) transistor operates as a cell selector. A gap is located between SG and MG. The gap region is not covered by any electrodes.

SPICE models which reproduce the cell currents are required both for the erase condition and program condition. Basic method to obtain the two models for split gate memories is to change the threshold voltage parameter of MG transistor. However, the approach cannot reproduce the influence of parasitic resistance in the gap region of SG-MONOS cell ($R_{gap}$ in Fig. 2). The parasitic resistance strongly affects the cell current especially in the program condition in which trapped charges exist. In addition, the effect becomes significant as the cell is miniaturized. The purpose of this paper is to develop a cell model for SG-MONOS which can reproduce not only the influence of the threshold voltage variation of MG transistor, but also the influence of the parasitic resistance variation due to the change in the trapped charge density, as shown in Fig. 2.

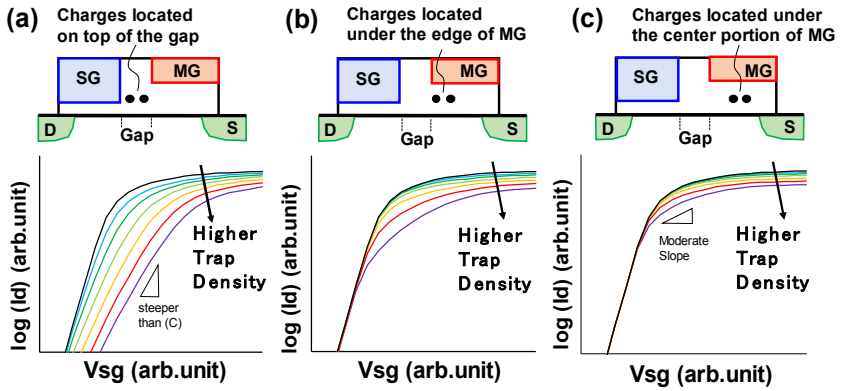


**Fig. 3** Simulated $I_d$-$V_{sg}$ characteristics obtained from TCAD.

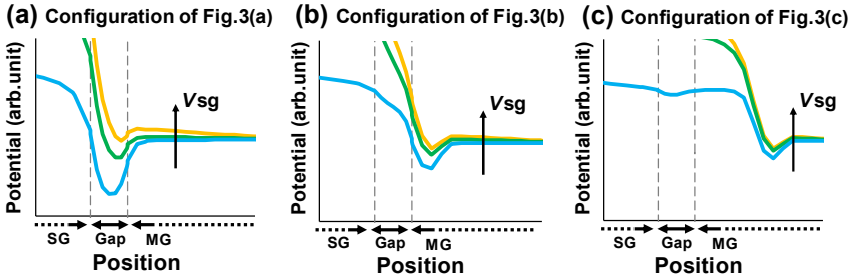


**Fig. 4** The horizontal potential distribution at the silicon surface obtained from TCAD. (a), (b), and (c) are plotted for configurations shown in Fig. 3(a), (b), and (c), respectively. Potential distributions for the highest trap density in Fig. 3 are shown.

## III. TCAD Analysis to Find Modeling Strategy

The influence of trapped charge on the drain current is analyzed by using TCAD. Simplified device structures with a constant doping and abrupt junctions are assumed, since the purpose of TCAD simulation is to obtain a qualitative insight. Fig. 3 shows simulated result of the drain current ($I_d$) dependences on the select gate voltage ($V_{sg}$). In the structure (a), trapped charges are located over the gap region. The charges are located under the edge of MG in (b), and the charges are located under the center portion of MG in (c).

The influence of trapped charge density on the $I_d$-$V_{sg}$ curve is significant in the arrangement of Fig. 3(a). The drain current decreases and the subthreshold slope becomes moderate as the trap density increases. In the case (c), no changes in the subthreshold current are observed. The $I_d$-$V_{sg}$ curve of case (c) suggests that the main reason for the $I_d$ degradation in the case is due to the change in the channel resistance of MG transistor which is serially connected with SG. However, the $I_d$-$V_{sg}$ curve of case (c) does not resemble the measurements (see Fig. 9 (b)). The result for case (b) shows an intermediate behavior between Fig. 3(a) and (c).

Fig.4 shows the horizontal electric potential distribution at the silicon surface. Fig. 4 (a), (b), and (c) are plotted for configurations shown in Fig. 3 (a), (b), and (c), respectively. The potential distributions for the highest trap density in Fig. 3 are plotted in the figure. One can see that a large potential dip appears in the Fig. 4 (a). This shows a large parasitic resistance exists in the gap region. Fig. 5(a) shows the potential dependence on $V_{sg}$ at silicon surface for the configuration of

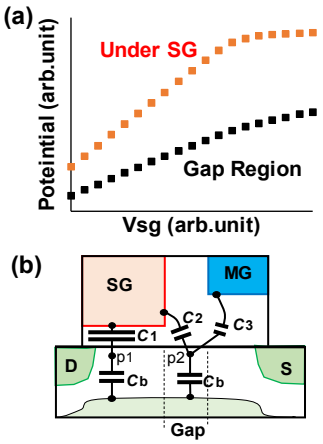


**Fig. 5** (a) Potential dependence on $V_{sg}$ at silicon surface. The results are shown for the highest trap density configuration of Fig. 3(a). (b) Virtual capacitance networks to explain the difference between two slopes in Fig. 5(a).

Fig. 3(a). The electric potential at the gap region are compared with that under the select gate. The result shows that the sensitivity of surface potential to $V_{sg}$ at the gap region is weaker than that under SG. This behavior can be explained by virtual capacitance networks shown in Fig. 5(b). The gap region has electrostatic coupling with SG (shown by $C_2$). However, the influence of $V_{sg}$ on the electric potential of gap region is small, since the capacitive coupling at the gap region ($C_2$) is smaller than that under SG ($C_1$) and the coupling capacitance with MG ($C_3$) exists in the gap region.

## IV. Model Configuration and Parameter Fitting

Fig. 3 suggests that the shape of $I_d$-$V_{sg}$ curve is dependent on the spatial distribution of trap density. However, it is difficult to know the actual distribution of trapped charges, and it is also difficult to include an actual spatial distribution in the model equation even if the distribution is found.

Therefore, an approximation has been developed based on the analysis discussed in the section III. Fig. 6(a) shows the proposed macro model configuration for SG-MONOS Cell. $R_{gap}$ is approximated by a composition of three variable resistances $R_1$, $R_2$, and $R_3$. SG and MG transistors are modeled by using BSIM4. $R_{gap}$ is expressed as in (1) and (2), by using coefficients $A_n$ which are functions of memory gate voltage ($V_{mg}$) and temperature. $B_n$ and $C_n$ in (2) are fitting parameters determined at a reference $V_{mg}$ and a reference temperature.

$$R_{gap} = \sum_{n=1}^{3} R_n \quad (1)$$

$$R_n = A_n \exp(B_n V_{sg} + C_n) \quad (2)$$

The relations among the three resistances $R_1$, $R_2$, and $R_3$ are shown in Fig. 6(b). $R_2$ has a weaker dependence on $V_{sg}$ than $R_1$ does, and $R_3$ has a weaker dependence on $V_{sg}$ than $R_2$ does. The parasitic resistance dependence on $V_{sg}$ in an actual device is approximated by a synthesis of the three resistances.

Fig. 7 shows the modeled $R_{gap}$ for program condition. The configuration shown in Fig. 6 is used. The coefficients for $R_1$, $R_2$, and $R_3$ have been determined from measured cell currents. $R_{gap}$ dependence on $V_{sg}$, that on $V_{mg}$, and that on temperature are included in the model.

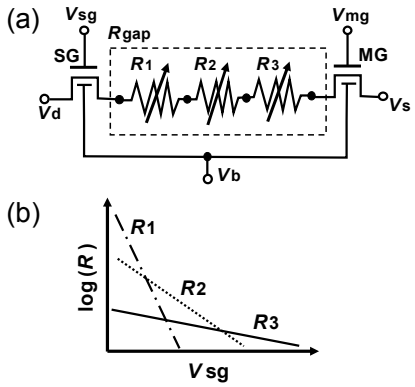


**Fig. 6** Proposed macro model for SG-MONOS Cell. (a) Model configuration. (b) The relation among the value of three variable resistances $R_1$, $R_2$, and $R_3$. The parasitic resistance of the device ($R_{gap}$) is approximated by a composition of $R_1$, $R_2$, and $R_3$. SG transistor and MG transistor are modeled by using BSIM4.

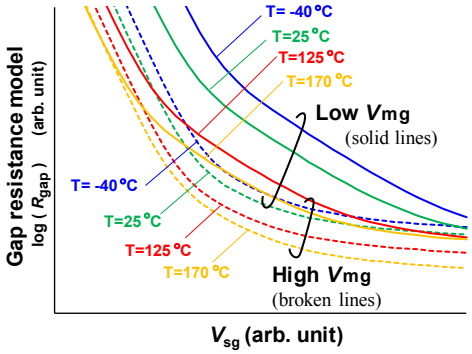


**Fig. 7** The parasitic resistance for the program condition given by sum of $R_1$, $R_2$, and $R_3$. The coefficients for these variable resistances have been extracted from measurements.

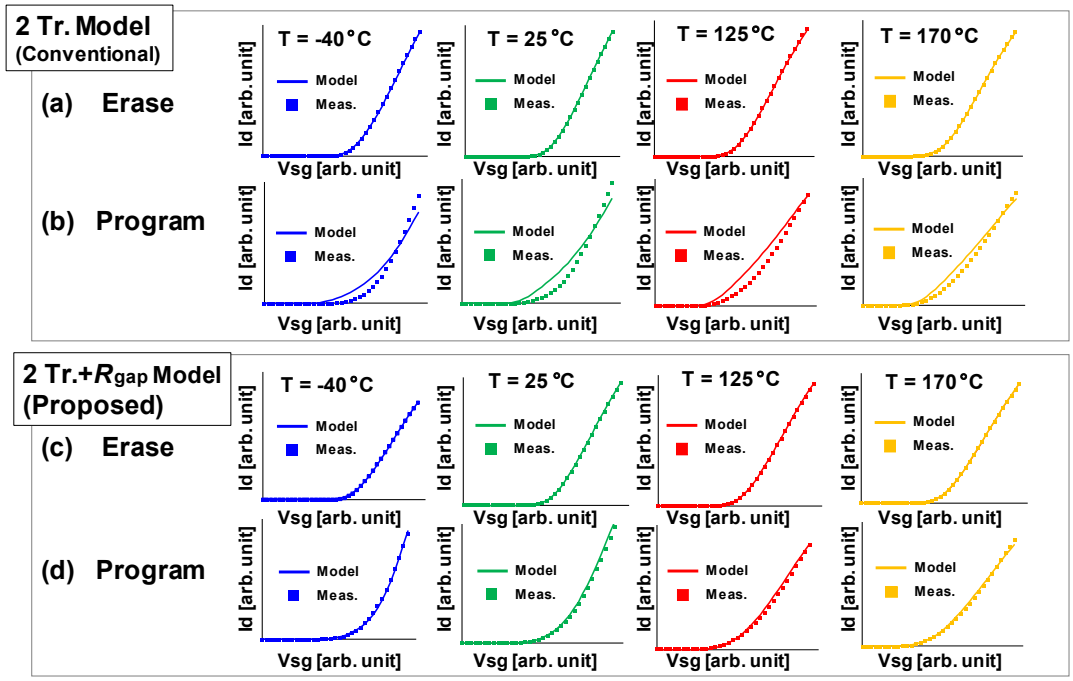


**Fig. 8** The fitting result for the read current of 28nm generation SG-MONOS cell. $I_d$ - $V_{sg}$ characteristics at the saturation region are shown for the erase condition and program condition. The prosed 2Tr.+$R_{gap}$ model is a single piece model for a continuous temperature, since the $R_{gap}$ dependence on the temperature is modeled. In contrast, the conventional 2 Tr. model requires parameter extraction for each discrete temperature.

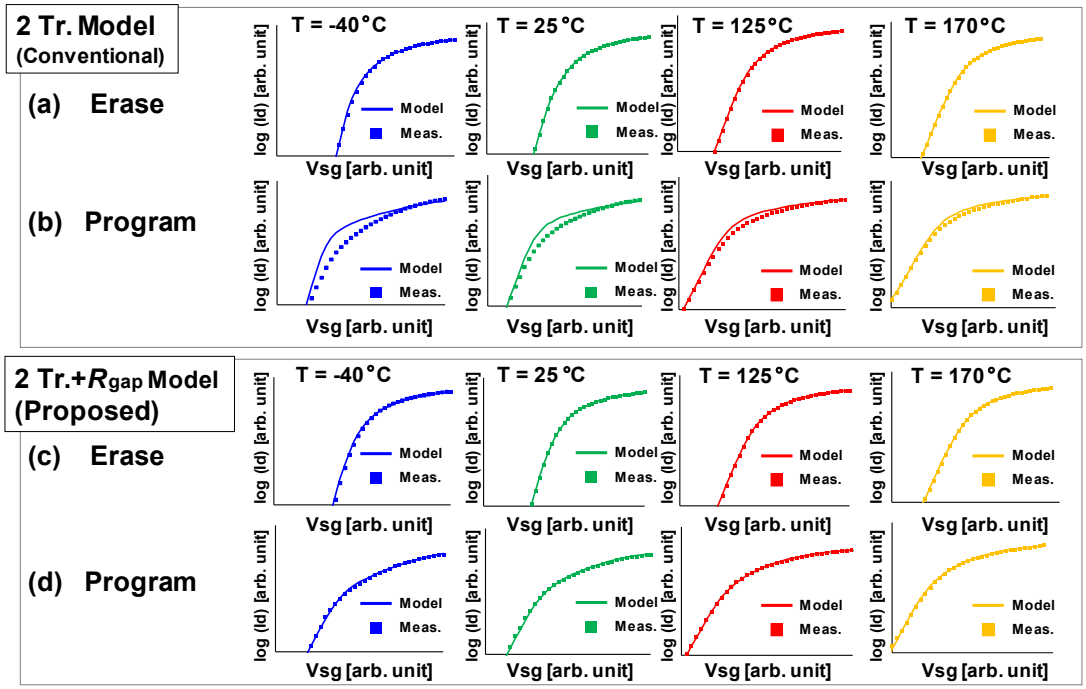


**Fig. 9** The fitting result for the read current of 28nm generation SG-MONOS cell. $\log(I_d)$ - $V_{sg}$ characteristics at the saturation region are shown for the erase condition and program condition. The prosed 2 Tr.+$R_{gap}$ model is a single piece model for a continuous temperature, since the $R_{gap}$ dependence on the temperature is modeled. In contrast, the conventional 2 Tr. model requires parameter extraction for each discrete temperature.

## V. Result of Model Fitting

Figs. 8 and 9 show the fitting result for the read current of 28nm generation SG-MONOS cell. $I_d$ - $V_{sg}$ characteristics at the saturation region are shown in the Fig. 8 and 9. The measured and simulated cell currents are plotted on a linear scale in Fig. 8 and plotted on a logarithmic scale in Fig. 9. A conventional model without $R_{gap}$ (2 Tr. model) does not reproduce the read current of the program condition, as shown in Fig. 8(b) and Fig. 9(b). However, the proposed model (2 Tr. + $R_{gap}$ model) exhibits an excellent fitting both for the erase and the program conditions (see Fig. 8 (c), Fig. 8(d), Fig. 9(c), and Fig. 9(d)).

## VI. Conclusions

A new SPICE-compatible model which reproduces the trap induced parasitic resistance of SG-MONOS cell using a synthesis of several variable resistances has been proposed. The model shows an excellent fitting on the cell current of 28nm generation SG-MONOS.

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