Efficient Models for Designing GB-Level 3-D 1S1R Horizontal-Stacked-RRAM and Vertical-RRAM Arrays

Lin Song, Jinyu Zhang

Institute of Microelectronics, Tsinghua University, Beijing, China, 100084
zhangjinyu@tsinghua.edu.cn

***Abstract*—Efficient models for simplifying 1S1R 3-D HRRAM and VRRAM arrays are proposed. Interconnect resistance, selector nonlinearity and different biasing schemes are considered. With reduction ratio of 1024, the models are accurate for Mb-size array and show a tendency to maintain high accuracy for larger sizes. Using the models, HRRAM up to 4 Gb and VRRAM up to 128 Mb are compared under the worst case scenario. To achieve larger array size, for HRRAM it is optimal to add layers; for VRRAM, it is optimal to enlarge array size per layer to maintain high write access voltage or add layers to keep high sensing margin.**

***Keywords*—3-D RRAM, HRRAM, VRRAM**

I. Introduction

3-D RRAM holds the advantage of high integration density, low operation power, high speed and low cost, which make it a promising candidate for future non-volatile memory [1]. There are mainly two types of 3-D RRAM arrays [2][3]: 3-D horizontal-stacked RRAM (HRRAM) (Fig.1 (a)) and 3-D vertical RRAM (VRRAM) (Fig.1 (b)). By adopting selectors, novel biasing schemes, RRAM array can avoid the sneak path problem thus achieve larger size. There are several works focusing on design and evaluation of large 3-D RRAM arrays by simulation [4][5]. Due to the limit of computing memory and simulation time (Fig.2), it is hard to simulate array larger than 1Mb. In this paper, efficient models for simplifying 1S1R HRRAM and 1S1R VRRAM arrays are proposed, and the performance metrics such as write access voltage, sensing margin, power consumption, and biasing schemes are compared and discussed.

II. Reduction Methods

A. Reduction method for HRRAM

The equivalent circuit is shown in Fig.3. The RRAM cells under the same biasing condition can be aggregated along the wordline/bitline using the so-called Y-Δ transform. The

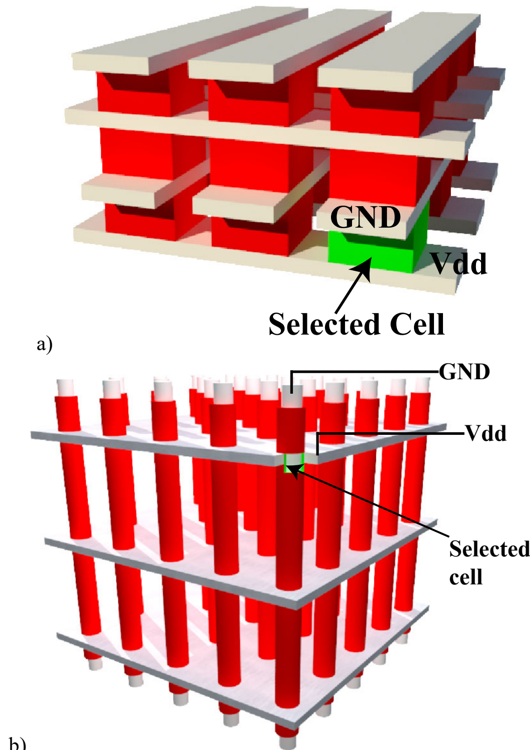

Fig. 1. 3-D RRAM arrays. a) HRRAM, b) VRRAM.

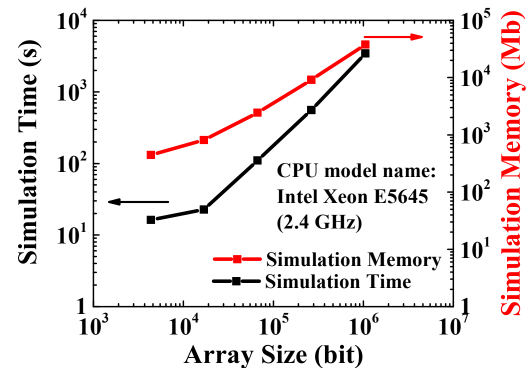

Fig. 2. Simulation time and memory of HRRAM.

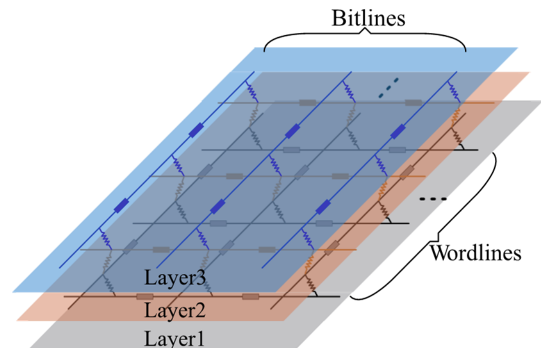

Fig.3. Equivalent circuit of 3-D HRRAM array.

© 2017 The Japan Society of Applied Physics

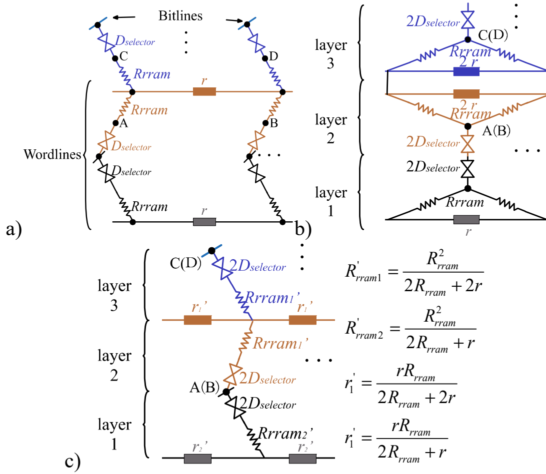

Fig.4. Reduction method of HRRAM. Different colors represent different layers. a) the aggregating unit. b) equivalent circuit after assuming $V_A = V_B$, $V_C = V_D$. c) equivalent circuit after reduction.

reduction method is demonstrated in Fig.4. The adjacent nodes of RRAM cells, which are not connected at the same wordline, for example, node A and B, C and D in Fig.4 (a), have close voltage potentials respectively so they are assumed to be connected together. Therefore, the selectors are in parallel and we can get Fig. 4 (b), after splitting one wordline resistor r into two paralleled ones. Then the array can be reduced by half using Y-Δ transform [6], as Fig. 4 (c) shows. The method to calculate R'_{rram1}, R'_{rram2}, r_1, r_2 is illustrated in [6]. The aggregation can be done recursively along both wordlines and bitlines. And after N rounds of iteration, the original array can be reduced by 4^N times.

B. Reduction method for VRRAM

One of the popular models is shown in Fig. 5, as is proposed in [7]. And the reduction method is shown in Fig.6. Take the aggregation along Y direction of 1-layer array as an example: First of all, RRAM cells are under the same biasing conditions. Then node A, B and C are assumed to be connected altogether due to two reasons: one is node A and B have very close voltage potentials according to symmetry. The other one is, the sneak current through the unselected RRAM is extremely small. Therefore, we get Fig. 6 (b), after splitting the plane resistors into paralleled ones. Furthermore, using the same Y-Δ transform, we can reach to Fig. 6 (c), now the number of RRAM cells in Y direction is reduced by half. Repeat the aggregation along X and Y directions by N rounds, the array can be reduced by 4^N times.

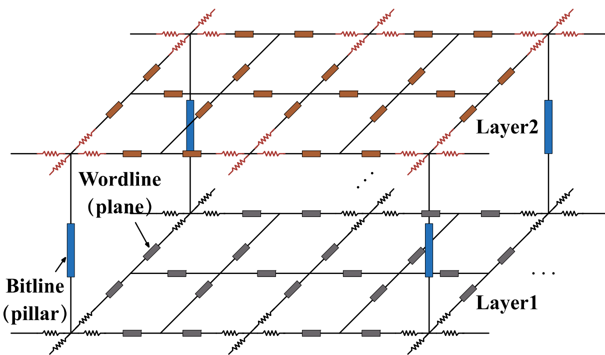

Fig.5. Equivalent Circuit of 3-D VRRAM array.

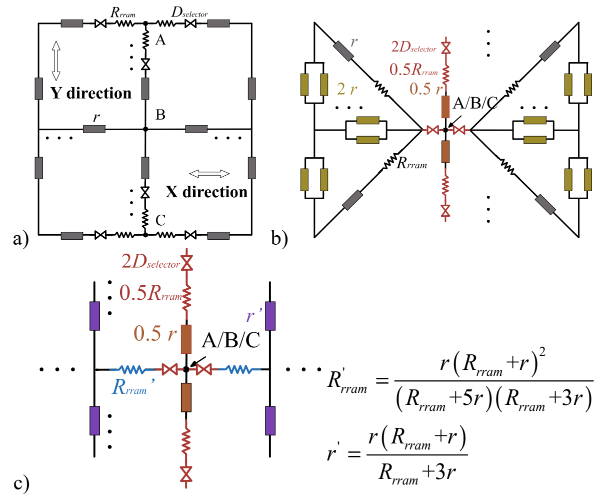

Fig. 6. Reduction Method of VRRAM. Different colors represent different values. a) the aggregating unit. b) equivalent circuit after assuming $V_A = V_B = V_C$. c) equivalent circuit after reduction.

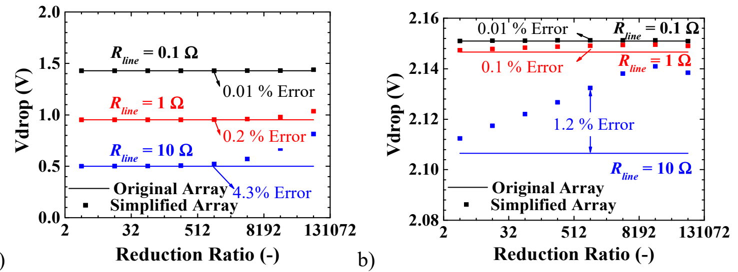

Fig.7. Comparison of the voltage drop on the selected RRAM between the model and original array. a) 4-Mb HRRAM. b) 512-Kb VRRAM.

III. Accuracy Validation

The simulation parameters are summarized in Table 1. This work is based on worst case scenario [8]. We evaluated the accuracy of models (Fig.7) in floating scheme. Due to the limitation of computing memory, the maximum array size is 4

TABLE I. Simulation Parameters

Parameters	HRRAM	VRRAM
Array size	1Mb ~4 Gb	512 Kb~ 128 Mb
Resistance of on state (R_{on})	10 KΩ	
Resistance of off state (R_{off})	1 MΩ	
Interconnect resistance (R_{line}/R_{plate})	0.1 Ω, 1 Ω, 10 Ω	
Selector I-V character	$I(V) = I_s \times \sinh(\alpha V)$	
Nonlinear factor (α)	18	
Zero biased current of Selector (I_s)	1 pA	
Writing voltage (V_w)	3 V	
Reading voltage (V_r)	1 V	
Biasing schemes	floating, 1/2 biasing, 1/3 Biasing	

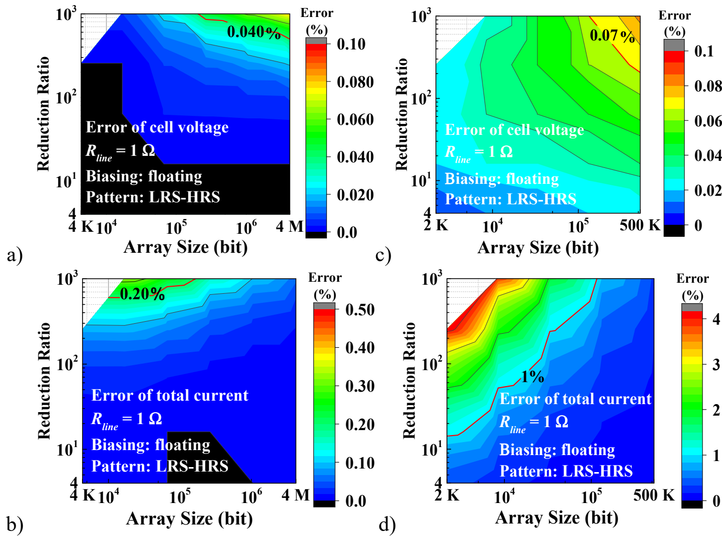

Fig.8. Model's error vs reduction ratio and array size. a) simulation error of cell voltage of HRRAM; b) simulation error of total current in array of HRRAM; c) simulation error of cell voltage of VRRAM; d) simulation error of total current in array of VRRAM.

Mb (HRRAM) and 512 Kb (VRRAM), respectively. The simplified arrays show a very good agreement with the original arrays, with a reduction ratio up to 1024. The relation between accuracy and reduction ratio is verified under different array sizes (Fig.8). For larger array sizes, given the same reduction ratio, simulation accuracy is either improved (Fig. 8 (b), Fig. 8 (d)) or maintaining high (Fig. 8 (a), Fig. 8 (c)), proving the model's capability of dealing with much larger arrays.

IV. Simulation Results and Discussion

Using the simplified models with reduction ratio of 1024, we compared the performance of HRRAM (4 Gb) and VRRAM (128 Mb) with three design aspects: access voltage ratio (AR), sensing margin (SM) and nonlinearity of selector (α). Different biasing schemes, interconnect resistance and power consumption are also considered.

A. Writing performance

With density of 1Mb/layer, HRRAM can hardly achieve access voltage higher than 50% V_{dd} (Fig. 9). Access voltage keeps constant over layers (Fig. 9 (a)). Moreover, 1/3 biasing scheme exhibits the best performance. For VRRAM, floating scheme achieves best AR as high as 70% and is constant over size per layer (Fig. 10 (b)). However, AR degrades fast over layers (Fig. 10 (a)).

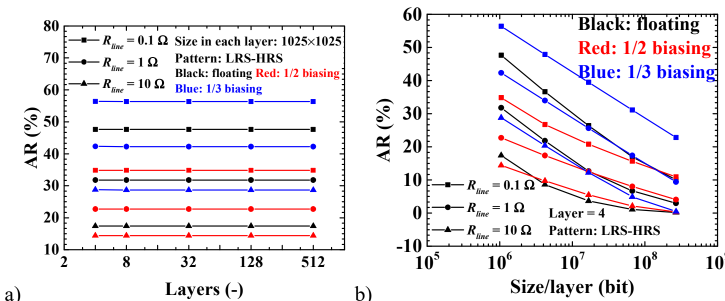

Fig.9. HRRAM: Access voltage ratio (AR). a) AR vs layers, b) AR vs array size per layer.

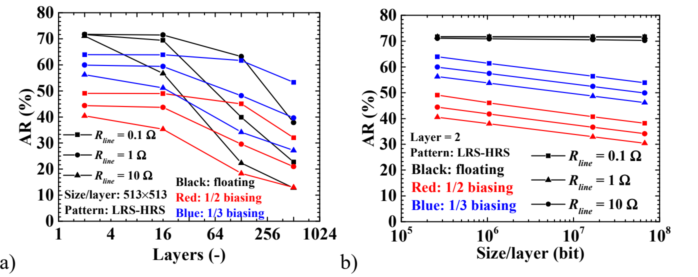

Fig.10. VRRAM: Access voltage ratio (AR). a) AR vs layers, b) AR vs array size per layer.

B. Reading performance

For reading case, with density of 1Mb/layer, HRRAM can hardly achieve SM higher than 12% (Fig. 11). Similar to AR, SM keeps constant over layers (Fig. 11 (a)). For VRRAM, 1/3

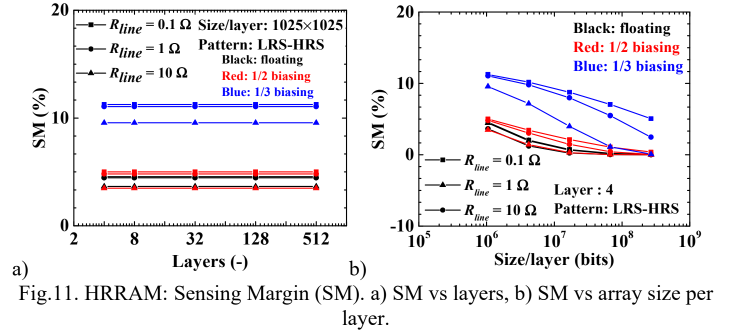

Fig.11. HRRAM: Sensing Margin (SM). a) SM vs layers, b) SM vs array size per layer.

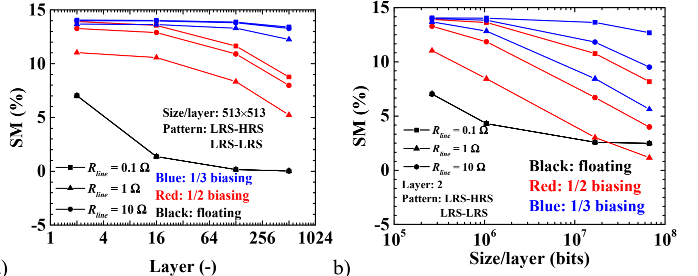

Fig.12. VRRAM: Sensing Margin (SM). a) SM vs layers b) SM vs array size per layer.

biasing scheme shows the best SM which reaches 13% (Fig.12). Moreover, it is almost constant over layers (Fig. 12 (a)).

C. Nonlinearity and power consumption

The influence of nonlinearity (α) on AR/SM is shown in Fig. 13 (HRRAM) and Fig.14 (VRRAM). With increasing of α, AR/SM first increases then decreases (Fig.13 (a) (b), Fig. 14 (b)) or saturates (Fig. 14 (a)). As to the power consumption, it saturates at high α. 1/3 biasing scheme shows much higher power consumption (100X~10000X) than the rest two schemes. For writing, VRRAM has the same power consumption per bit as HRRAM. For reading, the power consumption of VRRAM is 10X higher.

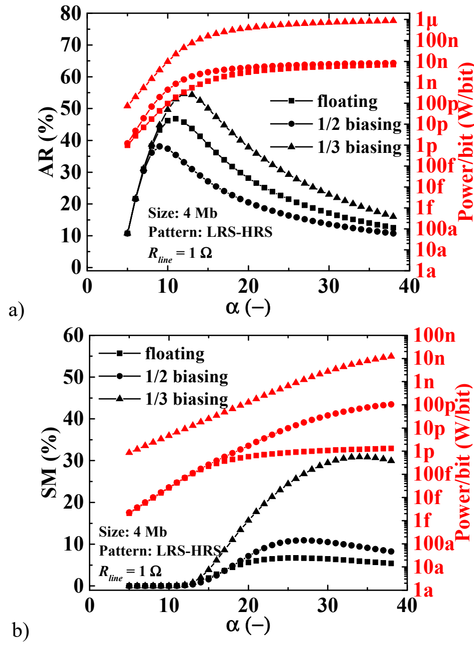

Fig.13. HRRAM: influence of selector's nonlinearity. a) α vs AR and writing power, b) α vs SM and reading power.

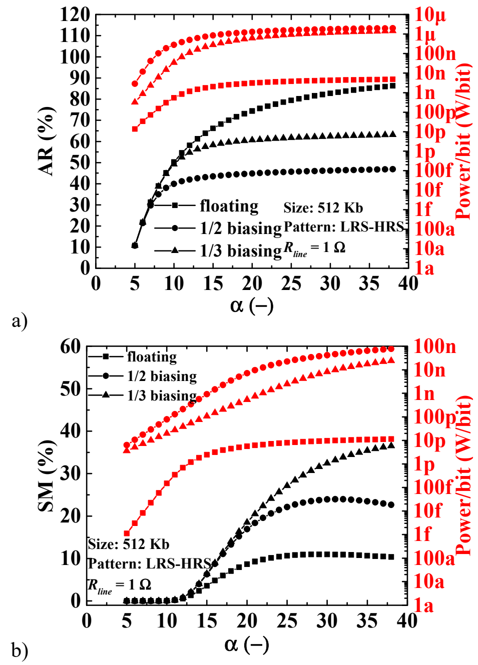

Fig.14. VRRAM: influence of selector's nonlinearity. a) α vs AR and writing power, b) α vs SM and reading power.

V. Conclusions

Simplified models for 3-D 1S1R HRRAM and VRRAM are developed for Gb-scale array design. With reduction ratio of 1024, they are proved to be accurate at Mb-scale and keep high accuracy for larger sizes. The AR/SM decreases as array size increases. In order to achieve larger size, it is optimal for HRRAM to increase layers instead of array size per layer. However, for VRRAM, it is optimal to increase array size per layer for keeping high AR, and increase layers for keeping high SM. There is no evident difference in writing power between HRRAM and VRRAM, however VRRAM consumes 10X reading power. Compared to the other two biasing schemes, generally, 1/3 biasing scheme shows better performance but consumes much higher power consumption (100X~10000X). Nonlinearity of selector influences AR and SM differently, which requires a tradeoff in performance.

References

[1] H. Wu, Y. Liao, B. Gao et al., in 3D Flash Memories, pp. 223–260.

[2] M. C. Hsieh, Y. Liao, Y. Chin et al., "Ultra high density 3D via RRAM in pure 28nm CMOS process", in IEDM2013, pp. 260-263.

[3] H. Chen, H. Tian, B. Gao et al., "Electrode/oxide interface engineering by inserting single-layer graphene: Application for HfO x-based resistive random access memory", in IEDM2012..

[4] Y. Deng, H. Chen, B. Gao et al., "Design and optimization methodology for 3D RRAM arrays", IEDM 2013, pp. 629-632.

[5] S. Yu, Y. Deng, B. Gao et al., "Design guidelines for 3D RRAM cross-point architecture", ISCS2014, pp. 421-424.

[6] . L. Song, J. Zhang, An Chen et al., "An efficient method for evaluating RRAM crossbar array performance", Solid. State. Electron., vol. 120, pp. 32–40, 2016.

[7] S. Yu, H. Chen, Y. Deng et al., "3D vertical RRAM-Scaling limit analysis and demonstration of 3D array operation", VLSI2013.

[8] Y. Deng, P. Huang, B. Chen et al., "RRAM Crossbar Array With Cell Selection Device: A Device and Circuit Interaction Study", TED, vol. 60, pp. 719-726, 2013