Modeling of BTI-Aging V_T Stability for Advanced Planar and FinFET SRAM Reliability

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***Abstract*—In this study, the comparison of time-zero V_T and Bias-Temperature Instability (BTI) induced V_T shift on advanced planar (20nm System-on-Chip, 20SoC) and FinFET (16nm FinFET, 16FF) is investigated, which is modeled by Dispersive Skellam (DS) cumulative distribution framework. As a result of the much better time-zero Vt mismatch and less V_T shift spread in FinFET devices, the SRAM static noise margin (SNM) shift distribution of 16FF is less than 20SoC planar technology node. We present a universal picture of time-zero Vt and BTI-aging V_T shift management to correlate SRAM bit cell SNM shift, which offers a prospected approach for advanced planar and FinFET SRAM reliability optimization.**

***Index Terms*—HK/MG, FinFET, BTI, SRAM, SNM**

I. Introduction

To continuously realize Moore's Law, transistor geometry keeps scaling for decades, which also leads to higher circuit density and performance. Up to 20nm technology node, the planar transistor scaling had reached the ultimate constraint due to process and physical limitation such as short-channel effect. To achieve better device performance with scaled geometry, we have successfully developed 16nm FinFET (16FF) technology node and investigated its unparalleled electrostatic and distinguished reliability, as compared to conventional planar devices [1-3]. However, the ultra-scaled transistors may result in larger V_T mismatch from process control fluctuation such as dopant variation, thus, leads to worse circuit performance and stability. Also, the BTI-aging variability could further degrade the product reliability.

In this work, we modeled the BTI-induced V_T shift (ΔV_T) through Dispersive Skellam (DS) distribution statistical model, to depict the ability of BTI ΔV_T dispersion and discuss its impact on SRAM SNM shift distribution. Finally, the significance of BTI degradation management on FinFET SRAM reliability is interpreted.

II. Experiments and Model

Transistor level V_T sigma/BTI variability and SRAM cell SNM are studied on 20SoC (HK/MG planar) and 16FF (HK/MG FinFET) process technologies. Rauch [4] derived V_T shift variance, by first assuming a Poisson distribution on the total number of charges generated through reliability stress or long-term circuit operation as follows:

$$\frac{Var(\Delta\delta V_T)}{Mean(\Delta V_T)} = \frac{k_1 k_0 T_{ox}}{A_{Gate}} \quad (1)$$

$$\text{where } K_Q = \frac{k_0 T_{ox}}{A_{Gate}} \quad (2)$$

Also, a comprehend BTI variability of Dispersive Skellam (DS) cumulative distribution framework was given by Rauch [2] as

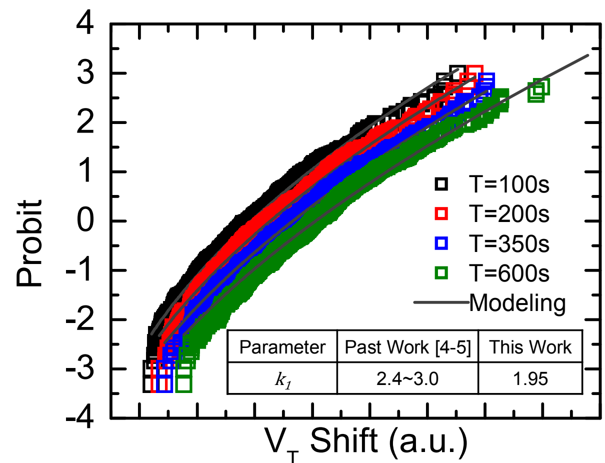
$$\mathrm{CDF}(\Delta V_T) = \sum_{m=0}^{\infty} \frac{e^{-(\overline{\Delta V_T}/K_Q)} \cdot (\overline{\Delta V_T}/K_Q)^m}{m!} \Phi\left(\frac{\Delta V_T/K_Q - m}{\sqrt{m(k_1-1)}}\right) \quad (3)$$

where $\overline{\Delta V_T}$ stands for mean ΔV_T. From (1), it's clear that k_1 is the parameter of the dependence between device ΔV_T variation and geometry (under similar gate dielectric thickness). Smaller value of k_1 represents smaller transistor ΔV_T spread under same device area, which are approximately 2.4 to 3 for conventional planar technologies [4-5].

III. Results and Discussion

A. BTI-aging Vt variability modeling of discrete devices

Fig. 1 shows 16FF NBTI V_T shift with respect to different stress time, and the V_T shift is modeled by DS framework shown in (3). For sufficient model determination, the sample size of NBTI measurement is larger than 1000. It could be seen that the DS framework is working well to model the NBTI degradation with various stress time.



Parameter	Past Work [4-5]	This Work
k_1	2.4~3.0	1.95

Fig. 1. NBTI-aging V_T shift of 16FF discret PFET for various stress time (up to 600sec). The V_T shift is modeled by DS framework, and the k_1 parameters with all stress time obtained in this work is 1.95, smaller than the past work of 2.4~3.0

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The value of k_I obtained from the DS framework modeling is 1.95 (Fig. 1), which is also independent of stress time. The value of k_I of 16FF FinFET device is obviously less than conventional planar transistor (k_I: 2.4~3, [4-5]), suggesting that the ΔV_T variability of FinFET is significantly less than planar devices. It is believed that the smaller ΔV_T spread of FinFET than planar devices is due to the process optimization of the interface and bulk trap reduction in FinFET gate dielectric stacks. From (1), to keep similar or better BTI aging variability for FinFET technology node evolution, the reduction of ΔV_T variation (revealed in k_I value reduction) of FinFET is quite critical since the device geometry of FinFET is significantly smaller than planar transistors.

For SRAM and other circuits, the AC waveform stress is more realistic to mimic real product operation. Also, AC stress is particularly important to obtain the degree of BTI recovery in device level. To study the recovery of BTI under AC stress, Fig. 2 shows the PBTI and NBTI AC-to-DC factors (by V_T shift) of 20SoC and 16FF as a function of duty ratio (DR). The relaxation signatures of PBTI and NBTI could be modeled by universal relaxation model as [6],

$$r(\xi) = \frac{1}{(1+B\times\xi^{\beta})} \quad (4)$$

where $r(\xi)$ is the AC-to-DC factor, ξ is the universal relaxation time (=relaxation time/stress time=1/DR-1), and B and β are the scaling and dispersive shape factors, respectively. Even the interface orientation of FinFETs contain both <100> and <110>, as compared to <100> in planar [7], NBTI recovery signature between 20SoC and 16FF is still comparable as demonstrated by the universal relaxation model.

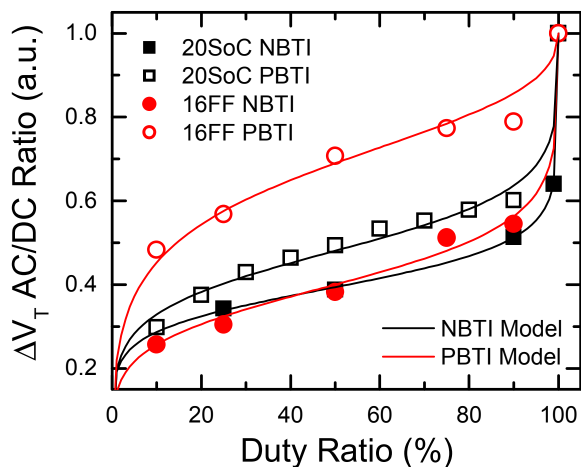

Fig. 2. PBTI and NBTI AC/DC factors (by V_T shift) as a function of duty ratio for 20SoC and 16FF. NBTI relaxation between 20SoC and 16FF are identical, while 16FF PBTI shows less recovery than 20SoC. Both PBTI and NBTI relaxation could be modeled by universal relaxation model shown in (4).

Fig. 3 shows the FinFET PBTI relaxation signatures comparison between 2SoC and 16FF NFET. The recovery fraction is defined as the recovery of V_T shift in the relaxation phase (under $V_{G,stress}$=0V) and normalized to the final PBTI degradation (at final stress point). It could be seen that the amount of FinFET PBTI relaxation is less than planar devices, which is consistent with Fig. 2. The less PBTI recovery of FinFET could be attributed to the higher field in the fin top region at PBTI stress. Fin top region is more depleted than fin body since it is truly surrounded by gate, and it makes the threshold voltage in fin top to be lower than fin body. And therefore, the electric field cross on gate stack on fin top region will be locally higher than fin sidewall during PBTI stress, the more electron traps on fin top HK make less PBTI relaxation than conventional planar devices.

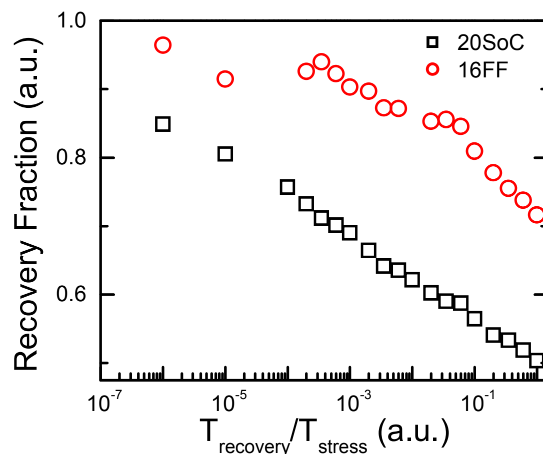

Fig. 3. PBTI relaxation signatures of 20SoC and 16FF. The recovery amount and recovery rate of 20SoC are higher than 16FF, which could be due to high local electric field at HK gate stack on fin top region, leading to more electron traps and less relaxation, as compared to PBTI in planar transistors.

B. Variability of SRAM PU/PD devices

After modeling the transistor BTI aging variability through DS framework, SRAM degradation such as SNM changes and its variation is also helpful to study the correlation between device level variability and product reliability. Fig. 4 shows the butterfly curve of 16FF SRAM pre- and post-stress, indicating the transistor characteristics (like V_T) at time-zero and post-stress are determining the SRAM static noise margin. During this characterization, AC stress is applied on the nodes of SN1 and SN2 (shown in the inset of Fig. 4) to emulate the real SRAM operation and burn-in conditions. It means the AC stress waveform is applied on PU (pull-up) and PD (pull-down) transistors at both sides, so the transistor BTI aging degradation leading to static noise margin reduction on both side could be characterized, as shown in Fig. 4.

Fig. 5 shows the time-zero PU V_T sigma comparison between 20SoC and 16FF. For both PU1 and PU2 (in Fig. 4), the 16FF FinFET shows smaller time-zero V_T sigma compared to 20SoC planar devices. Similarly, the NFET PD time-zero V_T variation of 16FF FinFET is also superior to 20SoC planar, as shown in Fig. 6. The physical origin of time-zero device V_T variability is resulted from process fluctuations, including dopant variation in the channel. In terms of the fully depleted fin body to reduce the V_T, the amount of channel dopant in FinFET is much less than planar, which makes the smaller V_T sigma for FinFET devices.

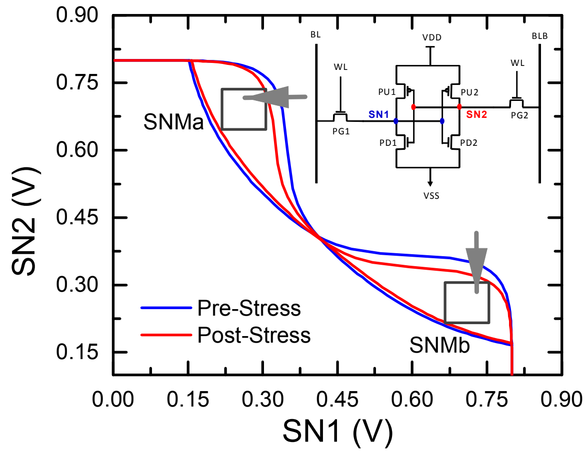

Fig. 4 Butterfly curve of 16FF SRAM SNM before and after stress. Schematic of SRAM cell is shown in the inset. The AC stress is applied on the SN1 and SN2, to emulate real SRAM burn-in condition. SNM shift is the consequence of BTI degradation in PU/PD transistors.

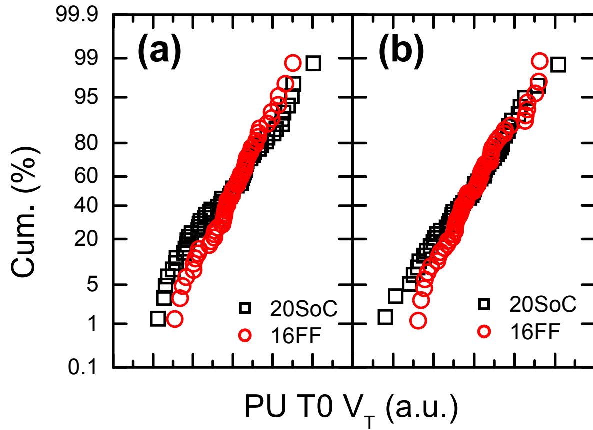

Fig. 5 (a) PU1 and (b) PU2 of time-zero V_T distribution of 20SoC and 16FF. For both PU1 and PU2, V_T sigma of 16FF is much tighter compared to 20SoC, which indicates the better process fluctuation control of 16FF.

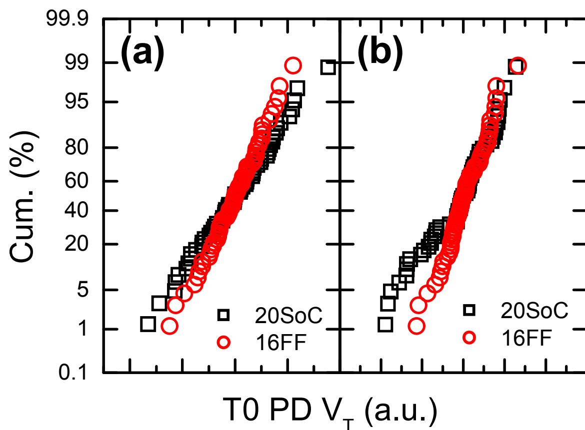

Fig. 6 (a) PD1 and (b) PD2 of time-zero V_T distribution of 20SoC and 16FF. Both PU1 and PU2 show better V_T sigma in 16FF as compared to 20SoC, which indicates the better process fluctuation control of 16FF.

After the AC stress on SN1 and SN2, the PU and PD V_T shift sigma for both 20SoC and 16FF are also compared. Fig. 7 shows both PU1 and PU2 V_T shift variation of 16FF are smaller than 20SoC. Those results are in good agreement with Fig. 1, means the BTI ΔV_T spread of FinFET is more optimized as compared to planar transistors through HK gate dielectric process improvement. Likewise, for NFET, Fig. 8 also shows both PD1 and PD2 V_T shift variability of 16FF are better than 20SoC, suggesting that the FinFET process control on gate stack traps is also beneficial to reduce PBTI aging spread as well.

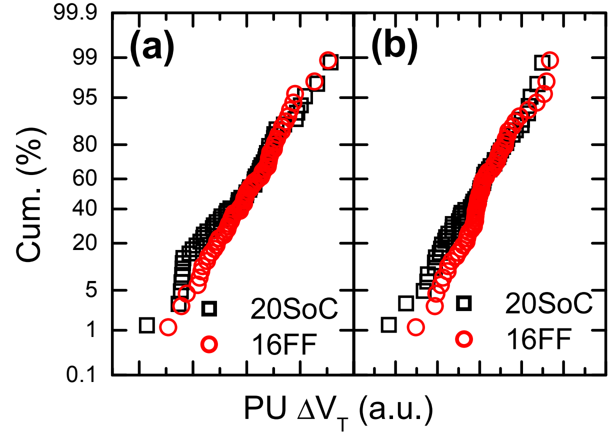

Fig. 7 (a) PU1 and (b) PU2 NBTI-induced V_T shift by AC stress at SRAM SN1/SN2 nodes. Both PU1 and PU2 show smaller Vt shift spread in 16FF as compared to 20SoC, which is consistent with DS framework modeling interpretation in Fig. 1.

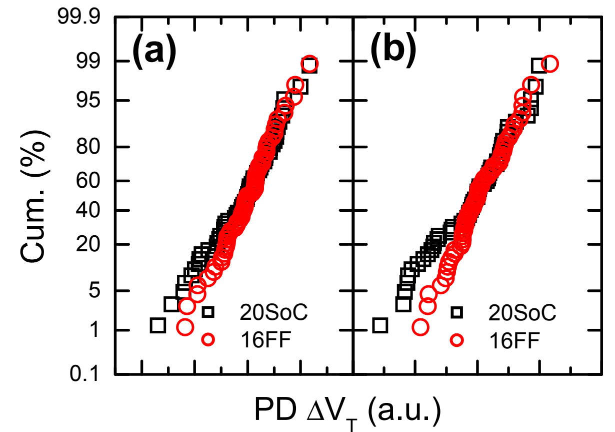

Fig. 8 (a) PD1 and (b) PD2 PBTI-induced Vt shift by AC stress at SRAM SN1/SN2 nodes. Both PD1 and PD2 show smaller Vt shift spread in 16FF as compared to 20SoC, which is consistent with DS framework modeling interpretation in Fig. 1.

C. Impact of device aging distribution on SRAM cell level SNM shift

The study of device level time-zero V_T and V_T shift sigma on SRAM PU/PD nodes is not only helpful to validate the DS framework for BTI aging variability modeling, but also serves as the basis to investigate the SRAM cell level SNM degradation and distribution. Fig. 9 shows the initial SNM distribution (where SNMa and SNMb are the upper and lower SNM, defined in Fig. 4) of 16FF is tighter than 20SoC, which is attributed to the smaller time-zero V_T sigma of 16FF (as shown in Figs. 5 and 6). Besides the better initial V_T spread, the tighter BTI induced ΔV_T distribution of 16FF also makes smaller SNM shift sigma for FinFET SRAM, as shown in Fig. 10.

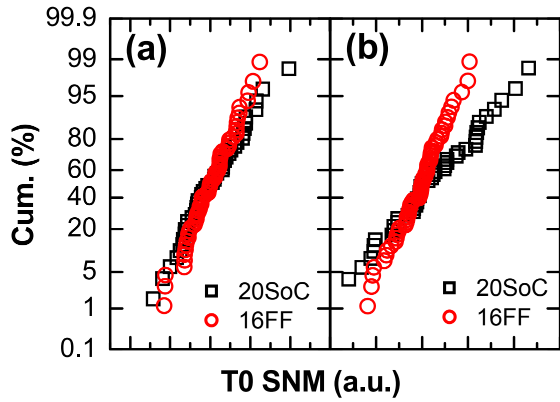

Fig. 9 (a) SNMa and (b) SNMb time-zero distribution of 20SoC and 16FF. Both SNMa and SNMb show tighter SNM distribution in FinFET SRAM. It is due to the smaller time-zero PU/PD Vt distribution of FinFET transistors shown in Figs. 5 and 6.

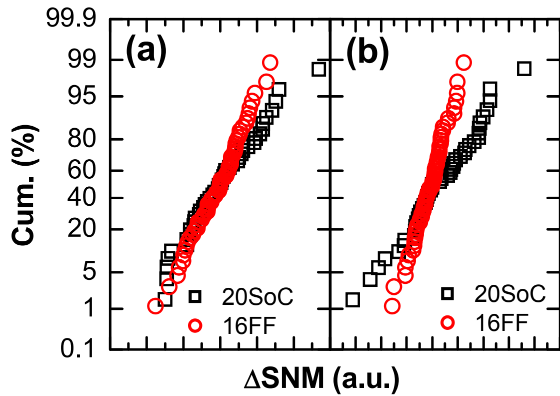

Fig. 10 (a) SNMa and (b)SNMb degradation of 20SoC and 16FF. Both ΔSNMa and ΔSNMb show smaller variation in 16FF.

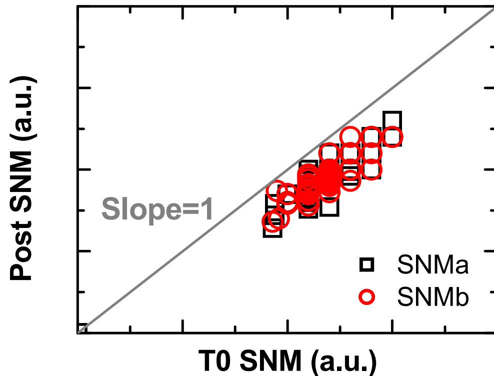

Fig. 11 16FF post AC stress SNMa and SNMb as function of time-zero SNMa and SNMb. Smaller static noise margin after stress is due to PU and PD device degradation from BTI aging.

Fig. 11 shows the post-stress SNM (for both SNMa and SNMb) with respect to time-zero SNM, which shows a certain amount of SNM shift after SN1/SN2 AC stress. To identify if NBTI or PBTI induced V_T shift may cause such SRAM SNM shift, Fig. 12 shows the post-stress V_T of PU and PD devices as a function of initial V_T. It is noted that even with more recovery in NBTI AC stress (Fig. 2), NBTI induced V_T shift on PU devices is still more significant than PBTI on PD devices. In fact, PBTI degradation on PD devices is quite negligible. Thus, we could conclude the SNM shift shown in Fig. 12 is dominated by NBTI. It means NBTI plays an important role in SRAM reliability, such that improvement of interface state reduction is critical for FinFET product reliability management.

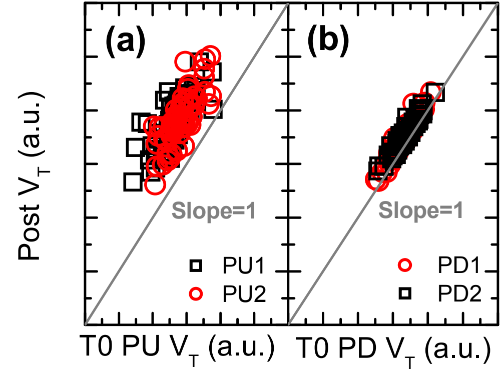

Fig. 12 Post AC stress V_T for (a) PU and (b) PD as function of time-zero V_T. The scale of x- and y-axis for (a) and (b) are the same for comparison. The NBTI-induced V_T shift in PU PFET is obviously larger than PBTI-induced V_T shift in PD NFET.

IV. Conclusions

In this work, BTI-aging V_T distribution in FinFET is successfully modeled by DS framework, in which the parameter of k_1 offers an indicator of BTI-aging variability. Smaller value of k_1 (1.95) consolidates the BTI V_T shift variability of 16FF is smaller than the conventional planar devices, which is critical to compensate the larger V_T shift mismatch in scaled FinFET transistors. In terms of AC stress on SRAM, we also demonstrate the initial and post-stress PU/PD V_T distribution of 16FF is superior to 20SoC planar devices, which makes the SNM shift distribution smaller on FinFET SRAM. Process optimization of interface state reduction is crucial in managing SNM shift since NBTI plays an important role in SRAM SNM shift.

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