Timing and Power Fluctuations on Gate-All-Around Nanowire CMOS Circuit Induced by Various Sources of Random Discrete Dopants

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***Abstract*—Random dopant fluctuation (RDF) is one of fluctuation sources in sub-7-nm semiconductor technology node. In this paper, we estimate the timing and power fluctuations on 10-nm-gate gate-all-around (GAA) silicon nanowire (NW) complementary metal-oxide-semiconductor (CMOS) circuit induced by various random discrete dopants (RDDs) from channel (with/without doping), source/drain (S/D) extensions and penetration from S/D extensions. The 3D quantum mechanical transport and non-equilibrium Green's function (NEGF) models were used for the NW CMOS circuit. The experimentally validated device simulation indicates that at a similar threshold voltage, CMOS devices without channel doping possess 49.5% reduction on the normalized fluctuation of the static power consumption due to the reduction of σV_{th} and σI_{off}. The normalized fluctuation of dynamic power is comparable with/without channel doping due to small variation of the gate capacitance. Because of reduction of σI_{sat}, the normalized fluctuation of short-circuit power of CMOS circuit was reduced from 21.7% to 10.2% without channel doping. And, we found that the fluctuations of the timing, noise margin (NM) and power consumption of the NW CMOS circuit follow the trend of σV_{th}. From the point of view of N-/P-type NW MOSFETs caused by RDF, this study may show the fluctuation of CMOS circuit performance highly influenced by the key parameters of N-/P-type NW MOSFETs.**

Keywords—Timing fluctuation; power fluctuation; gate-all-around; nanowire; CMOS circuit.

I. INTRODUCTION

Gate-all-around (GAA) nanowire (NW) MOSFET is a promising device for sub-7-nm technology nodes [1-4] and characteristic variabilities have suffered serious problems [5-6]. Channel engineering approaches (vertical and lateral) were reported to suppress the variations of timing and power for planar MOSFET [7]. The report showed that the RDDs contributed device random fluctuations have less suppressed in undoped channel Si GAA n-NWFETs with doped S/D regions [8]. The RDDs-induced variation problems of planar MOSFET such as timing and power fluctuations [9] may affect GAA NW CMOS circuit's transfer and dynamic characteristics seriously. However, the impact of RDDs from channel and S/D extensions on the variation of timing and power of GAA NW CMOS has not been investigated. In this study, we explore the fluctuated CMOS devices and circuit's properties caused by RDDs with all RDDs from channel, S/D extension and penetration from S/D extension (denoted as RDs_ch_Sext_Dext_pe) and without channel doping (denoted as RDs_Sext_Dext_pe), respectively.

II. DEVICE STRUCTURE AND STATISTICAL DEVICE SIMULATION

Fig. 1(a) shows the adopted device characteristics and the achieved nominal parameters of short-channel effect of the studied N-/P-type NW MOSFETs. Before estimating our simulation, the band profile along the channel was examined by solving 3D quantum mechanical transport and non-equilibrium Green's function (NEGF) models. It is validated with NEGF results by adjusting the electron effective mass. The results show a good agreement between the two models. Then, we calibrate the simulation result with measurement data by fitting the mobility model parameters [1]. As shown in Fig. 1(b), there are four types of RDDs, where their concentration and distribution are statistically generated by Monte Carlo method for N-/P-type NW MOSFETs, individually. The 2000 nm cylinder is partitioned into 200 sub-cylinders with 10 nm for acceptor-type RDDs in the channel (denoted as RDs_ch), and its distribution is shown in Fig. 1(d). Similarly, the 2000 nm cylinder is partitioned into 200 sub-cylinders with 10 nm for donor-type RDDs penetration from S/D into the channel (denoted as RDs_pe) and the distribution is shown in Fig. 1(e). The 1000 nm cylinder is partitioned into 200 sub-cylinders with 5 nm for donor-type RDDs in the source extension (denoted as RDs_Sext) and drain extension (denoted as RDs_Dext) and the distribution is shown in Fig. 1(f) and Fig. 1(g), respectively. Finally, we utilize the NW CMOS circuit as the tested device to explore the timing and power fluctuations of NW CMOS circuit, as shows in Fig. 1(c). The normalized fluctuation of the characteristic parameters of CMOS circuit and N-/P-type NW MOSFETs device is calculated by (6σ/Mean value) x 100%, where σ is standard derivation of the variation, and the mean value is the average of the characteristic parameters. Notably, the normalized fluctuation may be slightly different due to distribution of RDDs.

(a) Parameter	N-type	P-type
Gate Length (L) (nm)	10	
EOT (T_{ox}) (nm)	0.6	
Radius (R) (nm)	5	
Channel Doping (cm^{-3})	5e17	
S/D Doping (cm^{-3})	1e20	
I_{ON} (A)	7.636e-6	4.973e-6
I_{OFF} (A)	1.599e-11	2.757e-11
SS (mV/dec)	72	73
DIBL (mV/V)	65	65

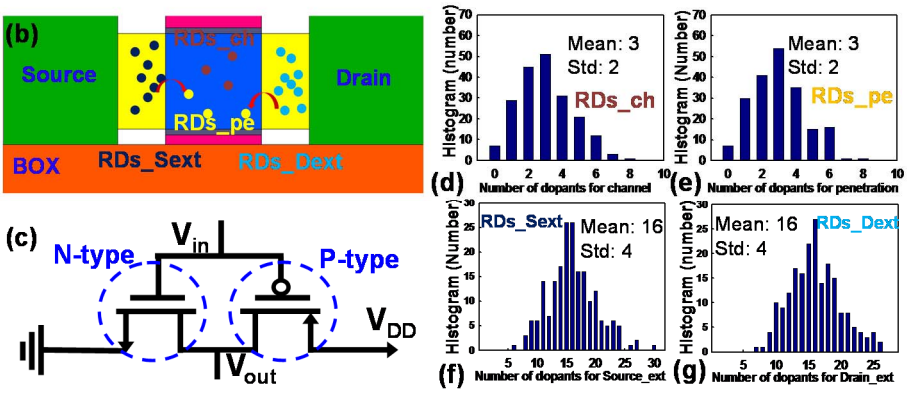

Fig. 1. (a) The device characteristics and the nominal short channel effect parameters of the studied n-/p-type NW MOSFET are shown. (b) The illustration of device structure with various types of random dopant. (c) The inverter circuit is utilized as the tested device in this study. (d) The distribution of RDs_ch with the equivalent channel doping concentration is $5x10^{17}$ cm^{-3}. (e) The distribution of RDs_pe with the equivalent channel doping concentration is $3.36x10^{17}$ cm^{-3}. (f) The distribution of RDs_Sext with the equivalent channel doping concentration is $4.8x10^{18}$ cm^{-3}. (g) The distribution of RDs_Dext with the equivalent channel doping concentration is $4.8x10^{18}$ cm^{-3}.

III. Results and Discussion

Fig. 2 shows the fluctuation of threshold voltage (σV_{th}) of N-/P-type NW MOSFETs and the timing characteristics of CMOS circuit. The falling time (tf), the rising time (tr), the high-to-low delay time (tHL), and the low-to-high delay time (tLH) including the input/output signals are shown in Figs. 2(a)-(c). Compared to RDs_ch_Sext_Dext_pe, the magnitude of σV_{th} can be reduced by RDs_Sext_Dext_pe for N-/P-type NW MOSFETs, as shown in Fig. 2(d). It seems that the effect of channel doping plays a key role for the reduction of V_{th}. In addition, the neutralization of RDs_ch and RDs_pe is implicit for the case of RDs_ch_Sext_Dext_pe. It might be attributed to different numbers of RDs_ch and RDs_pe inside the channel. For the transition of high-to-low, the output signal falls while the N-type NW MOSFET turns on; thus, the fluctuations of tf and tHL are substantially governed by σV_{th} of the NMOS device. Similarly, tr and tLH is strongly influenced by the fluctuation of V_{th} of PMOS device. The fluctuation of the timing of CMOS circuit follows the trend of V_{th} fluctuation. Hence, the fluctuation of the timing can be reduced for CMOS circuit without channel doping, as shown in Figs. 2(e)-(f). Fig. 3(a) shows the RDDs-fluctuated voltage transfer curves and the noise margin (NM). The maximum permitted logic 0" at input, VIL, and the minimum permitted logic "1" at input, VIH, are extracted from the output voltage at the slope of -1V/V. These two points are used to determine NMH (noise margin high) and NML (noise margin low); NML = VIL and NMH = VDD-VIH. Figs. 3(b)-(c) show that the fluctuations of NML and NMH are reduced for the case without channel doping. We found that the fluctuations of NM follow the trend of σV_{th}. Figure 4 shows the fluctuated power consumption induced by RDs_ch_Sext_Dext_pe and RDs_Sext_Dext_pe, respectively. The total power (P_{total}) is composed of static power (P_{stat}), short-circuit power (P_{sc}), and dynamic (P_{dyn}) power. The definition of these power components are listed as below:

$$P_{stat} = V_{DD} I_{leakage}, \quad (1)$$

$$P_{sc} = f_{0\to1} V_{DD} \int_T I_{sc}(\tau) d\tau, \quad (2)$$

and

$$P_{dyn} = C_{load} V_{DD}^2 f_{0\to1}, \quad (3)$$

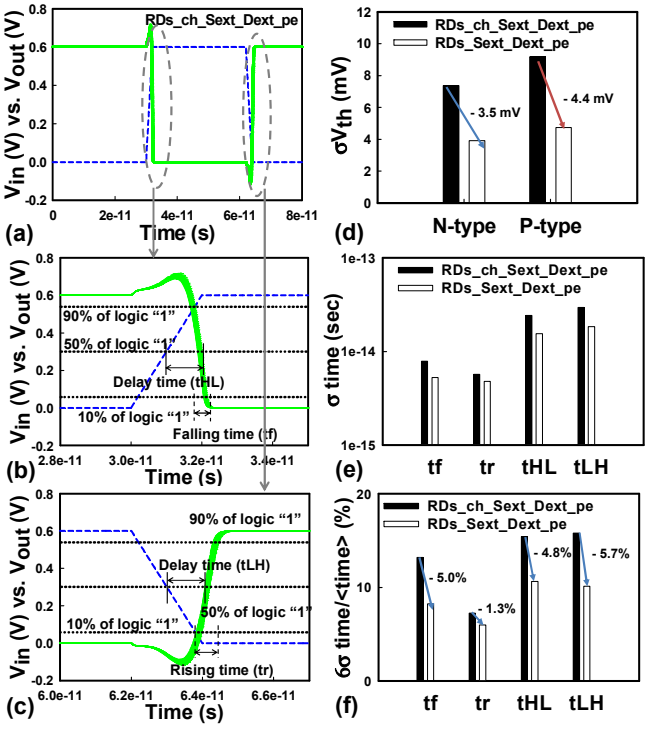

Fig. 2. Plot of the simulation structure of Si MOSFET and the defined parameters. (a) Input and output signal of tested inverter devices affected by RDDs. (b)-(c) The zoom-in plots of the time transition characteristic of (a) including tf, tr, tHL and tLH. (d) Comparison of the standard deviation of V_{th} induced by RDs_ch_Sext_Dext_pe and RDs_Sext_Dext_pe, respectively. (e)-(f) Plots of the standard deviation and the coefficient of variance of timing analysis tf, tr, tHL and tLH of inverter circuits induced by RDs_ch_Sext_Dext_pe and RDs_Sext_Dext_pe, respectively.

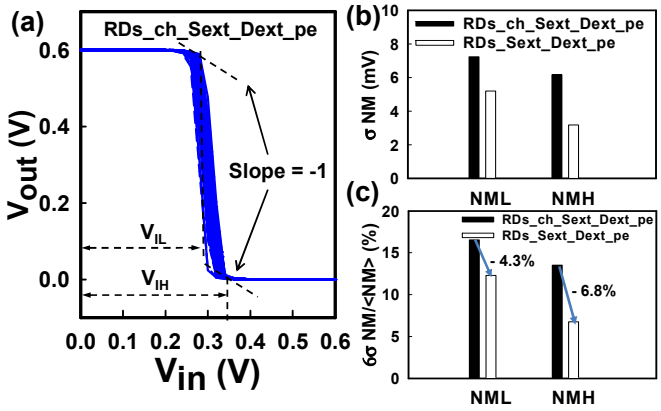

Fig. 3. (a) The fluctuated voltage transfer curves for 10-nm-gate NW MOSFET inverter circuits suffering from RDDs. (b)-(c) Plots of the fluctuated Noise Margin induced by RDs_ch_Sext_Dext_pe and RDs_Sext_Dext_pe, respectively. (b) The standard deviation and (c) the coefficient of variance of noise margin.

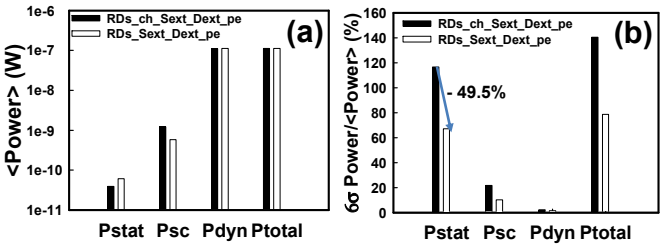

Fig. 4. (a)-(b) The fluctuated power consumption induced by RDs_ch_Sext_Dext_pe and RDs_Sext_Dext_pe, respectively. (a) The averaged and (b) the percentage of variance among various power consumptions. Notably, the averaged static power is the smallest one, but its fluctuation is the most significant with respect to different RDDs.

where $I_{leakage}$ is the leakage current that flows between the power rails when operating at static state. $f_{0->1}$ is the clock rate. I_{sc} is the short circuit current, which observed as both N- and P-type MOSFETs are turned on simultaneously, resulting in a DC path between the power rails. T is the switching period. P_{stat} is equivalent to the product of power supply (V_{DD}) multiplies the $I_{leakage}$. As the V_{DD} is applied, the P_{stat} will consume power, regardless of the switching activity between input and output. The P_{sc} is determined by I_{sc} and the time of existence of DC path between the power rails. The P_{dyn} is determined by the load capacitance (C_{load}). Notably, the gate capacitance (C_g) of transistor is used for C_{load} and highlights variability of the CMOS circuit induced by the fluctuation of the CMOS devices. As shown in Fig. 4(a), the average values of P_{sc} and P_{dyn} are the dominating elements of total power dissipation. As shown in Fig. 4(b), we found that the normalized fluctuation of dynamic power is comparable with/without channel doping and the normalized fluctuation of short-circuit power of CMOS circuit was reduced without channel doping. In particularly, the normalized fluctuations of P_{stat} can be reduced dramatically (49.5% reduction) without channel doping. The averaged static power is the smallest one, but its fluctuation is the most significant with respect to different RDDs. Figure 5 shows the fluctuation of I_{off} (leakage current), I_{sat} (saturation current) and C_g for N-/P-type NW MOSFETs, respectively. Since the leakage

Table I. The associated values of the fluctuation of timing, NM and power consumption on the tested NW CMOS circuits.

Parameter \ Type	RDs_ch_Sext_Dext_pe (%)	RDs_Sext_Dext_pe (%)
THL	15.4	10.7
TLH	15.8	10.1
tf	13.2	8.2
tr	7.2	6
NML	16.6	12.3
NMH	13.5	6.8
Pstat	116.7	67.2
Pdyn	2.1	1.3
Psc	21.7	10.2

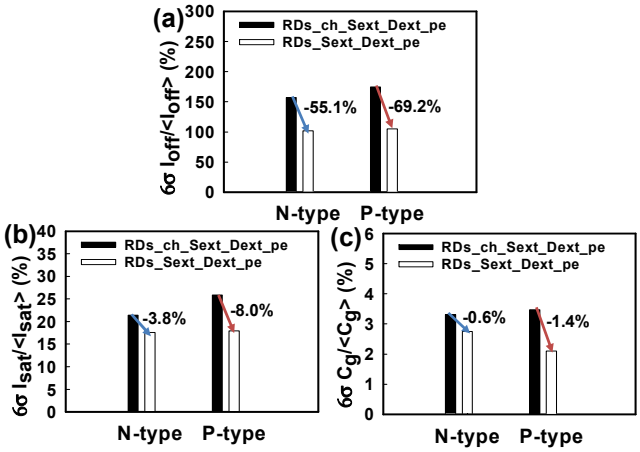

Fig. 5. The coefficient of variance induced by RDs_ch_Sext_Dext_pe and RDs_Sext_Dext_pe (a) I_{off}. (b) I_{sat}. (c) C_g.

current is an exponential function of V_{th} [10], the σI_{off} follows the trend of σV_{th}. Thus, the reduction of I_{off} was due to the reduction of V_{th} without channel doping, as shown in Fig. 5(a). Similarly, we observed that σI_{sat} follows the trend of σV_{th}, as shown in Fig. 5(b). Owing to the P_{stat} is strongly correlated to I_{off}, the reduction of σP_{stat} was attributed to the reduction of σV_{th} and σI_{off}. Additionally, the P_{sc} is highly related to I_{sat}. It can be explained that the fluctuation of P_{sc} is controlled by the fluctuation of I_{sat}. Thus, without channel doping, the fluctuation of P_{sc} can be reduced dramatically due to the reduction of σI_{sat}. As shown in Fig. 5(c), the normalized fluctuation of C_g is small and comparable with/without channel doping due to well control of surrounding gate for NW device. Due to the P_{dyn} is proportional to C_{load}, the normalized fluctuation of P_{dyn} is comparable with/without channel doping. This result is different from planar MOSFETs [9] due to the effects of C_g. The normalized fluctuation of the characteristic parameters of CMOS circuit are summarized in Table I.

IV. Conclusions

In this work, we have explored the timing, NM and power fluctuations on 10-nm-gate GAA silicon NW CMOS circuit induced by various RDDs from channel (with/without doping), S/D extensions and their penetration. Our findings suggest that the fluctuations of the timing, NM and power consumption of CMOS circuit follow the trend of σV_{th}. Thus, the normalized fluctuations of tf, tr, tHL, tLH, NML, NMH and P_{stat} are reduced

by 5.0%, 1.3%, 4.3%, 6.8%, 4.8%, 5.7%, 49.5%, respectively, for the CMOS circuit without channel doping. The characteristic fluctuation of CMOS circuit induced by RDDs inside the S/D regions combined with work function fluctuation will be explored in the future.

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